Buck Quasi-Resonant Converter Operating at Constant Frequency: Analysis, Design, and Experimentation

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Abstract—**A Buck pulsewidth modulated zero-current switching quasi-resonant converter (Buck PWM ZCS QRC) operating at constant frequency is discussed. Operating principle and design-oriented analysis are presented with normalized design curves, design procedure, design example, simulations, and experimental results. The new topology, which can be considered as a particular one, is compared with the well established Buck zero-current switching regulated by frequency modulation (Buck FM ZCS QRC) proposed by Fred C. Lee.**

I. Introduction

RECENTLY the concept of quasi-resonant converters (QRC's) has been introduced to replace the conventional pulsewidth-modulated (PWM) converters in high frequency operation [1]. High power density and high efficiency can be obtained with them, because the commutation takes place under zero-voltage or zero-current.

In QRC's an *LC* resonant circuit is always present and associated with a power switch and a diode to form a resonant commutation cell (RCC). Moreover the *LC* circuit is used to store and transfer energy from input to output in a similar manner to the resonant converters. Consequently the QRC's are regulated by frequency modulation (FM) [2].

To achieve output voltage regulation over a wide range of load and input voltage, the switching frequency range is large, particularly when the unidirectional switch is used. dc voltage-conversion ratio depends on switching and resonant frequencies [2] while the output filter parameters depend on minimum operating frequency. Therefore optimization of circuit components may be difficult.

In this paper a Buck PWM zero-current switching quasi-resonant converter (Buck PWM ZCS QRC) is proposed and compared with the Buck frequency-modulated zero-current switching quasi-resonant converter (Buck FM ZCS QRC).

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II. Buck Pulsewidth Modulated Zero-Current Switching Quasi-Resonant Converter (Buck PWM ZCS QRC)

A. Circuit Description

The Buck FM ZCS QRC and the Buck PWM ZCS QRC are shown in Fig. 1.

Transistor S_1 and diode D_1 form the principal bidirectional current switch. L_r and C_r form the resonant circuit.

Transistor S_2 and diode D_2 form an auxiliary bidirectional current switch, inserted in series with the resonant capacitor C_r. The Buck FM ZCS QRC is generated from the Buck PWM ZCS QRC, by replacing S_2 and D_2 by a short circuit. L_f and C_f form the output filter and R_l represents the load.

To simplify the analysis the following points are assumed:

1) the output filter inductance is sufficiently large to be approximated by a current source with a value equal to output current I;
2) the voltage drop across the conducting semiconductor switches is negligible;
3) the switching times of the transistors are zero;
4) the recovery times of the diodes are zero.

B. Principle of Operation

Fig. 2 shows equivalent circuits of the Buck PWM ZCS QRC in the six topological stages.

Suppose that before S_1 is turned on, output current I flows in diode D and resonant capacitor voltage is equal to zero. A switching cycle begins at $t = t_o$, when S_1 is turned on.

1) Inductor Charging Stage (t_o, t_1) Fig. 2(a): Inductor current i_{L_r} rises linearly and is represented by

$$i_{L_r} = \frac{V_s}{L_r} \cdot t. \tag{1}$$

This stage finishes at time $t = t_1$ when $i_{L_r} = I$, thus,

$$\Delta t_1 = t_1 - t_o = L_r \cdot I / V_s. \tag{2}$$

2) Capacitor Resonant Charging Stage (t_1, t_2), Fig. 2(b): During this stage the current i_{L_r} flows in the diode D_2 and C_r is charged in a resonant way.

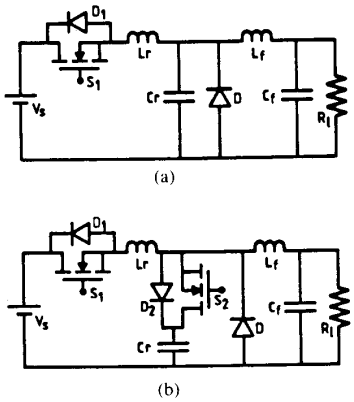


Fig. 1. (a) Buck FM ZCS QRC. (b) Buck PWM ZCS QRC.

The state equations are

$$i_{L_r} - I = C_r \frac{dv_{C_r}}{dt} \tag{3}$$

$$L_r \frac{di_{L_r}}{dt} = V_s - v_{C_r} \tag{4}$$

with the initial conditions

$$v_{C_r}(0) = 0 \quad \text{and} \quad i_{L_r}(0) = I,$$

thus

$$\sqrt{\frac{L_r}{C_r}}\, i_{L_r}(t) = V_s \cdot \sin \omega_o t + \sqrt{\frac{L_r}{C_r}}\, I \tag{5}$$

$$v_{C_r}(t) = V_s(1 - \cos \omega_o t) \tag{6}$$

where

$$\omega_o = 1/\sqrt{L_r C_r}.$$

At time t_2, the current i_{L_r} is equal to I and D_2 is commutated off. The duration of this stage is $\Delta t_2 = t_2 - t_1$.

3) Inductor Constant Current Stage (t_2, t_3) Fig. 2(c): During this stage the inductor current i_{L_r} is equal to I and the voltage capacitor is constant. The duration of this stage is $\Delta t_3 = t_3 - t_2$. If $\Delta t_3 = 0$, the Buck PWM ZCS QRC behaves as a Buck FM ZCS QRC.

4) Capacitor Resonant Discharging Stage (t_3, t_4) Fig. 2(d): At time t_3, to start this stage, transistor S_2 is switched on. The resonant capacitor C_r begins a resonant discharge. Current i_{L_r} continues to oscillate, reduces to zero, and feeds energy back to source V_s. The end of this stage takes place at time $t = t_4$, when i_{L_r} reduces to zero, after flowing through diode D_1. The duration of this stage is $\Delta t_4 = t_4 - t_3$.

With the initial conditions $v_{C_r}(0) = 2V_s$ and $i_{L_r}(0) = I$ one obtains

$$v_{C_r}(t) = V_s(1 + \cos \omega_o t) \tag{7}$$

$$\sqrt{\frac{L_r}{C_r}}\, i_{L_r}(t) = -V_s(\sin \omega_o t) + \sqrt{\frac{L_r}{C_r}}\, I. \tag{8}$$

By setting $i_{L_r}(\Delta t_4) = 0$ one obtains

$$v_{C_r}(\Delta t_4) = V_s(1 + \cos \gamma) \tag{9}$$

$$\gamma = \omega_o \cdot \Delta t_4. \tag{10}$$

5) Capacitor Linear Discharging Stage (t_4, t_5) Fig. 2(e): During this stage the capacitor C_r discharges linearly and at time $t = t_5$ v_{C_r} reaches zero. The state equation is given by

$$C_r \frac{dv_{C_r}}{dt} = I. \tag{11}$$

Thus

$$v_{C_r}(t) = V_s(1 + \cos \gamma) - \frac{I}{C_r} t \tag{12}$$

At time $t = \Delta t_5$, $v_{C_r}(t) = 0$, so:

$$\Delta t_5 = \frac{C_r \cdot V_s(1 + \cos \gamma)}{I}. \tag{13}$$

6) Free-Wheeling Stage (t_5, t_6) Fig. 2(f): In this stage the output current flows through diode D. It finishes at time t_6, when a new operating cycle begins. The duration of this stage is $\Delta t_6 = t_6 - t_5$.

C. Waveforms and State-Plane

Typical circuit waveforms are shown in Fig. 3. The corresponding state-plane is shown in Fig. 4. As it can be seen, both switches commutate under zero-current. The difference with respect to the operation of the Buck FM ZCS QRC is the time interval Δt_3 which is equal to zero.

III. Design Considerations and Procedure

A. DC Voltage-Conversion-Ratio and Duty-Cycle

By analysis one can obtain the dc voltage-conversion-ratio, given by

$$\frac{V_o}{V_s} = \frac{1}{2\pi} \frac{f}{f_o} \left\{ \frac{\alpha}{2} + \frac{1}{\alpha} - \sqrt{\frac{1}{\alpha^2}} - 1 + 2\pi - \sin^{-1} \right\} + \frac{\Delta t_3}{T} \tag{14}$$

where

$$\alpha = \frac{I}{V_s} \sqrt{\frac{L_r}{C_r}}$$

f = switching frequency

$$f_o = 1/2\pi \sqrt{L_r C_r}.$$

A simplified equation, sufficiently accurate to represent the behavior of the converter is given by

$$\frac{V_o}{V_s} = \frac{f}{f_o} + \frac{\Delta t_3}{T}. \tag{15}$$

Therefore, if f and f_o are fixed, output voltage can be regulated by variation of $\Delta t_3/T$, which represents a duty-cycle, as in a conventional PWM converter.

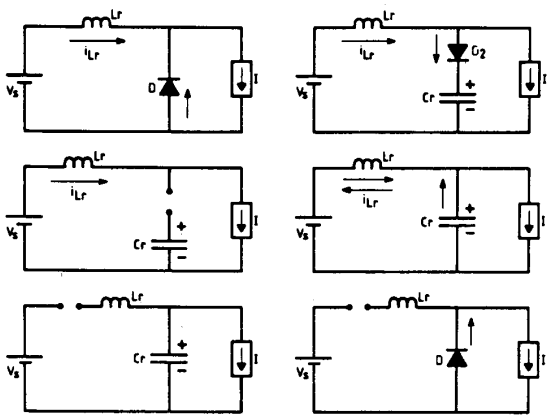


Fig. 2. Equivalent circuit of Buck PWM ZCS QRC in six topological stages of switching cycle. (a) Inductor charging stage (t_o, t_1). (b) Capacitor resonant charging stage (t_1, t_2). (c) Inductor constant current stage (t_2, t_3). (d) Capacitor resonant discharging stage (t_3, t_4). (e) Capacitor linear discharging stage (t_4, t_5). (f) Free-wheeling stage (t_5, t_6).

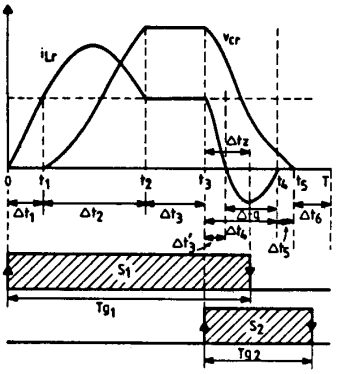


Fig. 3. Waveforms for Buck PWM ZCS QRC.

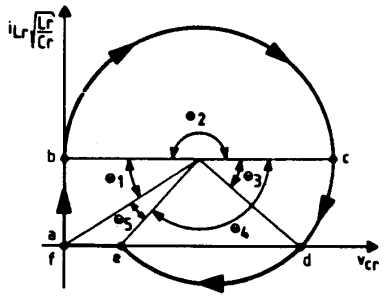


Fig. 4. Buck PWM ZCS QRC stage-plane ($\theta_n = \omega_o \cdot \Delta t_n$).

The graphical representation of (15) is shown in Fig. 5. The operating principle of the Buck PWM ZCS QRC requires that

$$\frac{V_o}{V_s} < 1 \quad \text{and} \quad 0 < \frac{f}{f_o} < 1.$$

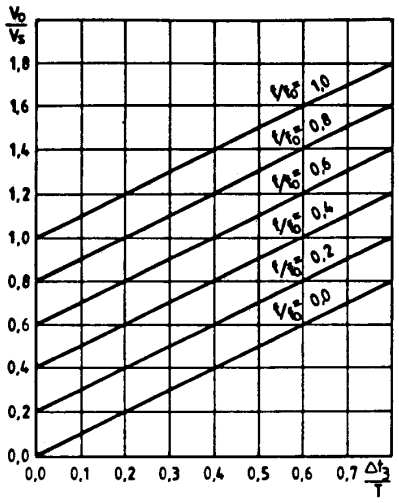


Fig. 5. Buck PWM ZCS QRC dc voltage-conversion ratio.

The input data for the design of the converter includes:

input voltage range V_s min, V_s max;
output voltage V_o;
switching frequency f;
output power range $P_{\min}$, $P_{\max}$.

By taking $\Delta t_3/T = 0$, f/f_o is determined by

$$f/f_o = V_o/V_{s\max} \tag{16}$$

The maximum value of $\Delta t_3/T$ is given by

$$\left[\frac{\Delta t_3}{T}\right]_{\max} = \frac{V_o}{V_{s\min}} - \frac{f}{f_o}. \tag{17}$$

B. Condition for Zero-Current Switching

The condition for zero-current switching, as shown in the state-plane, is given by $\alpha_{\max} < 1$, where

$$\alpha_{\max} = \frac{I_{\max}}{V_{s\min}}\sqrt{\frac{L_r}{C_r}} \tag{18}$$

and

$$I_{\max} = P_{\max}/V_o. \tag{19}$$

C. Parameters of Resonant Circuit

The parameters L_r and C_r of the resonant circuit are given by

$$L_r C_r = \frac{1}{(2\alpha f_0)^2} \tag{20}$$

$$\frac{L_r}{C_r} = \left[\frac{V_{s\min}\alpha_{\max}}{I_{\max}}\right]^2. \tag{21}$$

D. Time Conduction of Transistor $S_2(Tg_2)$

As shown in Fig. 3, before the gate voltage of transistor S_2 is made equal to zero, the linear discharging state of the resonant capacitor C_r must be completed.

Therefore

$$Tg_2 > \Delta t_x \tag{22}$$

$$\Delta t_x = \Delta t_4 + \Delta t_5. \tag{23}$$

So

$$\frac{\Delta t_x}{T} = \frac{1}{2\pi}\frac{f}{f_o}\left\{\pi - \sin^{-1}\alpha + \frac{1}{\alpha} - \sqrt{\frac{1}{\alpha^2} - 1}\right\}. \tag{24}$$

The expression (24) is graphically represented in Fig. 6.

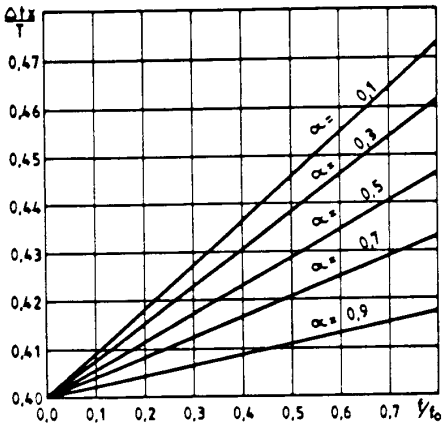


Fig. 6. Ratio of time interval Δt_x to switching period T.

E. Limit of Duty-Cycle ($\Delta t_3/T$)

According to waveforms that are shown in Fig. 3, to assure the complete discharging of capacitor C_r before the beginning of a new operating-cycle, the following inequality must be verified:

$$\Delta t_1 + \Delta t_2 + \Delta t_3 + \Delta t_4 + \Delta t_5 < T. \tag{25}$$

Thus

$$\left[\frac{\Delta t_3}{T}\right]_L = 1 - \frac{1}{2\pi}\frac{f}{f_o} \cdot \left[2\pi + \alpha + \frac{1}{\alpha} - \sin^{-1}\alpha - \sqrt{\frac{1}{\alpha^2} - 1}\right] \tag{26}$$

where $[\Delta t_3/T]_L$ is a theoretical limit value.

This means that for given values of f, f_o and α, the maximum duty-cycle obtained by (17) must be lower than the limit value obtained by (26).

The simplified form of (26) is given by

$$\left[\frac{\Delta t_3}{T}\right]_L = 1 - \frac{f}{f_o}. \tag{27}$$

F. Time Interval Between Turn-On of S_1 and Turn-Off of S_2

Transistor T_1 must be turned off during the time interval so that current i_{L_r} flows through the antiparallel diode D_1, which is represented by Δt_q in Fig. 3. Let us consider the expressions as follows:

$$\Delta t_4 = \Delta t_3' + \Delta t_q \tag{28}$$

$$\Delta t_3' = \Delta t_4 - \Delta t_q \tag{29}$$

$$\Delta t_3' < \Delta t_z < \Delta t_4 \tag{30}$$

$$\Delta t_4 - \Delta t_q < \Delta t_z < \Delta t_4 \tag{31}$$

$$\frac{\Delta t_q}{T} = \frac{1}{2\pi}\frac{f}{f_o}\left[\pi - 2 \cdot \sin^{-1}\alpha\right] \tag{32}$$

$$\frac{\Delta t_4}{T} = \frac{1}{2\pi}\frac{f}{f_o}\left[\pi - \sin^{-1}\alpha\right] \tag{33}$$

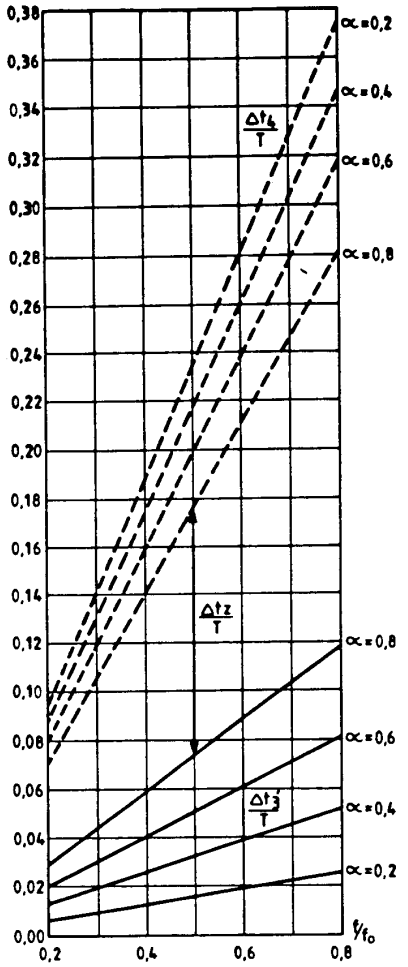


Fig. 7. $\Delta t_z/T$ as function of f/f_o taking α as parameter ($\Delta t_z/T < \Delta t_4/T - \Delta t_3'/T$).

$$\frac{\Delta t_4}{T} - \frac{\Delta t_q}{T} = \frac{1}{2\pi}\frac{f}{f_o}\sin^{-1}\alpha \tag{34}$$

$$\frac{1}{2\pi}\frac{f}{f_o}\cdot\sin^{-1}\alpha < \frac{\Delta t_z}{T} < \frac{1}{2\pi}\frac{f}{f_o}[\pi - \sin^{-1}\alpha]. \tag{35}$$

Δt_z represents the time interval. S_1 must be turned off, after S_2 is turned on, as shown in Fig. 7.

IV. Design Example

1) Input data:

$$V_{s\max} = 56\text{ V}$$
$$V_{s\min} = 40\text{ V}$$
$$P_{\max} = 100\text{ W}$$
$$P_{\min} = 20\text{ W}$$
$$V_o = 24\text{ V}$$
$$f = 400\text{ kHz}.$$

2) $I_{\max} = (P_{\max}/V_o) = (100/24) = 4.17$ A

$$I_{\min} = \frac{P_{\min}}{V_o} = \frac{20}{24} = 0.83\text{ A}$$

$$\frac{V_o}{V_{s\max}} = \frac{24}{56} = 0.43$$

$$\frac{V_o}{V_{s\min}} = \frac{24}{40} = 0.6$$

$$T = 2.5\ \mu\text{s}.$$

3) For $\Delta t_3/T = 0$, $f/f_o = V_o/V_{s\max} = 0.43$.

To compensate the power switch voltage drops it is taken that $f/f_o = 0.30$.

Therefore,

$$f_o = \frac{f}{0.3} = 1.336\text{ MHz} = \frac{1}{\sqrt{L_rC_r}\times 2\pi}.$$

Thus $L_rC_r = 1.426\times 10^{-14}$.

4) Let us choose $\alpha_{\max} = 0.6$

$$\alpha_{\max} = \frac{I_{\max}}{V_{s\min}}\sqrt{\frac{L_r}{C_r}}$$

thus

$$\frac{L_r}{C_r} = 33.12$$

consequently,

$$L_r = 0.68\ \mu\text{H} \quad \text{and} \quad C_r = 20\text{ nF}.$$

5) $[\Delta t_3/T]_{\max} = (V_o/V_{s\min}) - (f/f_o) = 0.6 - 0.3 = 0.30$.

Therefore, $\Delta t_{3\max} = 0.75\ \mu$s. For this case, the limit of duty-cycle is given by

$$\left[\frac{\Delta t_3}{T}\right]_L = 1 - \frac{f}{f_o} = 1 - 0.30 = 0.70.$$

Therefore, $\Delta t_{3_L} = 1.75\ \mu$s.

As $[\Delta t_3/T]_L > [\Delta t_3/T]_{\max}$, the converter can supply maximum output power at minimum input voltage, preserving the natural commutation.

6) $\Delta t_q/T = (1/2\pi)(f/f_o)[\alpha - 2\sin^{-1}\alpha] = (1/2\pi)\,0.30\,[\pi - 2\times 0.64]$

$$\frac{\Delta t_q}{T} = 0.09 \qquad \Delta t_q = 0.225\ \mu\text{s}.$$

7) $\Delta t_4/T = (1/2\pi)\cdot(f/f_o)\,[\pi - \sin^{-1}\alpha] = (0.30/2\pi)\,[\pi - 0.64]$

$$\frac{\Delta t_4}{T} = 0.12 \quad \therefore\ \Delta t_4 = 0.30\ \mu\text{s}.$$

8) $\Delta t_4 - \Delta t_q = 0.30 - 0.225 = 0.075\ \mu$s, thus $0.075\ \mu\text{s} < \Delta t_z < 0.30\ \mu$s.

9) $\Delta t_1/T = (\alpha/2\pi)(f/f_o) = 0.6\times 0.30/2\pi = 0.029$; $\Delta t_1 = 0.0725\ \mu$s.

10) $\Delta t_2/T = (1/2)(f/f_o) = 0.5\times 0.30 = 0.15$

$$\Delta t_2 = 0.375\ \mu\text{s}.$$

11) $\Delta t_5/T = (1/2\pi)\,(f/f_o)\,[(1/\alpha) - \sqrt{(1/\alpha^2) - 1}]$

$$\frac{\Delta t_5}{T} = \frac{0.3}{2\pi}[1.67 - 1.333] = 0.016$$

$$\Delta t_5 = 0.04\ \mu\text{s}.$$

12) For correct operation $\Delta t_6 = T - t_5$, must be greater than zero, which is confirmed as

$$t_5 = \Delta t_1 + \Delta t_2 + \Delta t_{3\max} + \Delta t_4 + \Delta t_5$$
$$\Delta t_5 = 1.54\ \mu\text{s}$$
$$T = 2.5\ \mu\text{s}$$
$$\Delta t_6 = 0.96\ \mu\text{s}.$$

13) The gate-drive signals, for the maximum duty-cycle, are represented in Fig. 8.

$$Tg_{1\max} = \Delta t_1 + \Delta t_2 + \Delta t_{3\max} + \Delta t_z.$$

By taking $\Delta t_z = 0.2\ \mu$s one obtains

$$Tg_{1\max} = 1.397\ \mu\text{s}$$
$$Tg_{1\min} = \Delta t_1 + \Delta t_2 + \Delta t_z$$
$$Tg_{1\min} = 0.647\ \mu\text{s}$$
$$Tg_2 = \Delta t_4 + \Delta t_5 + \Delta t_6/2$$
$$Tg_2 = 0.82\ \mu\text{s}.$$

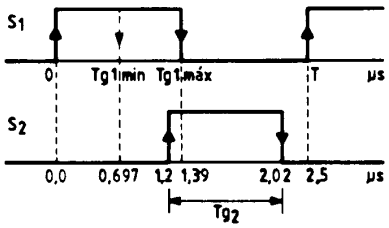


Fig. 8. Gate-drive signals for maximum duty-cycle.

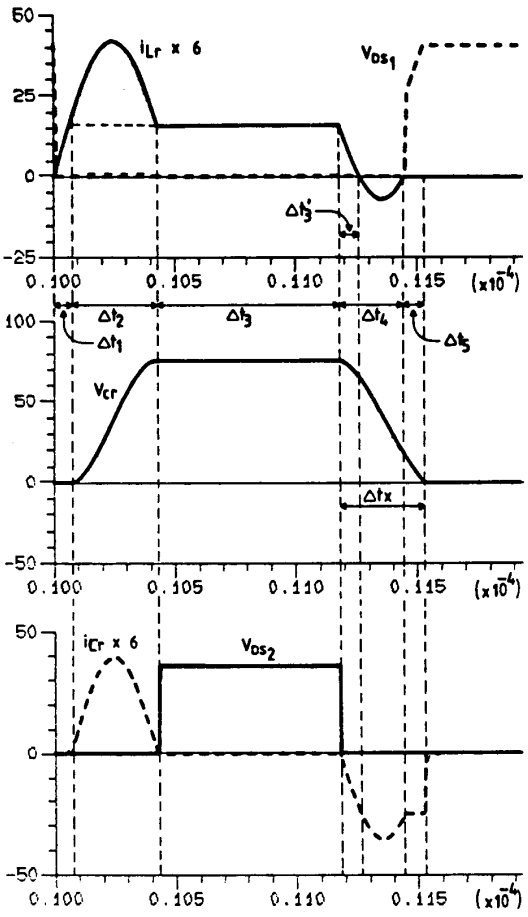


Fig. 9. Simulation results using parameters obtained by design, for V_s = 40 V; P = 100 W; R_l = 5.7 Ω; and $\Delta t_3/T$ = 0.3.

V. Simulation Results

Fig. 9 shows a simulation of the Buck PWM ZCS QRC with the parameters obtained by design example in the preceding paragraph. It can be seen that both transistors commutate under zero-current, as previously mentioned.

VI. Experimental Results

Following the design outlined in the preceding section, a Buck PWM ZCS QRC was implemented, with the following specifications:

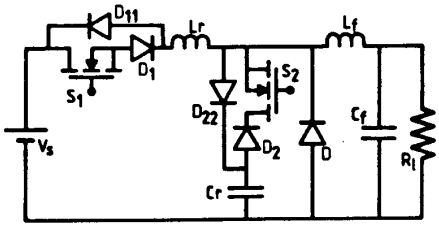
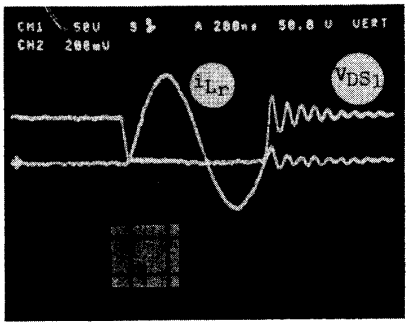
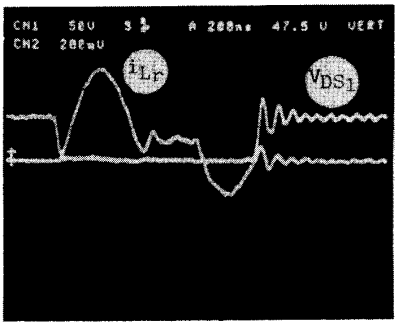


Fig. 10. Power stage circuit diagram of the implemented Buck PWM ZCS QRC.



(a)



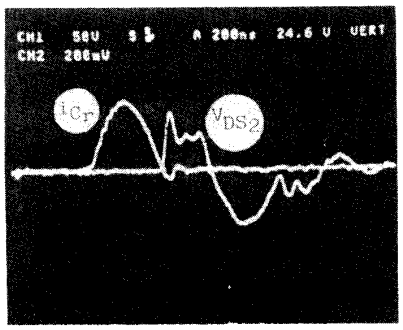
(b)

Fig. 11. Experimental waveforms of L_r current and S_1 drain-to-source voltage. (a) $\Delta t_3/T$ = 0. (b) $\Delta t_3/T$ = 0.12. i_{Lr}: 4 A/div and v_{DS1}: 50 V/div.

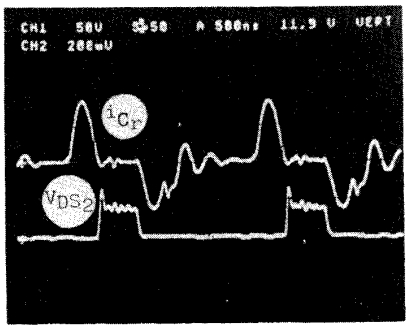
output power range P = 20 − 100 W;
input voltage range V_s = 40;
output voltage V_o = 24 V − 56 V
switching frequency f = 400 kHz.

The circuit diagram of the converter is shown in Fig. 10. The power stage consists of the following parameters:

S_1, S_2	IRF 640 (Motorola);
D_1, D_{11}, D_2, D_{22}	MUR 1515 (Motorola);
C_r	20 nF, polypropylene (Icotron);
L_r	0.66 μH, 3 turns on ferrite core E-20;
D	MUR 1515 (Motorola);
L_f	100 μH, 22 turns on ferrite core E-30/14;
C_f	2 μF, polypropylene (Icotron).

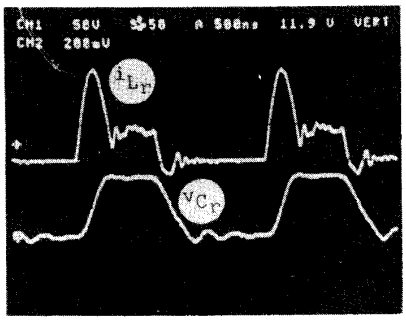


(a)

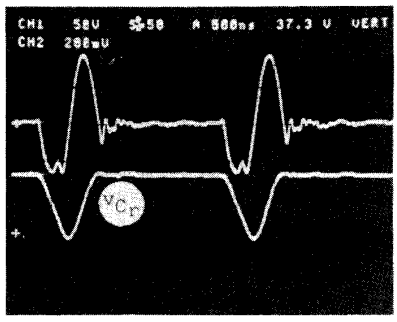


(b)

Fig. 12. Experimental waveforms of C_r current and S_2 drain-to-source voltage. (a) $\Delta t_3/T = 0.1$. (b) $\Delta t_3/T = 0.2$. i_{C_r}: 4 A/div and v_{DS_2}: 50 V/div.



(a)



(b)

Fig. 13. Experimental waveforms of L_r current and C_r voltage. (a) $\Delta t_3/T = 0.25$. (b) $\Delta t_3/T = 0.7$. i_{L_r}: 4 A/div and v_{C_r}: 50 V/div.

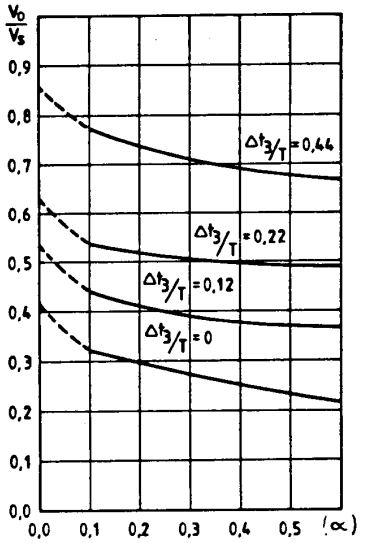


Fig. 14. Experimental output characteristics.

Experimentally obtained waveforms of the inductor L_r current and drain-to-source voltage across transistor S_1 are shown in Fig. 11. The capacitor current i_{C_r} and drain-to-source voltage across transistor S_2 are shown in Fig. 12. These waveforms agree with those predicted theoretically.

Both transistors turn on and turn off under zero-current, assuring practically zero switching losses.

The inductor current i_{L_r} and the capacitor voltage v_{C_r} are shown in Fig. 13. Notice that in Fig. 13(b) the converter is operating at limit duty-cycle $\Delta t_3/T = 0.7$, which agrees with the predicted theoretical value obtained in the design example.

The dc voltage-conversion ratio versus α, for various values of $\Delta t_3/T$, obtained experimentally, is shown in Fig. 14. In fact, it represents the output-characteristic of the Buck PWM ZCS QRC. Due to on-resistance of S_1 and voltage drop of D_1, the output voltage reduces as the output current increases.

VII. Conclusion

The well established Buck FM ZCS QRC, which is regulated by frequency modulation by inserting an auxiliary bidirectional switch, was transformed into a Buck PWM ZCS QRC.

Theoretical analysis, design procedures and design example have been presented in the paper. A laboratory prototype rated at 100 W, operating at switching frequency of 400 kHz and resonant frequency of 1.35 MHz has been implemented and tested. Operating principle and theoretical analysis has been confirmed by experimental results.

The same technique extended to other QRC's, including the zero-voltage switching, the isolated and the symmetrical QRC, is under investigation and promises the same success.

Regulation of resonant-mode power converters at constant frequency is a very desirable property, though not easy to achieve, and constitutes one of the most important trends in power electronics research. So we can expect important progress on this subject in the near future.

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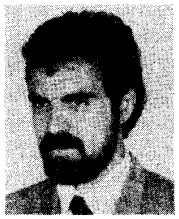

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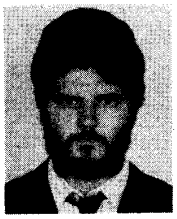

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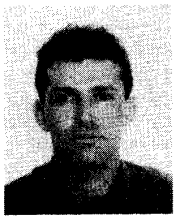

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