The Three-Level ZVS-PWM DC-to-DC Converter

José Renes Pinheiro and Ivo Barbi, *Senior Member, IEEE*

***Abstract*—A new high frequency dc-to-dc power converter for high voltage and high power is introduced in this paper, which features zero-voltage-switching, operation at constant frequency, regulation by pulsewidth modulation, and low rms current stress upon power switches. Its greatest attribute, in comparison with the full-bridge (FB-ZVS-PWM) converter, is that the voltage across the switches is half of the input voltage. This property is achieved due to the employment of a three-level leg in place of the conventional two-switch leg. Operation, analysis, design procedure and example, and simulation are presented. A prototype operating at 100 kHz, rated at 600 V input voltage, and 1.5 kW output power and 25 A output current has been fabricated and successfully tested in the laboratory.**

NOMENCLATURE

$C_{1\text{-}4}$	MOSFET intrinsic capacitance.
$C_{a1\text{-}2}$	Auxiliary commutation capacitance.
C_b	Blocking dc capacitance.
C_f	Filter capacitance.
C_r	Resonant capacitance.
C_s	Snubber capacitance.
D	Control duty-cycle.
$D_{1\text{-}4}$	MOSFET intrinsic diode.
Δ	Reduction of the duty-cycle.
$D_{c1\text{-}2}$	Clamping diode.
D_{eff}	Effective duty-cycle
$D_{r1\text{-}4}$	Rectifier diode.
D_s	Snubber diode.
E	Input source.
f_s	Switching frequency.
$i_{M1\text{-}4}$	MOSFET drain current.
i_{Lr}	Resonant inductor current.
$I_{\min}$	Minimum load current.
I_o	Load current.
L_a	Auxiliary commutation inductor.
L_f	Filter inductance.
L_r	Resonant inductance.
$M_{1\text{-}4}$	Power MOSFET.
n	Transformer turn ratio.
P_o	Output power.
R_o	Load resistance.
R_s	Snubber resistance.
$S_{1\text{-}4}$	Semiconductor switch.
t	Time.
Tr	Transformer.
T_s	Switching period.
v_{ab}	Voltage between the points a and b.
$v_{C1\text{-}4}$	MOSFET intrinsic capacitance voltage.
V_o	Output voltage.
$v_{ds1\text{-}4}$	Drain-source voltage.
ω_r	Resonant angular frequency.
Z_r	Resonant characteristic impedance.

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J. R. Pinheiro is with the Federal University of Santa Maria, Brazil.

I. Barbi is with the Power Electronics Laboratory, Federal University of Santa Catarina, Florianópolis, Brazil.

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I. INTRODUCTION

ENGINEERS involved in the design of high frequency switching mode power supplies for high power application presently recognize that one of the best power converter topologies is the FB-ZVS-PWM converter [1], [2]. This is because it possesses the basic desirable characteristics of both the hard switching PWM converters and the soft switching ones, while avoiding their major drawbacks, such as commutation losses in the former, and variable switching frequency and high conduction losses in the second group. However, the power switches of the FB-ZVS-PWM converter are subjected to the maximum input voltage level. In the cases where the input voltage is high, it may not be possible to get adequate switches. In order to reduce the voltage stress of the switches, this paper proposes the three-level (TL-ZVS-PWM) dc-to-dc converter. As is demonstrated hereafter, this new topology operates like the FB-ZVS-PWM converter from the commutation standpoint, having identical output characteristics and power transfer control. In addition, the maximum voltage across the switches is half the value of the input voltage. The TL-ZVS-PWM converter offers a clear advantage over the FB-ZVS-PWM converter since switch voltage stress is reduced to one-half the input voltage. Lower switch stress offers the advantages of reduced power switching device cost and higher reliability due to lower switching stress. This technique was inspired by the hard switched three-level inverter [3].

II. THE THREE-LEVEL ZERO-VOLTAGE-SWITCHING PULSEWIDTH-MODULATED DC-TO-DC CONVERTER (TL-ZVS-PWM)

A. Circuit Description

The TL-ZVS-PWM converter proposed in this paper is shown in Fig. 1. The main commutation leg is formed by M_1, M_2, M_3, and M_4. D_1, D_2, D_3 and D_4 are the MOSFET's body diodes, while C_1, C_2, C_3, and C_4 are the MOSFET's intrinsic capacitors, employed to perform the commutation at zero voltage. No external commutation capacitors are needed. L_r is the commutation inductor, composed of an external inductor plus the leakage inductor of the transformer. T_r is the isolation transformer. The output stage is formed by rectifiers

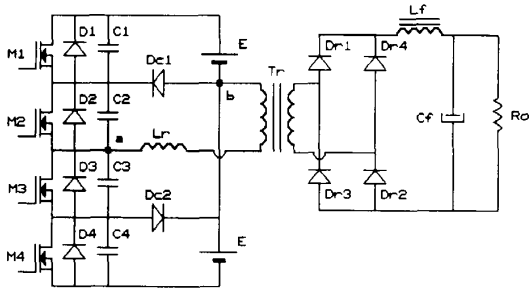


Fig. 1. Proposed TL-ZVS-PWM dc-to-dc converter.

D_{r1}, D_{r2}, D_{r3}, and D_{r4} and the output filter composed of L_f and C_f. D_{c1} and D_{c2} constitute the clamping diodes. R_o represents the load resistance.

B. Principle of Operation

To simplify the analysis, the following assumptions are made: 1) the circuit operates in a steady-state. 2) All power semiconductors are ideal. 3) The MOSFET's intrinsic capacitances are constant and incorporate all the transformer's parasitic capacitances. 4) The output filter inductance is sufficiently large to be approximated by a current source with a value equal to load current I_o. 5) The transformer magnetizing current is neglected.

Fig. 2 shows the seven topological stages for a half-period of operation. The main waveforms are represented in Fig. 3. The operation is described as follows:

First Stage (t_0, t_1): During this stage the load current flows through M_1, M_2, D_{r1}, and D_{r2}. $v_{C1} = v_{C2} = 0, v_{C3} = V_{C4} = E$ and $i_{Lr} = I_o$ [Fig. 2(a)].

Second Stage (t_1, t_2): This stage begins at time t_1, when M_1 is gated off and turns off in a soft-switching manner. Voltage v_{C1} increases from zero to E, while $(v_{C3} + v_{C4})$ decreases from $2E$ to E. This stage ends at instant t_2, when D_{c1} is directly polarized and starts conducting. Through output rectifiers D_{r1} and D_{r2} flows the load current [Fig. 2(b)].

Third Stage (t_2, t_3): This is a free-wheeling stage, during which the load current flows through D_{c1}, M_2, L_r and the output rectifiers (D_{r1} and D_{r2}) [Fig. 2(c)].

Fourth Stage (t_3, t_4): At moment t_3, M_2 is gated off and turns off in a soft-switching manner. Capacitor voltage v_{C2} increases up to E while $(v_{C3} + v_{C4})$ decreases towards zero. This stage ends when v_{C2} reaches E. All output rectifiers are conducting, therefore short-circuiting the output stage [Fig. 2(d)].

Fifth Stage (t_4, t_5): During this stage, current i_{Lr} flows through diodes D_3 and D_4 and decreases linearly. During the conduction of D_3 and D_4, switches M_3 and M_4 are gated on at zero-voltage and zero-current [Fig. 2(e)].

Sixth Stage (t_5, t_6): When i_{Lr} reaches zero, D_3 and D_4 turn off and M_3 and M_4 start conducting. Current i_{Lr} increases linearly in the reverse direction [Fig. 2(f)].

Seventh Stage (t_6, t_7): This stage begins when i_{Lr} reaches load current I_o. Output rectifiers D_{r1} and D_{r2} turn off naturally, and only through D_{r3} and D_{r4} does the load current flow [Fig. 2(g)].

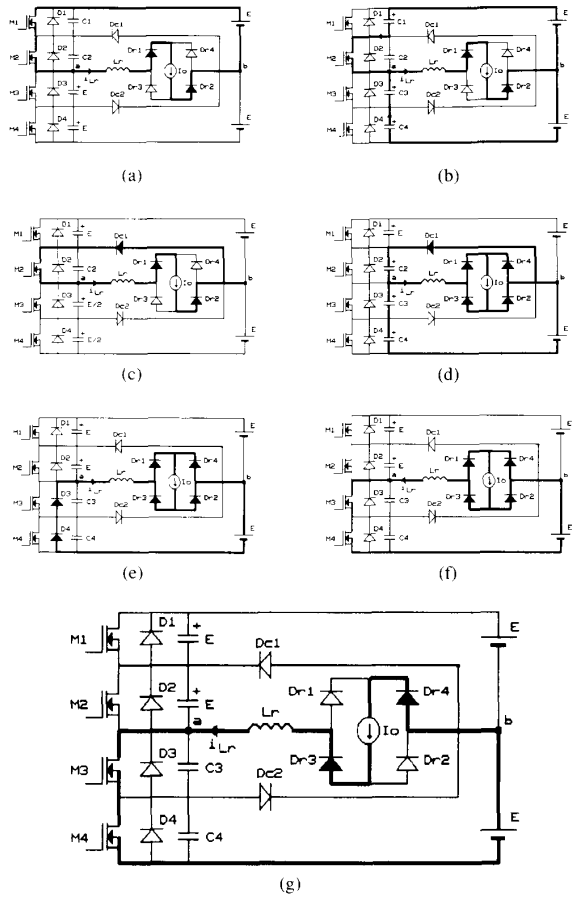


Fig. 2. Stages of operation of the TL-ZVS-PWM converter. (a) First stage. (b) Second stage. (c) Third stage. (d) Fourth stage. (e) Fifth stage. (f) Sixth stage. (g) Seventh stage.

The second half-period which is identical to the first one is omitted in this paper.

The power transfer from the input source to the load occurs during the first stage of operation, when both M_1 and M_2 conduct current i_{Lr}.

During the third stage, the output current free-wheels through M_2, D_{c1}, L_r, and the output rectifier. Thus, the voltage applied to the load, neglecting the commutation intervals, depends on the M_1 conduction time over the half-period. Consequently the power transfer is controlled in a manner similar to the hard-switching PWM converter.

III. Theoretical Analysis

A. Output Characteristics

According to the waveforms shown in Fig. 3, and considering that the commutation time is much smaller than the switching period, the average output voltage is given by

$$V_o = \frac{2E(t_1 - t_0)}{T_s}. \quad (1)$$

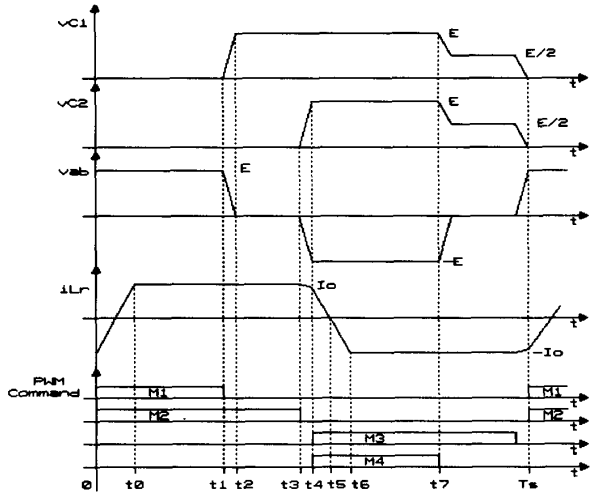


Fig. 3. Main theoretical waveforms.

During time interval $(0, t_0)$, current i_{Lr} is represented by

$$i_{Lr} = -I_0 + \frac{E}{L_r}t. \tag{2}$$

At time $t = t_0, i_{Lr} = I_o$. Thus

$$t_0 = \frac{2L_rI_o}{E}. \tag{3}$$

By substituting (3) into (1) we obtain

$$V_o = E\left(\frac{2t_1}{T_s} - \frac{4f_sL_rI_o}{E}\right). \tag{4}$$

Let us define the control duty-cycle as

$$D = \frac{2t_1}{T_s} \tag{5}$$

and the reduction of the duty-cycle is given by

$$\Delta = \frac{4f_sL_rI_o}{E}. \tag{6}$$

The effective duty-cycle is defined as

$$D_{\text{eff}} = \frac{V_o}{E}. \tag{7}$$

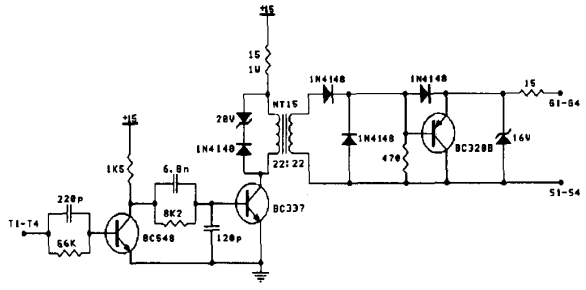
Hence,

$$\frac{V_o}{E} = D - \frac{4f_sL_rI_o}{E} \tag{8}$$

or

$$D_{\text{eff}} = D - \Delta. \tag{9}$$

Equation (8) represents the dc voltage-conversion-ratio of the TL-ZVS-PWM converter. Notice that the larger L_r is, the larger also is the reduction of the output voltage caused by the reactive voltage drop.



(a)

Fig. 4. (a) Drive circuit.

B. Commutation Analysis

During time interval (t_1, t_2), voltages v_{C1} and $(v_{C3} + v_{C4})$ are represented as follows:

$$v_{C1} = \frac{I_o t}{1.5C} \tag{10}$$

and

$$v_{C3} + v_{C4} = 2E - \frac{I_o t}{1.5C} \tag{11}$$

where C represents the intrinsic capacitance of each MOSFET.

The second and more critical commutation takes place during time interval (t_3, t_4) where v_{C2} increases from zero up to E and $(v_{C3} + v_{C4})$ reduces from E to zero. If v_{C2} does not reach E, the soft-commutation is not achieved.The voltage across C_2 is governed by

$$v_{C2} = \sqrt{\frac{L_r}{1.5C}}I_o \sin(\omega_r t) \tag{12}$$

where

$$\omega_r = \frac{1}{\sqrt{1.5L_rC}} \tag{13}$$

and

$$Z_r = \sqrt{\frac{L_r}{1.5C}}. \tag{14}$$

At $\omega_r t = \pi/2$, capacitor voltage v_{c2} is

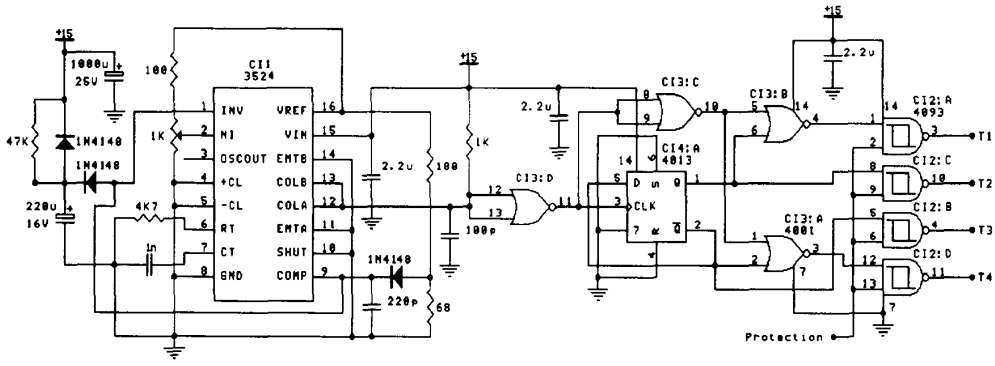
$$v_{C2} = I_o\sqrt{\frac{L_r}{1.5C}} \tag{15}$$

and letting $I_o = I_{\min}$ and $v_{C2} = E$, then

$$I_{\min} = E\sqrt{\frac{1.5C}{L_r}}. \tag{16}$$

In order to ensure the soft-commutation, $I > I_{\min}$.

According to (6) and (16), the wider the load range with ZVS is, which implies smaller minimum load current $I_{\min}$, the higher is the reactive voltage drop across commutation



(b)

Fig. 4. (Cont.'d) (b) Command circuit.

inductor L_r. In other words, a wide load range yields a large amount of the circulating energy, increasing the conduction losses. However, this problem is not a characteristic of the TL-ZVS-PWM converter, since it is also encountered in other ZVS converters.

A good design involves sacrificing the soft-commutation at low load, where the conduction losses are low, to obtain a high efficiency at full-load.

IV. Simplified Design Procedure and Example

The design of the TL-ZVS-PWM converter is similar to that of the FB-ZVS-PWM converter, as it is presented in [2] and [4], whereas a simplified approach is presented hereafter. The main purpose of this section is to use the deduced equations to define the components for simulation and fabrication of a prototype.

a) Input data

P_o=	1.5 kW (rated output power)
E=	300 V (half input voltage)
V_o=	60 V (output voltage)
f_s=	100 kHz (switching frequency)
I_o=	25 A (rated output current).

b) The effective duty-cycle D_{eff} is chosen to be 0.6 and L_r is chosen in such a way that it causes 20% of reduction in duty-cycle D. Thus, from (9):

$$D = 0.6 + 0.2D$$

hence

$$D = 0.75.$$

Isolating L_r from (6), we obtain

$$L_r = \frac{0.2DnE}{4f_s I_0}$$

where

$$\frac{nV_o}{E} = 0.6.$$

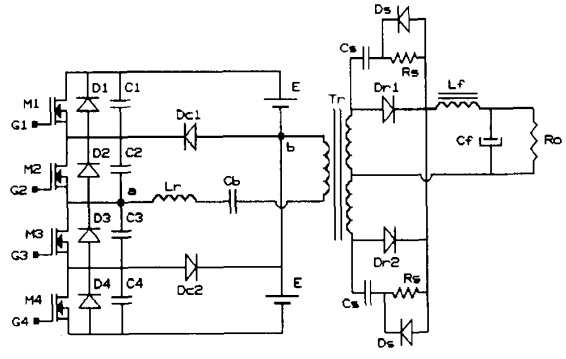


Fig. 5. Power stage diagram of the implemented TL-ZVS-PWM power supply.

Then

$$L_r = 13.5\,\mu\text{H}.$$

A value equal to 16.0 μH was adopted. As the measured leakage transformer inductance was 4 μH, the value of the external inductance is equal to 12 μH.

c) The chosen MOSFET (APT5040) to meet voltage and current requirements has an intrinsic capacitance equal to 500 pF.

So the minimum current to ensure ZVS is

$$I_{\min} = E\sqrt{\frac{1.5C}{L_r}} = 2.10\,\text{A}$$

which corresponds to 6.3 A at the load, representing 25% of the full load current.

V. Experimental Results

Following the design outlined in the preceding section, a TL-ZVS-PWM dc-to-dc converter was implemented, with the following specifications:

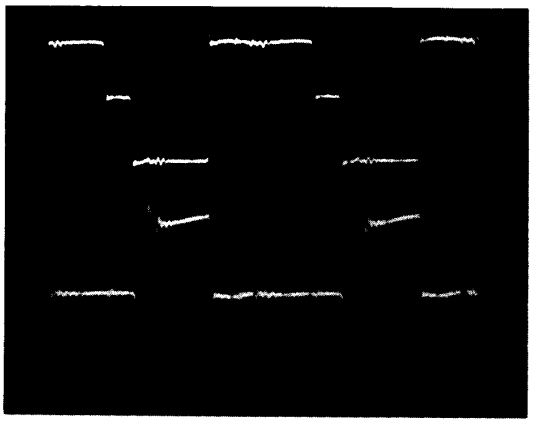


Fig. 6. Experimental waveforms. Upper trace: Drain-to-source voltage v_{ds1}. Scales: 100 V/div. 2 μs/div. Lower trace: Drain current i_{M1}. Scales: 5 A/div., 2 μs/div.

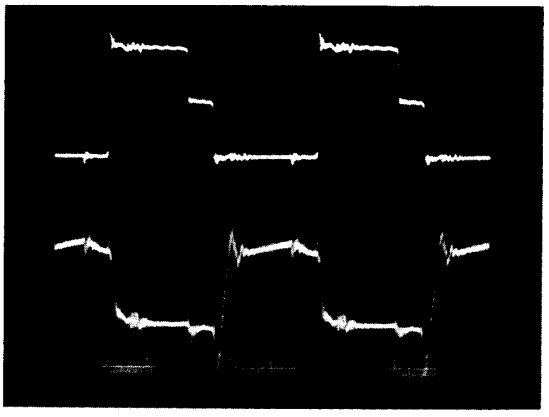


Fig. 7. Experimental waveforms. Upper trace: Drain-to-source voltage v_{ds2}. Scales: 100 V/div., 2 μs/div. Lower trace: drain current i_{M2}. Scales: 5 A/div, 2 μs/div.

output power:	$P_o = 1500$ W;
output voltage:	$V_o = 60$ V;
input voltage:	$2E = 600$ V;
switching frequency:	$f_s = 100$ kHz.

The implemented drive and command circuits are shown in Fig. 4(a) and (b), respectively. The power stage of the converter is shown in Fig. 5, which consists of the following components:

$M_{1\text{-}4}$	APT5040 (Advanced Power Technology);
$D_{1\text{-}4}$	MOSFET body diode;
$C_{1\text{-}4}$	MOSFET intrinsic capacitor, equal to 465 pF for $V_{DS} = 300$ V;
$D_{c1\text{-}2}$	MUR 440 (Motorola);
$D_{r1\text{-}4}$	MUR 1540 (Motorola);
D_s	MR 854 (Motorola);
T_r	HF transformer, on ferrite core E-65/39 (Thornton); primary: 15 turns; secondary: 10 turns, center tapped;

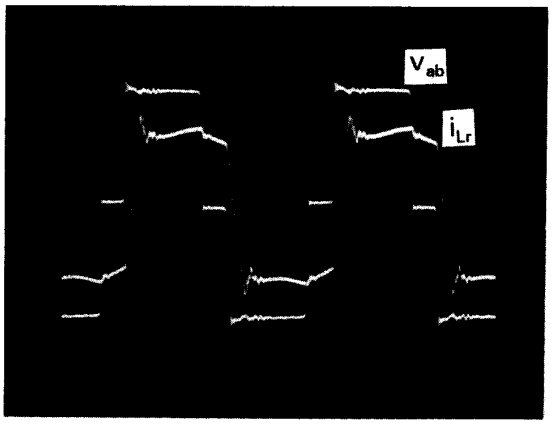


Fig. 8. Experimental waveforms. (a) v_{ab} voltage. Scales: 100 V/div., 2 μs/div. (b) i_{Lr} current. Scales: 5 A/div., 2 μs/div.

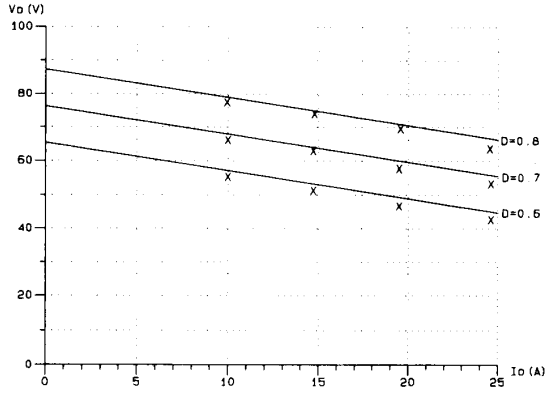


Fig. 9. Measured efficiency as a function of the load current for output voltage equal to 60 V and switching frequency equal to 100 kHz.

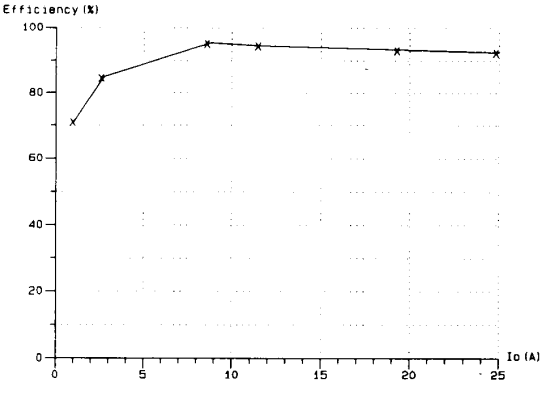


Fig. 10. Experimental output voltage V_o versus output current I_o for different values of D.

C_f	880 μF, electrolytic (Icotron);
C_b	5 μF, polypropylene (Icotron);
L_r	12 μH, 8 turns on ferrite core E-42/15 (Thornton);
L_f	61 μH, 15 turns on ferrite core E-55/21 (Thornton);

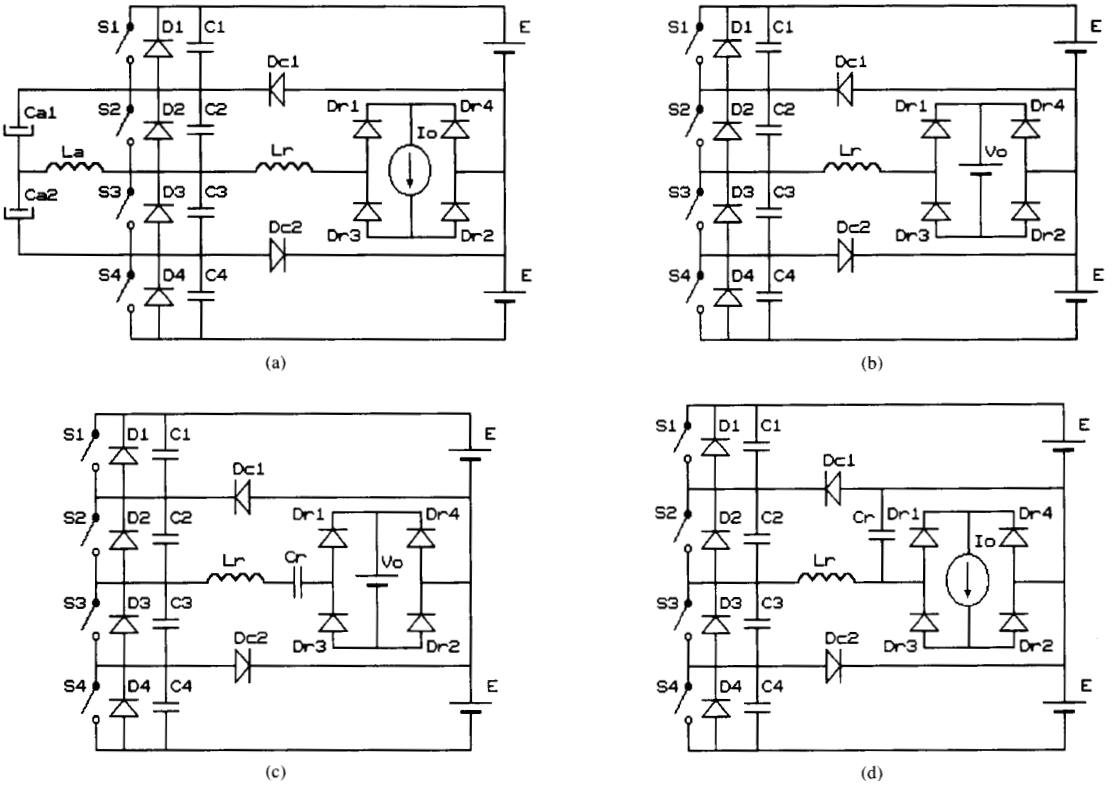


Fig. 11. A family of three-level PWM dc-to-dc converter operating at ZVS. (a) TL-ZVS-PWM converter for wide load range. (b) TL-ZVS-PWM nonresonant converter supplying a capacitor load. (c) TL-ZVS-PWM series-resonant converter. (d) TL-ZVS-PWM parallel-resonant converter.

C_s	10 nF, polypropylene (Icotron);
R_s	10 kΩ, 5 W.

The total resonance inductance is composed of the leakage transformer inductance (4 μH) and the external resonance inductance (12 μH), yielding 16 μH. Experimentally obtained waveforms for $P_o = 1500$ W, $I_o = 25$ A, $2E = 600$ V, $f_s = 100$ kHz and $D = 0.75$ are shown in Figs. 6, 7, and 8. They confirm the theoretically predicted results. Notice that the maximum voltage across the MOSFET's is 300 V, half the value of the input voltage.

The experimentally measured efficiency as a function of the load current is shown in Fig. 9, for constant output voltage equal to 60 V. Its measured value at full load (25 A) is 93%. The main source of losses are diode conduction losses, MOSFET conduction losses, and magnetic and snubber losses. MOSFET switching losses are practically zero and are neglected for the following reasons:

1) During the turn-off transition the load current flows through the intrinsic capacitor which works as a lossless snubber. The corresponding losses, besides being small, are difficult to be calculated.

2) The turn-on switching losses caused by the discharge of the intrinsic capacitor are equal to zero whenever $I_0 \geq I_{\min}$. In the case where $I_o < I_{\min}$, these losses are no longer equal to zero and can be easily calculated [5].

Output voltage V_o versus output current I_o, for different values of D, obtained experimentally, are shown in Fig. 10. Besides confirming the results predicted by theoretical analysis, these curves demonstrate that the TL-ZVS-PWM and FB-ZVS-PWM converters are governed by identical output characteristics.

VI. Application to Other Topologies

The basic TL-ZVS-PWM commutation cell can be applied to some other dc-to-dc converters with the same commutation and modulation mechanism.

In principle, there is no reason why this technique could not be applied to all full-bridge pulsewidth modulated zero-voltage-switching converters, such as clamped mode series resonant converters operating above the resonant frequency, parallel converters, series-parallel converters, etc. Some of the abovementioned topologies are shown in Fig. 11. The analysis of these circuits is presently in progress.

VII. Conclusion

This paper introduces the three-level zero-voltage-switching pulsewidth modulated (TL-ZVS-PWM) dc-to-dc converter, which is destined to be used in the design of high input voltage switching mode power supply.

Following the theoretical studies, a prototype has been designed and fabricated, rated at 1.5 kW, 100 kHz, and having an input voltage equal to 600 V. The measured efficiency at full load was 93%.

It has also been demonstrated that from the commutation standpoint the TL-ZVS-PWM dc-to-dc converter behaves like the FB-ZVS-PWM one, having identical output characteristics as well.

In designing high input voltage SMPS, there are cases in which the FB-ZVS-PWM converter cannot be used due to the unavailability of high-voltage switches. The TL-ZVS-PWM converter represents a possible alternative in these cases, as it subjects the switches to half of the input voltage.

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José Renes Pinheiro was born in Santa Maria, Rio Grande do Sul, Brazil, on September 30, 1958. He received the B.S. in electrical engineering from the Federal University of Santa Maria in 1981. In 1984 he received the M.S. degree in electrical engineering from the Federal University of Santa Catarina.

Since 1985 he has been an Assistant Professor at Federal University of Santa Maria. He is currently a Ph.D. candidate at the Federal University of Santa Catarina, Brazil, and he is been supervised by Professor Ivo Barbi. His research interests include modeling, control, analysis, design and applications of high-frequency converters, mainly those operating at constant frequency.

Ivo Barbi (SM'90) was born in 1949 in Gaspar, Santa Catarina, Brazil. He received the B.S. and M.S. degrees in electrical engineering from the Universidade Federal de Santa Catarina, Florianópolis, Brazil, in 1973 and 1976, respectively, and the Ph.D. degree from the Institut National Polytechnique de Toulouse, France, in 1979.

In 1979 he founded the Power Electronics Research Group and the Power Electronics Laboratory of the Universidade Federal de Santa Catarina, where he is presently Professor of Power Electronics and head of the Power Electronics Research Group. In 1990 he founded the Brazilian Power Electronics Society.

He was the Technical Program Chairman of the 1991 Brazilian Power Electronics Conference. He has developed extensive cooperation with the industry and supervised over 40 M.S. and four Ph.D. dissertations. His research interest include modeling, analysis, design, and application of high-frequency converters, power supplies and power factor correction.