The Three-Level ZVS-PWM DC-to-DC Converter
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Abstract—A new high frequency dc-to-dc power converter for high voltage and high power is introduced in this paper, which features zero-voltage-switching, operation at constant frequency, regulation by pulsewidth modulation, and low rms current stress upon power switches. Its greatest attribute, in comparison with the full-bridge (FB-ZVS-PWM) converter, is that the voltage across the switches is half of the input voltage. This property is achieved due to the employment of a three-level leg in place of the conventional two-switch leg. Operation, analysis, design procedure and example, and simulation are presented. A prototype operating at 100 kHz, rated at 600 V input voltage, and 1.5 kW output power and 25 A output current has been fabricated and successfully tested in the laboratory.

NOMENCLATURE

- $C_{1-4}$: MOSFET intrinsic capacitance.
- $C_{b}$: Auxiliary commutation capacitance.
- $C_{f}$: Blocking dc capacitance.
- $C_{r}$: Filter capacitance.
- $C_{d}$: Resonant capacitance.
- $D$: Snubber capacitance.
- $D_{1-4}$: Control duty-cycle.
- $D_{1-2}$: MOSFET intrinsic diode.
- $D_{eff}$: Reduction of the duty-cycle.
- $D_{d}$: Clamping diode.
- $E$: Effective duty-cycle.
- $f_{o}$: Rectifier diode.
- $f$: Input source.
- $I_{dr}$: MOSFET drain current.
- $I_{dr}$: Resonant inductor current.
- $I_{min}$: Minimum load current.
- $I_{o}$: Load current.
- $L_{a}$: Auxiliary commutation inductor.
- $L_{f}$: Filter inductance.
- $L_{r}$: Resonant inductance.
- $M_{1-4}$: Power MOSFET.
- $n$: Transformer turn ratio.
- $P_{o}$: Output power.
- $R_{o}$: Load resistance.
- $R_{s}$: Snubber resistance.
- $S_{1-4}$: Semiconductor switch.
- $T$: Time.
- $T_{r}$: Transformer.
- $T_{s}$: Switching period.

Voltage between the points $a$ and $b$.
MOSFET intrinsic capacitance.
Voltage.
Output voltage.
Drain-source voltage.
Resonant voltage.
Resonant characteristic impedance.

I. INTRODUCTION

Engineers involved in the design of high frequency switching mode power supplies for high power application presently recognize that one of the best power converter topologies is the FB-ZVS-PWM converter [1], [2]. This is because it possesses the basic desirable characteristics of both the hard switching PWM converters and the soft switching ones, while avoiding their major drawbacks, such as commutation losses in the former, and variable switching frequency and high conduction losses in the second group. However, the power switches of the FB-ZVS-PWM converter are subjected to the maximum input voltage level. In the cases where the input voltage is high, it may not be possible to get adequate switches. In order to reduce the voltage stress of the switches, this paper proposes the three-level (TL-ZVS-PWM) dc-to-dc converter. As is demonstrated hereafter, this new topology operates like the FB-ZVS-PWM converter from the commutation standpoint, having identical output characteristics and power transfer control. In addition, the maximum voltage across the switches is half the value of the input voltage. The TL-ZVS-PWM converter offers a clear advantage over the FB-ZVS-PWM converter since switch voltage stress is reduced to one-half the input voltage. Lower switch stress offers the advantages of reduced power switching device cost and higher reliability due to lower switching stress. This technique was inspired by the hard switched three-level inverter [3].

II. THE THREE-LEVEL ZERO-VOLTAGE-SWITCHING PULSEWIDTH-MODULATED DC-TO-DC CONVERTER (TL-ZVS-PWM)

A. Circuit Description

The TL-ZVS-PWM converter proposed in this paper is shown in Fig. 1. The main commutation leg is formed by $M_{1}, M_{2}, M_{3},$ and $M_{4}, D_{1}, D_{2}, D_{3}$ and $D_{4}$ are the MOSFET's body diodes, while $C_{1}, C_{2}, C_{3},$ and $C_{4}$ are the MOSFET's intrinsic capacitors, employed to perform the commutation at zero voltage. No external commutation capacitors are needed. $L_{r}$ is the commutation inductor, composed of an external inductor plus the leakage inductor of the transformer. $T_{r}$ is the isolation transformer. The output stage is formed by rectifiers.
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\[ D_{c1}, D_{c2}, D_{c3}, \text{ and } D_{c4} \] and the output filter composed of \( L_f \) and \( C_f \). \( D_{c1} \) and \( D_{c2} \) constitute the clamping diodes. \( R_o \) represents the load resistance.

**B. Principle of Operation**

To simplify the analysis, the following assumptions are made: 1) the circuit operates in a steady-state. 2) All power semiconductors are ideal. 3) The MOSFET’s intrinsic capacitances are constant and incorporate all the transformer’s parasitic capacitances. 4) The output filter inductance is sufficiently large to be approximated by a current source with a value equal to load current \( I_L \). 5) The transformer magnetizing current is neglected.

Fig. 2 shows the seven topological stages for a half-period of operation. The main waveforms are represented in Fig. 3. The operation is described as follows:

**First Stage** \((t_0, t_1)\): During this stage the load current flows through \( M_1, M_2, D_{c1}, \text{ and } D_{c2} \). \( v_{C1} = v_{C2} = 0, v_{C3} = V_{C3} = E \) and \( i_{L_L} = I_L \) [Fig. 2(a)].

**Second Stage** \((t_1, t_2)\): This stage begins at time \( t_1 \), when \( M_1 \) is gated off and turns off in a soft-switching manner. Voltage \( v_{C3} \) increases from zero to \( E \), while \( v_{C2} \) decreases from \( 2E \) to \( E \). This stage ends at instant \( t_2 \), when \( D_{c1} \) is directly polarized and starts conducting. Through output rectifiers \( D_{c1} \) and \( D_{c2} \) flows the load current [Fig. 2(b)].

**Third Stage** \((t_2, t_3)\): This is a free-wheeling stage, during which the load current flows through \( D_{c1}, M_2, L_f, \text{ and the output rectifiers } (D_{c1} \text{ and } D_{c2}) \) [Fig. 2(c)].

**Fourth Stage** \((t_3, t_4)\): At moment \( t_3 \), \( M_2 \) is gated off and turns off in a soft-switching manner. Capacitor voltage \( v_{C2} \) increases up to \( E \) while \( v_{C3} \) decreases towards zero. This stage ends when \( v_{C2} \) reaches \( E \). All output rectifiers are conducting, therefore short-circuiting the output stage [Fig. 2(d)].

**Fifth Stage** \((t_4, t_5)\): During this stage, current \( i_{L_L} \) flows through diodes \( D_{c1} \) and \( D_{c2} \) and decreases linearly. During the conduction of \( D_{c3} \) and \( D_{c4} \), switches \( M_3 \) and \( M_4 \) are gated on at zero-voltage and zero-current [Fig. 2(e)].

**Sixth Stage** \((t_5, t_6)\): When \( i_{L_L} \) reaches zero, \( D_3 \) and \( D_4 \) turn off and \( M_3 \) and \( M_4 \) start conducting. Current \( i_{L_L} \) increases linearly in the reverse direction [Fig. 2(f)].

**Seventh Stage** \((t_6, t_7)\): This stage begins when \( i_{L_L} \) reaches load current \( I_L \). Output rectifiers \( D_{c1} \) and \( D_{c2} \) turn off naturally, and only through \( D_{c3} \) and \( D_{c4} \) does the load current flow [Fig. 2(g)].

**III. THEORETICAL ANALYSIS**

**A. Output Characteristics**

According to the waveforms shown in Fig. 3, and considering that the commutation time is much smaller than the switching period, the average output voltage is given by

\[
V_o = \frac{2(0 - t_0)}{T_s}.
\]
During time interval \((0, t_0)\), current \(i_{Lr}\) is represented by

\[
i_{Lr} = -I_0 + \frac{E}{L_r} t.
\]

At time \(t = t_0\), \(i_{Lr} = I_0\). Thus

\[
t_0 = \frac{2L_r I_0}{E}.
\]

By substituting (3) into (1) we obtain

\[
V_o = E \left(\frac{2t_1}{T_o} - \frac{4f_s L_r I_0}{E}\right).
\]

Let us define the control duty-cycle as

\[
D = \frac{2t_1}{T_o}
\]

and the reduction of the duty-cycle is given by

\[
\Delta = \frac{4f_s L_r I_0}{E}.
\]

The effective duty-cycle is defined as

\[
D_{eff} = \frac{V_o}{E}.
\]

Hence,

\[
\frac{V_o}{E} = D - \frac{4f_s L_r I_0}{E}
\]

or

\[
D_{eff} = D - \Delta.
\]

Equation (8) represents the dc voltage-conversion-ratio of the TL-ZVS-PWM converter. Notice that the larger \(L_r\) is, the larger also is the reduction of the output voltage caused by the reactive voltage drop.

In order to ensure the soft-commutation, \(I > I_{min}\).

According to (6) and (16), the wider the load range with ZVS is, which implies smaller minimum load current \(I_{min}\), the higher is the reactive voltage drop across commutation.

**B. Commutation Analysis**

During time interval \((t_1, t_2)\), voltages \(v_{C1}\) and \((v_{C3} + v_{C4})\) are represented as follows:

\[
v_{C1} = \frac{I_0 t}{1.5C}
\]

and

\[
v_{C3} + v_{C4} = 2E - \frac{I_0 t}{1.5C}
\]

where \(C\) represents the intrinsic capacitance of each MOSFET.

The second and more critical commutation takes place during time interval \((t_3, t_4)\) where \(v_{C2}\) increases from zero up to \(E\) and \((v_{C3} + v_{C4})\) reduces from \(E\) to zero. If \(v_{C2}\) does not reach \(E\), the soft-commutation is not achieved. The voltage across \(C_2\) is governed by

\[
v_{C2} = \sqrt{\frac{L_r}{1.5C}} I_o \sin (\omega_r t)
\]

where

\[
\omega_r = \sqrt{\frac{1}{1.5L_r C}}
\]

and

\[
Z_r = \sqrt{\frac{L_r}{1.5C}}
\]

At \(\omega_r t = \pi/2\), capacitor voltage \(v_{C2}\) is

\[
v_{C2} = I_o \sqrt{\frac{L_r}{1.5C}}
\]

and letting \(I_o = I_{min}\) and \(v_{C2} = E\), then

\[
I_{min} = E \sqrt{\frac{1.5C}{L_r}}.
\]
inductor $L_r$. In other words, a wide load range yields a large amount of the circulating energy, increasing the conduction losses. However, this problem is not a characteristic of the TL-ZVS-PWM converter, since it is also encountered in other ZVS converters.

A good design involves sacrificing the soft-commutation at low load, where the conduction losses are low, to obtain a high efficiency at full-load.

IV. SIMPLIFIED DESIGN PROCEDURE AND EXAMPLE

The design of the TL-ZVS-PWM converter is similar to that of the FB-ZVS-PWM converter, as it is presented in [2] and [4], whereas a simplified approach is presented hereafter. The main purpose of this section is to use the deduced equations to define the components for simulation and fabrication of a prototype.

a) Input data

- $P_o = 1.5$ kW (rated output power)
- $E = 300$ V (half input voltage)
- $V_o = 60$ V (output voltage)
- $f_s = 100$ kHz (switching frequency)
- $I_o = 25$ A (rated output current).

b) The effective duty-cycle $D_{eff}$ is chosen to be 0.6 and $L_r$ is chosen in such a way that it causes 20% of reduction in duty-cycle $D$. Thus, from (9):

$$D = 0.6 + 0.2D$$

hence

$$D = 0.75.$$ 

Isolating $L_r$ from (6), we obtain

$$L_r = \frac{0.2DnV_o}{4f_sI_o}$$

where

$$\frac{nV_o}{E} = 0.6.$$ 

Then

$$L_r = 13.5 \mu H.$$ 

A value equal to 16.0 $\mu H$ was adopted. As the measured leakage transformer inductance was 4 $\mu H$, the value of the external inductance is equal to 12 $\mu H$.

c) The chosen MOSFET (APT5040) to meet voltage and current requirements has an intrinsic capacitance equal to 500 pF.

So the minimum current to ensure ZVS is

$$I_{min} = \frac{1.5C}{L_r} = 2.10 \text{ A}$$

which corresponds to 6.3 A at the load, representing 25% of the full load current.

V. EXPERIMENTAL RESULTS

Following the design outlined in the preceding section, a TL-ZVS-PWM dc-to-dc converter was implemented, with the following specifications:
output power: $P_o = 1500$ W;
output voltage: $V_o = 600$ V;
input voltage: $2E = 1000$ V;
switching frequency: $f_s = 100$ kHz.

The implemented drive and command circuits are shown in Fig. 4(a) and (b), respectively. The power stage of the converter is shown in Fig. 5, which consists of the following components:

- $M1_{1-4}$: APT5040 (Advanced Power Technology)
- $D_{1-4}$: MOSFET body diode
- $C_{1-4}$: MOSFET intrinsic capacitor, equal to 465 pF for $V_{DS} = 300$ V
- $D_{r_{1-2}}$: MUR 440 (Motorola)
- $D_{r_{1-4}}$: MUR 1540 (Motorola)
- $D_r$: MR 854 (Motorola)
- $T_r$: HF transformer, on ferrite core E-65/39 (Thornton): primary: 15 turns; secondary: 10 turns, center tapped

$C_f$: 880 μF, electrolytic (lecron);
$C_r$: 5 μF, polypropylene (lecron);
$L_r$: 12 μH, 8 turns on ferrite core E-42/15 (Thornton);
$L_f$: 61 μH, 15 turns on ferrite core E-55/21 (Thornton);
The total resonance inductance is composed of the leakage transformer inductance ($4 \mu H$) and the external resonance inductance ($12 \mu H$), yielding $16 \mu H$. Experimentally obtained waveforms for $P_o = 1500 W$, $I_o = 25 A$, $2E = 600 V$, $f_s = 100 kHz$ and $D = 0.75$ are shown in Figs. 6, 7, and 8. They confirm the theoretically predicted results. Notice that the maximum voltage across the MOSFET’s is $300 V$, half the value of the input voltage.

The experimentally measured efficiency as a function of the load current is shown in Fig. 9, for constant output voltage equal to $60 V$. Its measured value at full load ($25 A$) is $93\%$. The main source of losses are diode conduction losses, MOSFET conduction losses, and magnetic and snubber losses. MOSFET switching losses are practically zero and are neglected for the following reasons:

1) During the turn-off transition the load current flows through the intrinsic capacitor which works as a lossless snubber. The corresponding losses, besides being small, are difficult to be calculated.

2) The turn-on switching losses caused by the discharge of the intrinsic capacitor are equal to zero whenever $I_o \geq I_{min}$. In the case where $I_o < I_{min}$, these losses are no longer equal to zero and can be easily calculated [5].

Output voltage $V_o$ versus output current $I_o$, for different values of $D$, obtained experimentally, are shown in Fig. 10. Besides confirming the results predicted by theoretical analysis, these curves demonstrate that the TL-ZVS-PWM and FB-ZVS-PWM converters are governed by identical output characteristics.

VI. APPLICATION TO OTHER TOPOLOGIES

The basic TL-ZVS-PWM commutation cell can be applied to some other dc-to-dc converters with the same commutation and modulation mechanism.

In principle, there is no reason why this technique could not be applied to all full-bridge pulsewidth modulated zero-voltage-switching converters, such as clamped mode series resonant converters operating above the resonant frequency, parallel converters, series-parallel converters, etc. Some of the abovementioned topologies are shown in Fig. 11. The analysis of these circuits is presently in progress.

VII. CONCLUSION

This paper introduces the three-level zero-voltage-switching pulsewidth modulated (TL-ZVS-PWM) dc-to-dc converter, which is destined to be used in the design of high input voltage switching mode power supply.
Following the theoretical studies, a prototype has been designed and fabricated, rated at 1.5 kW, 100 kHz, and having an input voltage equal to 600 V. The measured efficiency at full load was 93%.

It has also been demonstrated that from the commutation standpoint the TL-ZVS-PWM dc-to-dc converter behaves like the FB-ZVS-PWM one, having identical output characteristics as well.

In designing high input voltage SMPS, there are cases in which the FB-ZVS-PWM converter cannot be used due to the unavailability of high-voltage switches. The TL-ZVS-PWM converter represents a possible alternative in these cases, as it subjects the switches to half of the input voltage.

REFERENCES


