

Constant Frequency PWM Capacitor Voltage-Clamped Series Resonant Power Supply

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Abstract—This paper proposes a capacitor voltage clamped series resonant converter, regulated at constant frequency by pulse-width modulation (PWM-CVC-SRC), suitable for an off-line isolated multiple output power supply. The principle of operation, theoretical analysis, simulation, design procedure, and design example are provided, along with experimental results. The validity of the theoretical analysis and the main properties of the proposed converter were demonstrated in the laboratory, with the design and construction of an isolated power supply rated at 12 V/16 A, operating at 100 kHz. The proposed technique propitiates a significant reduction in the rms value of the current through transistors, besides the reduction of the size of the output filter capacitor and dynamic response improvements.

I. INTRODUCTION

THE series resonant converter, whose basis topologies for off-line power supplies are shown in Fig. 1, is suitable for high-frequency operation because of low switching losses. However, the energy exchange between the source and the resonant circuit raises the rms value of the current through the semiconductors and the conduction losses, causing a reduction in efficiency. To avoid these difficulties, the capacitor voltage clamped mode series resonant converter (CVC-SRC) has been proposed [1]–[3], which features low switching losses, low conduction losses, and clamped voltage across the resonant capacitor. These converters are derived from the basic topologies shown in Fig. 1, by the addition of clamping diodes, as illustrated in Fig. 2. Despite these considerable improvements, with respect to the conventional series resonant converter, the most undesirable property, i.e., regulation by frequency modulation, is not eliminated. It can be demonstrated that, in fixed values of input and output voltage, the output power is given by

$$P_0 = K_1 \cdot f_s. \quad (1)$$

This means that a power range from 10% to 100% causes an equivalent switching frequency variation from 10% to 100%, an unacceptable range for most applications, due to the increase in size of transformers, inductors, and capacitors.

This paper proposes, analyzes, and designs a clamped voltage capacitor series resonant converter regulated at constant frequency by PWM (PWM-CVC-SRC), to overcome the difficulties of the clamped voltage capacitor series resonant

converter, regulated by variation of resonant frequency (FM-CVC-SRC).

II. THE PROPOSED CIRCUIT AND PRINCIPLE OF OPERATION

The power stage diagram of the proposed converter, shown in Fig. 3, is described as follows:

T_1, T_2 = Main transistors

T_3, T_4 = Auxiliary transistors

L_r, C_r = Resonant components

V_s = Input voltage

E = Output voltage

D_1, D_2 = Clamping diodes

D_3, D_4, D_5, D_6 = Output rectifiers

The stages of operation (Fig. 4), are described as follows:

Stage I (t_0, t_1): At instant t_0 , the resonant capacitor voltage is negative, and transistor T_1 is turned on. The voltage V_{C_r} and current i_{L_r} change in a resonant way, until the instant t_1 , when V_{C_r} becomes equal to zero.

Stage II (t_1, t_2): At the instant t_1 , switches T_3 and T_4 are turned on at zero voltage, and stage II begins. During this stage, the current i_{L_r} rises linearly. The duration of this stage, $\Delta t = t_2 - t_1$, controls the power transferred to the load.

Stage III (t_2, t_3): At the instant t_2 , switches T_3 and T_4 are turned off and V_{C_r} and i_{L_r} change in a resonant fashion. At instant t_3 , V_{C_r} reaches the voltage $V_s/2$. Diode D_1 starts to conduct the current i_{L_r} , and V_{C_r} is clamped at $V_s/2$.

Stage IV (t_3, t_4): During this stage, the current i_{L_r} free-wheels through diode D_1 . At instant t_4 , i_{L_r} reaches zero, and this stage is concluded.

A dead time is introduced between the first and second half period of operation to prevent a short circuit of the converter leg, formed by T_1 and T_2 . The main waveforms, along with the gate signals, are shown in Fig. 5.

III. RELEVANT ANALYSIS RESULTS

The relevant expressions obtained by theoretical analysis are as follows:

$$\bar{I}_0 = \frac{2}{\pi} \cdot \frac{1}{q} \cdot \frac{f_s}{f_0} + \frac{(1-q)}{2q} \cdot \frac{\pi D^2}{f_s/f_0} + \frac{\sqrt{3-2q}}{q} \cdot D \quad (2)$$

$$\bar{I}_{rms}^2 = \frac{1}{2\pi} \cdot \frac{f_s}{f_0} \cdot \left(\frac{1}{2} \cdot (2-q)^2 \cdot \cos^{-1} \frac{1-q}{2-q} \right)$$

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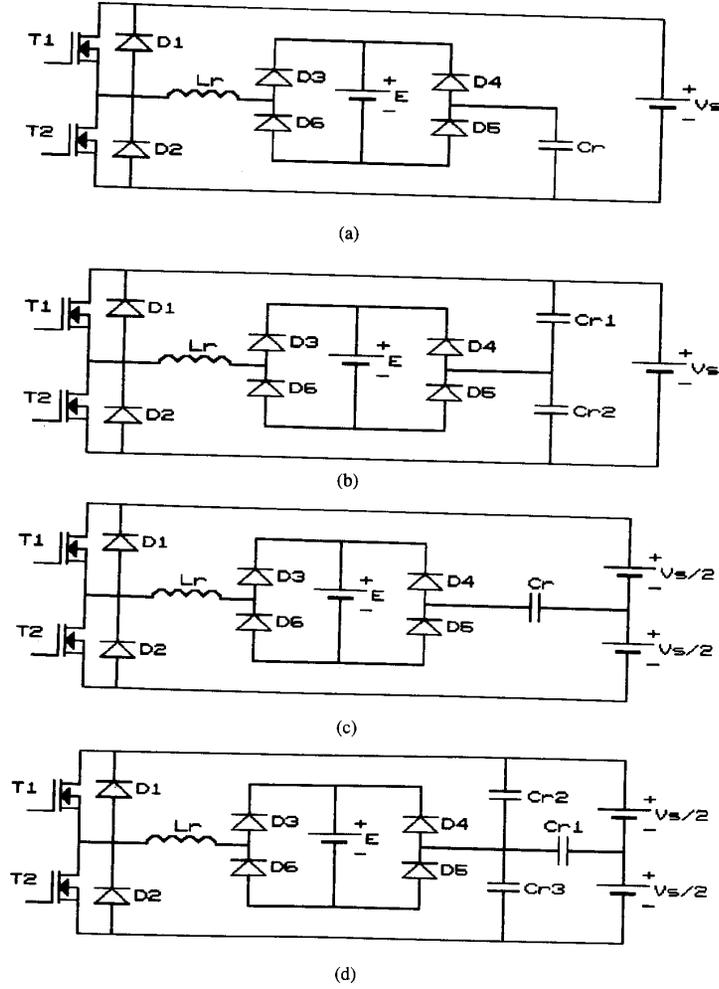


Fig. 1. Topological variations of the SRC for off-line power supplies.

$$\begin{aligned}
 & -\frac{1-q}{2} \cdot \sqrt{3-2q} + \frac{1}{3q} \cdot \bar{I}_{L3}^3 \\
 & + \frac{1}{3(1-q)} \cdot (\bar{I}_{L2}^3 - \bar{I}_{L1}^3) \\
 & + \frac{\bar{R}^2}{2} \cdot \left\{ \pi - \cos^{-1} \left[\frac{q \cdot (1-q) - \bar{I}_{L3} \cdot \bar{I}_{L2}}{\bar{R}^2} \right] \right\} \\
 & + \frac{1}{2} [q(\bar{I}_{L3} - \bar{I}_{L2}) + \bar{I}_{L2}]
 \end{aligned}$$

$$\bar{I}_{av} = \frac{1}{2\pi} \cdot \frac{f_s}{f_0} \cdot \frac{1}{2q} \cdot \bar{I}_{L3}^3$$

$$\bar{I}_{L1} = \sqrt{3-2q}$$

$$\bar{I}_{L2} = \bar{I}_{L1} + (1-q) \cdot \frac{\pi D}{f_s/f_0}$$

$$\bar{I}_{L3} = \sqrt{(1-q) \left[4 + 2 \cdot \sqrt{3-2q} \cdot \frac{\pi D}{f_s/f_0} + (1-q) \cdot \left(\frac{\pi D}{f_s/f_0} \right)^2 \right]} \quad (7)$$

$$\bar{R} = \sqrt{(2-q)^2 + 2 \cdot \sqrt{3-2q} \cdot (1-q) \cdot \frac{\pi D}{f_s/f_0} + (1-q)^2 \cdot \left(\frac{\pi D}{f_s/f_0} \right)^2} \quad (8)$$

(4) where

- (5) \bar{I}_0 = Normalized output current
- q = DC voltage conversion ratio
- (6) \bar{I}_{rms} = Normalized rms current through T_1 and T_2
- \bar{I}_{av} = Normalized average current through D_1 and D_2

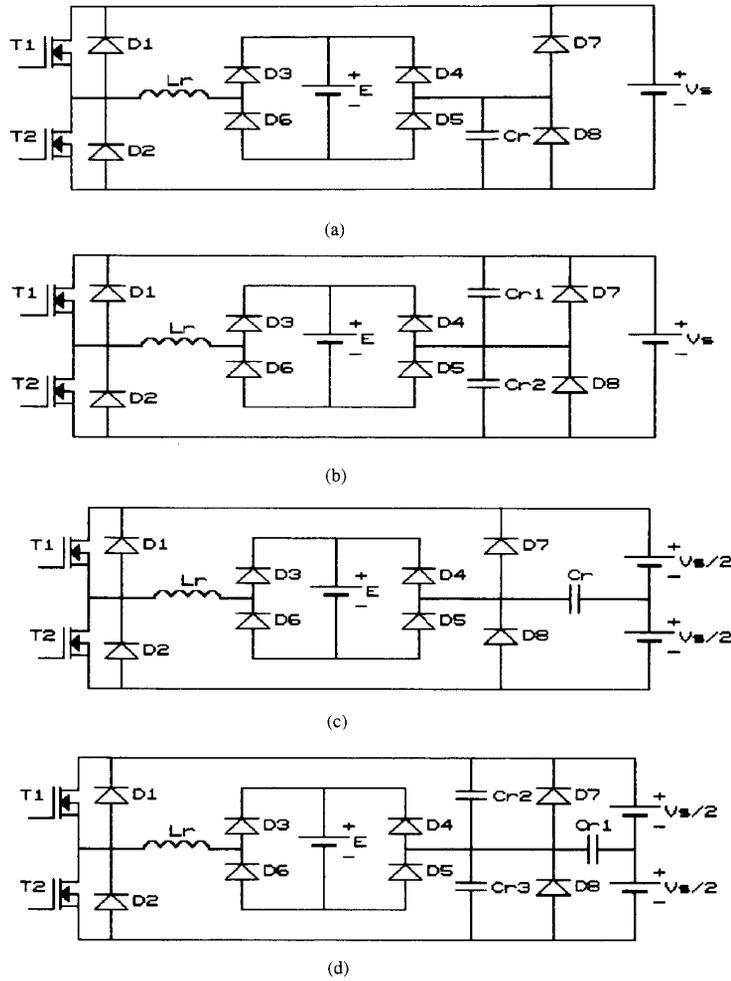


Fig. 2. Topological variations of the capacitor voltage clamped series resonant converter (CVC-SRC).

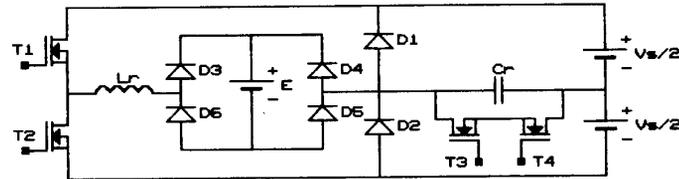


Fig. 3. Power stage diagram of the proposed PWM-CVC-SRC.

where

$$q = \frac{E}{V_s/2} \tag{9}$$

$$\bar{I} = \frac{Z_0 \cdot I}{V_s/2} \tag{10}$$

$$D = \frac{2\Delta t}{T_s} \tag{11}$$

where

- D = Duty cycle
- Z_0 = Characteristic impedance.

Theoretical output characteristics, represented by (2), are shown in Fig. 6 for different values of f_s/f_0 .

Equation (3), which represents the rms current through MOSFET's, is represented in Fig. 7, compared to the corresponding values of the FM converter. As can be noted, the PWM converter provides a significant reduction in the conduction losses of the MOSFET's. The curves of Fig. 7 were obtained for $Z_0 = 28.8 \Omega$ for the PWM converter, and $Z_0 = 9.6 \Omega$ for the FM converter, with $q = 0.75$ for both converters.

IV. DESIGN PROCEDURE AND EXAMPLE

A design procedure of the investigated converter, along with a practical example, is presented as follows:

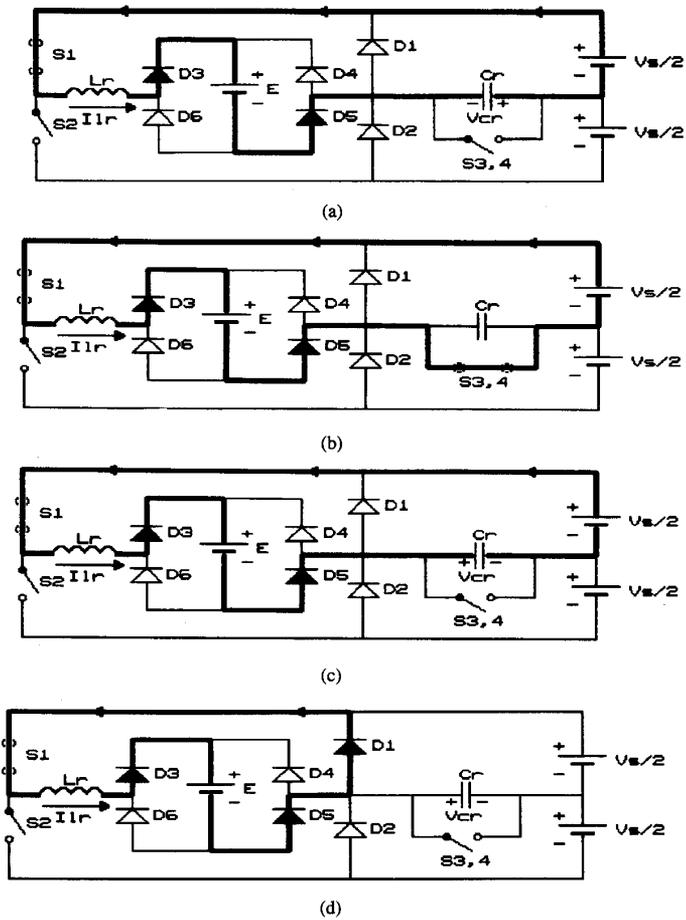


Fig. 4. Stages of operation of the PWM-CVC-SRC. (a) t_0, t_1 . (b) t_1, t_2 . (c) t_2, t_3 . (d) t_3, t_4 .

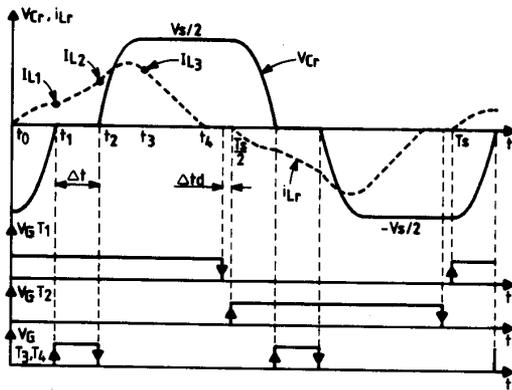


Fig. 5. Main waveforms and gate drive signal.

A. Design Procedure

- 1) Define the input data, as follows.
 - Maximum, minimum, and rated value of the input voltage $V_s/2$
 - Output voltage V_0
 - Maximum, minimum, and rated output power P_0
 - Switching frequency f_s

2) Select the ratio f_s/f_0 .

According to the theoretical output characteristics, the output power range depends on the ratio f_s/f_0 . For a wide load current range, a small relation f_s/f_0 is required. A suitable value is $f_s/f_0 = 0.15$.

3) Utilizing the output characteristics, for the selected value of f_s/f_0 , and taking into account the load current range, the value of q is selected. Thus $E = q \cdot (V_s/2)$. The transformer turns ratio is given by $n = (E/V_0)$.

4) Select the duty cycle for rated output current. Consequently, the value of \bar{I}_0 is defined by the output characteristics.

5) Calculate the value of L_r and C_r , with the employment of the expressions as follows.

$$f_0 = \frac{1}{2\pi \cdot \sqrt{L_r \cdot C_r}}$$

$$Z_0 = \sqrt{\frac{L_r}{C_r}}$$

$$\bar{I}_0 = \frac{Z_0 \cdot I_{0rated}}{V_{srated}/2}$$

$$I_0 = P_0/V_0$$

6) Calculate the values of the maximum and minimum duty

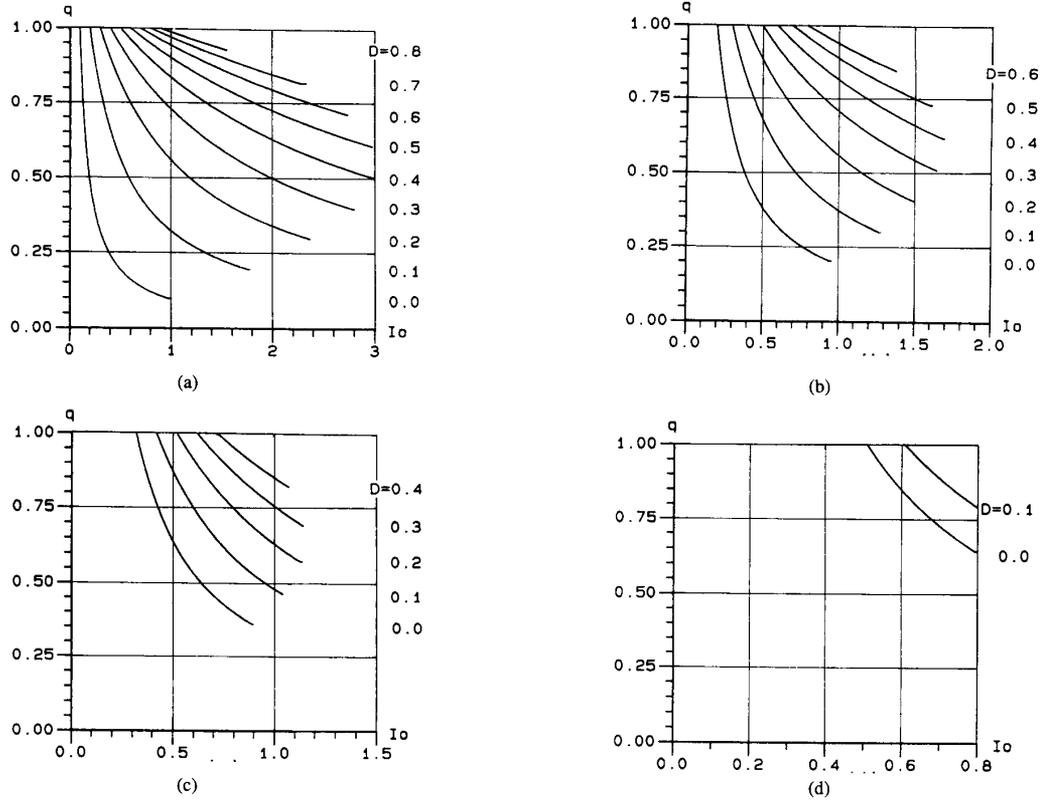


Fig. 6. Output characteristics of the PWM-CVC-SRC for f_s/f_0 . (a) 0.15. (b) 0.3. (c) 0.5. (d) 0.8.

cycle, D_{\max} and D_{\min} , as follows.

$$\begin{aligned} q_{\max} &= \frac{E}{V_{s_{\min}}/2} & q_{\min} &= \frac{E}{V_{s_{\max}}/2} \\ \bar{P}_{0_{\max}} &= \frac{Z_0 \cdot P_{0_{\max}}}{(V_s/2)^2} & \bar{P}_{0_{\min}} &= \frac{Z_0 \cdot P_{0_{\min}}}{(V_{s_{\max}}/2)^2} \\ \bar{I}_{0_{\max}} &= \frac{\bar{P}_{0_{\max}}}{q_{\min}} & \bar{I}_{0_{\min}} &= \frac{\bar{P}_{0_{\min}}}{q_{\max}} \end{aligned}$$

The pair $\bar{I}_{0_{\max}}$ and q_{\min} define the value of D_{\max} , whereas $\bar{I}_{0_{\min}}$ and q_{\max} define the value of D_{\min} from the output characteristics.

B. Design Example

1) Input Data

$$\begin{aligned} V_{s_{\max}}/2 &= 90 \text{ V} & P_{0_{\max}} &= 200 \text{ W} \\ V_{s_{\min}}/2 &= 70 \text{ V} & P_{0_{\min}} &= 50 \text{ W} \\ V_{s_{\text{rated}}}/2 &= 80 \text{ V} & P_{0_{\text{rated}}} &= 150 \text{ W} \\ V_0 &= 12 \text{ V} & f_s &= 100 \text{ kHz} \end{aligned}$$

2) $f_s/f_0 = 0.15$

$$f_0 = \frac{100 \text{ kHz}}{0.15} = 667 \text{ kHz}$$

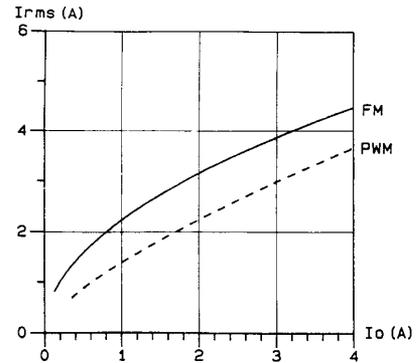


Fig. 7. MOSFET's rms current as function of the output current.

3) $q = 0.75$

$$\begin{aligned} E &= q \cdot \frac{V_{s_{\text{rated}}}}{2} = 0.75 \cdot 80 = 60 \text{ V} \\ n &= \frac{E}{V} = 5 \end{aligned}$$

4) $D_{\text{rated}} = 0.3$

$$\bar{I}_0 = 0.9$$

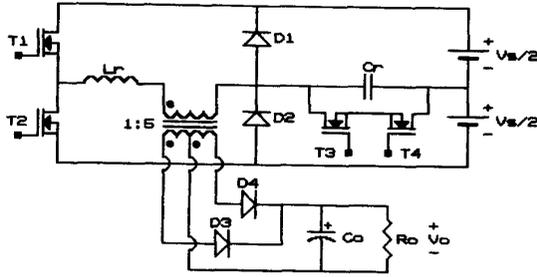
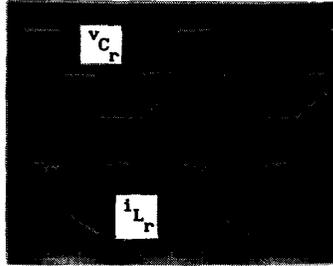
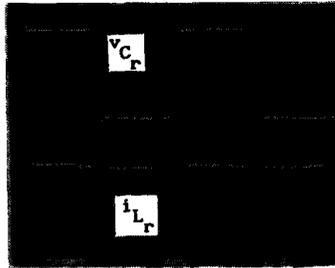


Fig. 8. Power stage diagram of the implemented power supply.



(a)



(b)

 Fig. 9. Capacitor voltage, v_{C_r} and inductor current i_{L_r} of the PWM-CVC-SRC for (a) $D = 0.4$ and (b) $D = 0.0$. Upper traces: $v_{C_r} = (50 \text{ V/div})$. Lower traces: $i_{L_r} = (2 \text{ A/div})$. Time scale: $2 \mu\text{s/div}$.

$$5) I_{0,\text{rated}} = P_{0,\text{rated}}/60 = 150/60 = 2.5 \text{ A}$$

$I_{0,\text{rated}}$ = output current reflected to the primary side of the transformer

$$Z_0 = \frac{\bar{I}_0}{I_{0,\text{rated}}} \times \frac{V_{s,\text{rated}}}{2} = 28.8 \Omega$$

$$\frac{L_r}{C_r} = Z_0^2 = 829.44$$

$$L_r \times C_r = \frac{1}{(2\pi \times f_0)^2} = 5.69 \times 10^{-14}$$

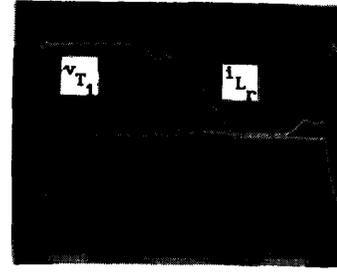
$$L_r = 6.9 \mu\text{H}$$

$$C_r = 8.3 \text{ nF.}$$

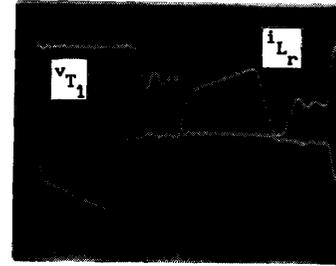
Choosing a commercial value for C_r , we obtain

$$C_r = 10 \text{ nF} \quad \text{and} \quad L_r = 7.4 \mu\text{H}$$

$$f_0 = 585 \text{ kHz.}$$



(a)



(b)

 Fig. 10. Transistor T_1 , voltage v_{T_1} , and inductor current i_{L_r} for (a) $D = 0.4$ and (b) $D = 0.0$. Scales: v_{T_1} (50 V/div); i_{L_r} (2 A/div); time ($2 \mu\text{s/div}$).

Thus, $f_s/f_0 = 0.17$ and $Z_0 = 27.2 \Omega$

$$q_{\text{max}} = \frac{E}{V_{s,\text{min}}/2} = \frac{60}{70} = 0.86$$

$$q_{\text{min}} = \frac{E}{V_{s,\text{max}}/2} = \frac{60}{90} = 0.67$$

$$\bar{P}_{0,\text{max}} = \frac{Z_0 \times P_{0,\text{max}}}{(V_{s,\text{min}}/2)^2} = \frac{27.2 \times 200}{70^2} = 1.11$$

$$\bar{P}_{0,\text{min}} = \frac{Z_0 \times P_{0,\text{min}}}{(V_{s,\text{max}}/2)^2} = \frac{27.2 \times 50}{90^2} = 0.17$$

$$\bar{I}_{0,\text{max}} = \frac{\bar{P}_{0,\text{max}}}{q_{\text{min}}} = \frac{1.11}{0.67} = 1.66$$

$$\bar{I}_{0,\text{min}} = \frac{\bar{P}_{0,\text{min}}}{q_{\text{max}}} = \frac{0.17}{0.86} = 0.20.$$

As a consequence, from the output characteristics,

$$D_{\text{max}} = 0.4 \quad \text{and} \quad D_{\text{min}} = 0.0.$$

V. EXPERIMENTAL RESULTS

The power stage diagram of the implemented power supply is shown in Fig. 8, whose specifications and parameters are as follows:

$$V_s = 160 \text{ V}$$

$$V_0 = 12 \text{ V}$$

$$f_s = 100 \text{ kHz}$$

$$I_{0,\text{max}} = 15 \text{ A}$$

$$f_0 = 585 \text{ kHz}$$

$$P_{\text{max}} = 200 \text{ W}$$

$$L_r = 7.4 \mu\text{H}$$

$$R_0 = 0.96 \Omega$$

$$C_r = 10 \text{ nF (polypropylene)}$$

$$C_0 = 100 \mu\text{F}$$

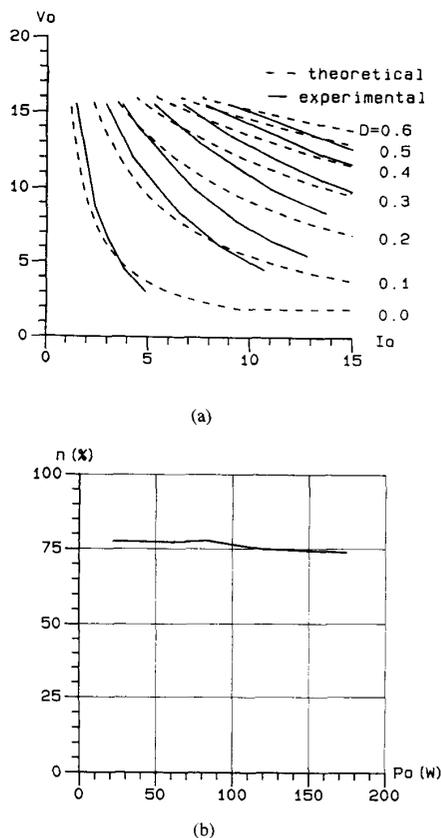


Fig. 11. (a) Experimental output characteristics. (b) Efficiency.

T_1, T_2, T_3, T_4 – IRF 740 (International Rectifier)
 D_1, D_2 – 4F2/06 (Semikron)
 D_3, D_4 – USD475 (Unitrode)
 Transformer – $N_1 = 22$ turns and
 $N_2 = 5$ turns on ferrite core E-30/7.

Experimentally obtained waveforms, shown in Figs. 9 and 10, demonstrate that the power transfer to the load is controlled by PWM, and that the commutations of the main transistors T_1 and T_2 take place under zero current. The commutations of transistors T_3 and T_4 , which occur at zero voltage, are not shown. Output characteristics and efficiency are shown in Fig. 11(a) and (b), respectively.

VI. CONCLUSION

This paper presented a clamped voltage capacitor series resonant converter, regulated at constant frequency, by PWM (PWM-CVC-SRC). From the theoretical and experimental studies accomplished, we summarize its features as follows:

- The power transfer to the load is controlled at constant frequency, as a conventional PWM converter.
- The maximum voltage across the resonant capacitor is clamped at the input voltage.

- It always operates in discontinuous current mode (DCM), contributing to reduce the switching losses even more.
- There is no energy feed back to the source, consequently the transistors conduction losses are lower than the conventional SRC.
- The rms current through the semiconductors is reduced as compared to the FM equivalent converter.
- The peak current through the output capacitor is smaller than the conventional SRC.
- The converter is suitable for isolated multiple output off-line power supply.
- It is believed that, due to the above-mentioned features, it will be appropriate for high-power applications.
- The clamping diodes and the auxiliary transistors commute at zero voltage.
- It is more appropriate for wide load range than the conventional SRC.

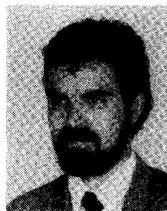
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In 1979 he founded the Power Electronics Research Group and the Power Electronics Laboratory of the Universidade Federal de Santa Catarina, where he is presently Professor of Power Electronics and head of the Power Electronics Research Group. In 1990 he founded the Brazilian Power Electronics Society. He was the Technical Program Chairman of the 1991 Brazilian Power Electronics Conference. He has developed extensive cooperation with the industry and supervised over 40 M.S. and 4 Ph.D. dissertations. Dr. Barbi's research interest include modeling, analysis, design, and application of high-frequency converters, power supplies, and power factor correction. Since January 1992, he has been Associate Editor in the power converters area, of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.