A New ZVS-PWM Unity Power Factor Rectifier with Reduced Conduction Losses

Alexandre Ferrari de Souza, *Member, IEEE,* and Ivo Barbi, *Senior Member, IEEE*

***Abstract*—This paper introduces a new single-phase high power factor rectifier, which features regulation by conventional PWM, soft commutation and instantaneous average line current control. Furthermore, thanks to the use of a single converter, instead of the conventional configuration composed of a four-diode front-end rectifier followed by a boost converter, a significant reduction in the conduction losses is achieved. A prototype rated at 1.6 kW, operating at 70 kHz, with an input ac voltage of 220 Vrms and an output voltage of 400 V_{dc} has been implemented in laboratory. An efficiency of 97.8% at 1.6 kW has been measured. Analysis, design, and the control circuitry are also presented in the paper.**

I. Introduction

THE conventional input stage for single phase power supplies operates by rectifying the ac line voltage and filtering with large electrolytic capacitors. This process generates a distorted input current waveform with large harmonic content. Thus, the resulting power factor is very poor (around 0.6).

The reduction of input current harmonics and high power factor operation are important requirements for power supplies, specially when the forthcoming harmonic standards, such as IEC-555-2, must be satisfied. In these applications, ac-dc converters featuring almost unity power factor are required.

The technique usually employed to correct power factor of single-phase power supplies consists of a front-end full-bridge diode rectifier followed by a boost converter, as shown in Fig. 1(a). This converter, however, presents commutation and conduction losses, contributing to reduce the overall efficiency of the power supply. The first does exist because the power semiconductors undergo hard commutation. The conduction losses are significant because the current always flows through three power semiconductors simultaneously, two of them are diodes, and the other one, depending on the operation stage, is a MOSFET or a diode.

In order to reduce the commutation losses, [1] and [2] have proposed similar techniques, using auxiliary commutation circuits, which are shown in Fig. 1(b). However, the conduction losses continue present in the circuit.

The circuit presented in [3] and shown in Fig. 1(c) operates with much lower conduction losses than the previous one. This occurs because the current always flows through two semiconductors simultaneously, instead of three. Nevertheless, the commutation loss problem is not solved.

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The authors are with the Department of Electrical Engineering, Power Electronics Institute, Federal University of Santa Catarina, 88040-970 Florianópolis SC, Brazil.

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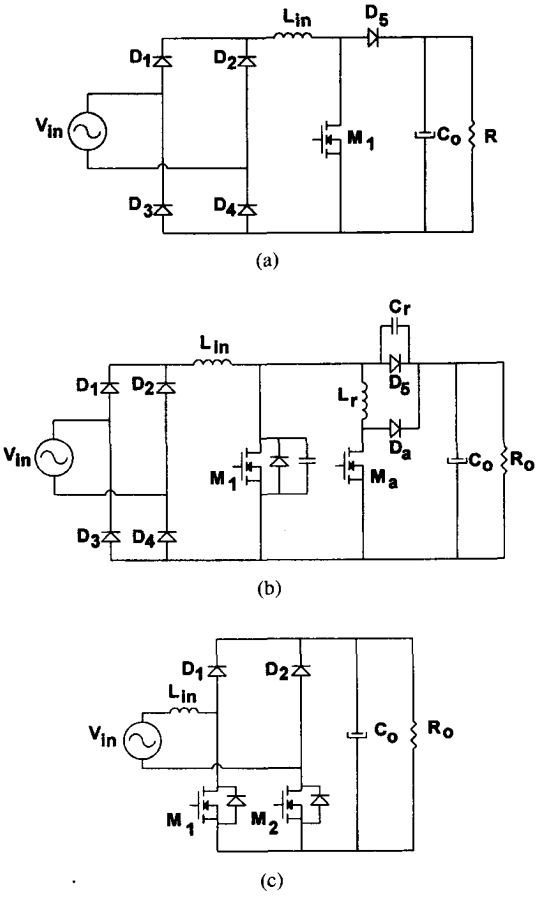


Fig. 1. (a) Conventional front-end rectifier followed by a hard-switching boost converter. (b) Conventional front-end rectifier followed by a Zero Voltage Transition boost converter. (c) Low conduction losses high power factor rectifier.

The purpose of this paper is to introduce and analyze a new converter, along with its control principle, which operates with soft-commutation and reduced conduction losses, resulting in an efficiency higher than the techniques described in the mentioned references.

II. The ZVS-PWM Unity Power Factor Rectifier with Reduced Conduction Losses

A. Circuit Description

The power stage diagram of the proposed ZVS-HPF boost converter is shown in Fig. 2. The circuit can be divided in two sections. The first is the pulse-width-modulated continuous current mode step-up converter, composed by L_{in}, M_1, M_2, D_3, D_4 and C_0, operating as two boost converters, each one in a half cycle of the input voltage.

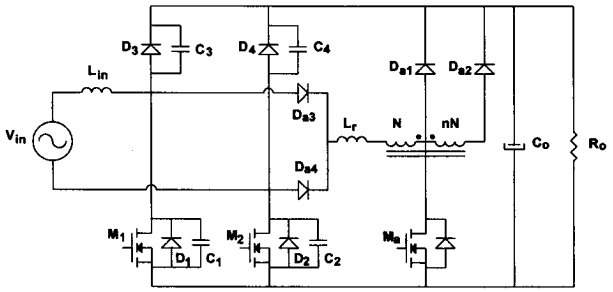
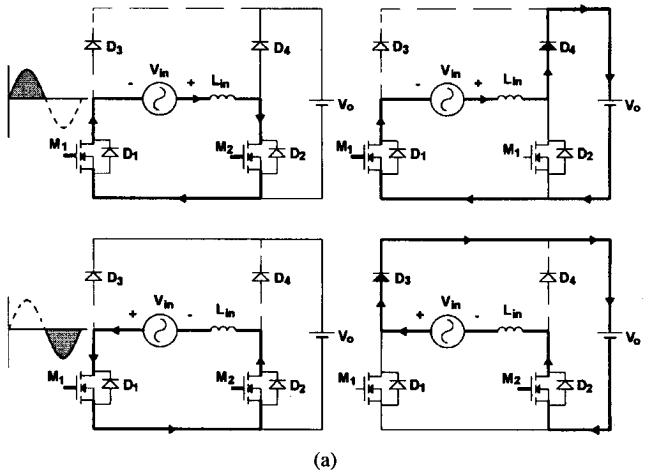
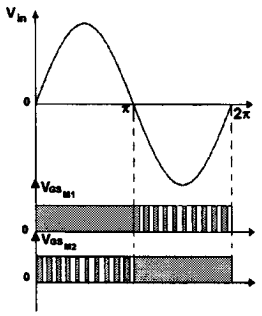


Fig. 2. Power stage diagram of the proposed converter.



(a)



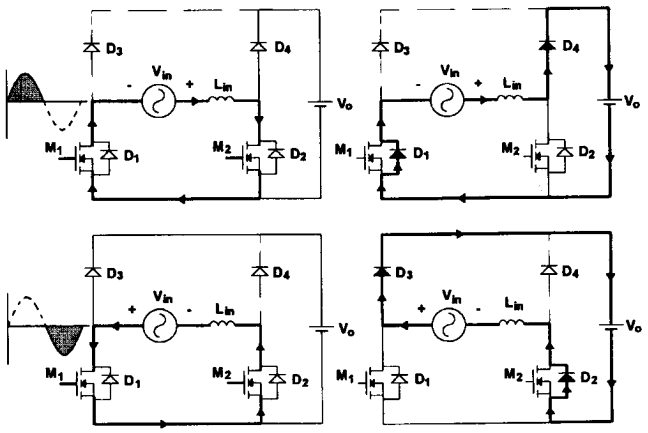
(b)

Fig. 3 (a) Topological stages for the first operation mode. (b) Gate signals of the MOSFET's for the first operation mode.

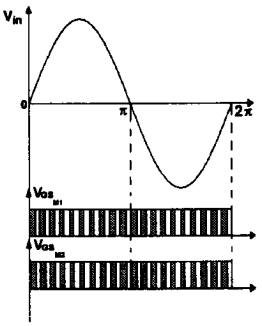
The second section is a zero-voltage-switching commutation cell [4], [5] to provide the soft-switching from D_3 to M_1 and from D_4 to M_2. It is composed of the auxiliary diodes D_{a1}, D_{a2}, D_{a3}, D_{a4}, the resonant inductor L_r, the resonant capacitors C_3 and C_4, an auto-transformer and auxiliary MOSFET M_a, which are rated for a small power when compared to the output power. The body diodes (D_1, D_2) and the parasitic capacitances of main MOSFET's (M_1, M_2) also take part in the commutation process.

B. Principle of Operation

The reduced conduction losses are achieved by the fact that there are only two semiconductors in the current flow path, instead of three semiconductors. The basic step-up converter presents two different modes of operation, which are explained hereafter.



(a)



(b)

Fig. 4 (a) Topological stages for the second operation mode. (b) Gate signals of the MOSFET's for the second operation mode.

First Mode: In the first operation mode, shown in Fig. 3, at each half line cycle, one of the two MOSFET's is conducting all the time. The other MOSFET performs the boost operation.

The MOSFET that is turned on during half line cycle will conduct the current in the reverse direction, from source to drain. The current will not flow through the body diode of this MOSFET, but through the MOSFET itself. This property will reduce the conduction losses in this device and will increase the converter efficiency. Notice that there will be only two semiconductor voltage drops in the current flow path, and one of these voltage drops will be always on a MOSFET, which will lead to smaller voltage drops when an appropriate MOSFET with low R_{DSon} is chosen.

The gate signals of the MOSFET's along with the input voltage are also shown in Fig. 3. This operation mode introduces more complexity in the circuitry to generate MOSFET's drive signals when compared to the conventional boost converter shown in Fig. 1(a).

Second Mode: In this operation mode, shown in Fig. 4, the drive signals of both MOSFET's are the same. Thus, the MOSFET's will turn-on simultaneously.

In the positive half cycle and when both MOSFET's are turned-on, the current will flow in the forward direction through MOSFET M_2 and in the reverse direction through MOSFET M_1 itself, instead of its body diode. When both MOSFET's are turned-off the current will flow through diode D_2 and through the body diode of M_1.

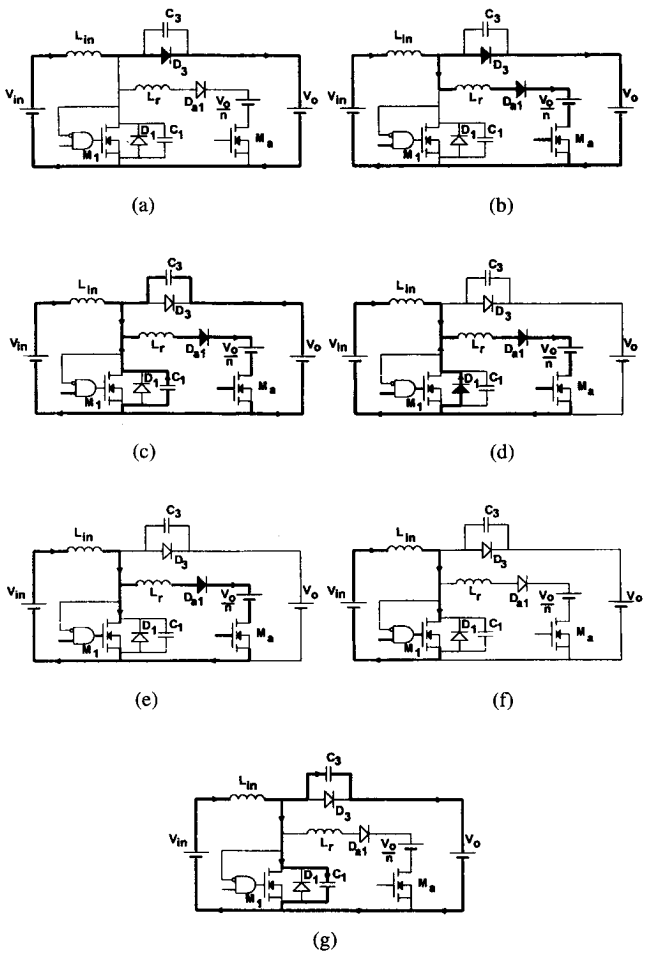


Fig. 5. Topological stages of the commutation for the simplified ZVS-PWM boost converter.

This operation mode will lead to a bit larger conduction loss than the first one. However, there will also be only two voltage drops in the current flow path and when MOSFET's are turned-on, these voltage drops will be on MOSFET's, not on diodes.

The drive signals of both MOSFET's along with line voltage are shown in Fig. 4, also. In this mode it will not be necessary to include extra logic in the drive circuitry, once the two MOSFET's have the same gate signal. This mode will allow the employment of the available PFC controllers.

Thus, the second operation mode will be chosen to the implemented prototype.

C. Commutation Analysis

The ZVS commutation will occur during a short time when compared to the switching period. Thus, it will not affect significantly the output characteristics of the boost converter operating in continuous current mode with instantaneous average line current control. During the commutation, the input voltage can also be considered as a constant voltage source.

In order to analyze the ZVS commutation of the main switches, let us assume that a positive current is flowing through L_{in}. Thus, MOSFET M_1 and diode D_3 will operate along with the commutation cell. The voltage drop in M_2 and its body diode will be neglected and the output voltage V_0 is constant. The auto-transformer will provide a voltage proportional to the output voltage that will permit the Zero-Current-Switching of the auxiliary MOSFET M_a. Therefore, the topology can be simplified in order to analyze the stages of operation shown in Fig. 5.

- **First stage** (t_0, t_1) (Fig. 5(a))—*Power transfer stage.* During this stage, power is transferred from source V_{in} to the load through diode D_3.
- **Second stage** (t_1, t_2) (Fig. 5(b))—*Linear stage.* At the instant t_1 a gate signal is applied to the drive circuits of both MOSFET's M_1 and M_a. However, only MOSFET M_a begins to conduct immediately, because a dual-thyristor circuit prevents MOSFET M_1 to conduct while its drain to source voltage does not reach zero. The current through L_r begins to increase linearly, while the current through D_3 decreases at the same rate.
- **Third stage** (t_2, t_3) (Fig. 5(c))—*Resonant stage.* At time t_2 the current through L_r is equal to the input current. The current through diode D_3 becomes zero and a resonant stage comprising L_r, C_3 and C_1 begins. The capacitor C_1 begins to discharge in a resonant way, while C_3 charges in an analogous way.
- **Fourth Stage** (t_3, t_4) (Fig. 5(d))—*Linear stage.* The voltage over C_1 becomes null, and the body diode of MOSFET M_1 begins to conduct. The current through L_r begins to decrease linearly with a voltage V_0/n applied to its terminals.
- **Fifth Stage** (t_4, t_5) (Fig. 5(e))—*Linear stage.* When the current through L_r is equal to I_{Lin}, the main MOSFET M_1 begins to conduct at zero voltage and zero current. The current through M_1 increases linearly, at the same rate in which the current through L_r decreases.
- **Sixth Stage** (t_5, t_6) (Fig. 5(f))—*Linear stage.* At instant t_5 the current through M_a extinguishes, and this MOSFET is turned off at zero current. The input current flows through M_1, accumulating energy in the input inductor L_{in}.
- **Seventh Stage** (t_6, t_0) (Fig. 5(g))—*Linear stage.* At time t_6 MOSFET M_1 is blocked. The output capacitance of M_1 begins to charge and C_3 begins to discharge in a linear way with constant current I_{Lin}. This stage finishes when $V_{C3}(t) = 0$ and $V_{C1}(t) = V_o$. At this time, diode D_3 begins to conduct the input current.

The duty-cycle of MOSFET M_1 as well as MOSFET M_2 are given by the power factor control circuit.

The theoretical waveforms for the commutation stages are shown in Fig. 6. It is important to notice that the voltages across the MOSFET's and all the diodes are clamped to the output voltage, with no stress. The current peak through the commutation circuit is much less than the double of the input current.

The commutation of the main MOSFET M_1 is shown in Fig. 9. It can be observed that zero-voltage-switching is accomplished.

The efficiency as a function of the output power is shown in Fig. 12. The efficiency obtained at 1.6 kW is very high (97.8%).

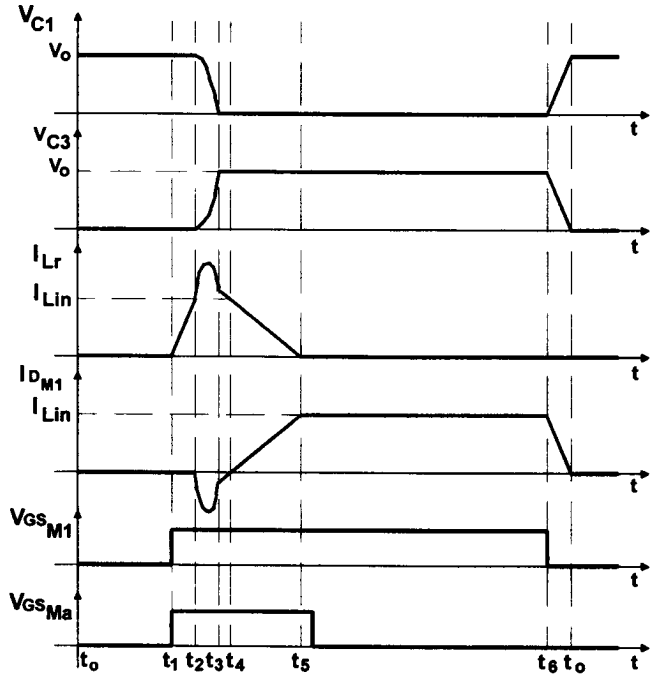


Fig. 6. Main waveforms for the simplified ZVS-PWM boost converter.

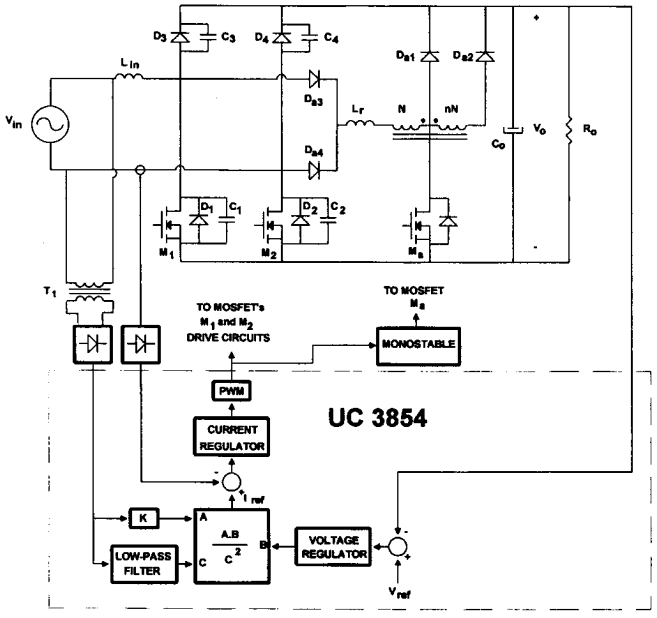


Fig. 7. Simplified circuit of the implemented prototype.

III. Theoretical Analysis

A. Auto-Transformer Turns Ratio

The auto-transformer will ensure ZCS in auxiliary switch, however, with an incorrect turns ratio it will not ensure de Zero-Voltage-Switching in the main switch. In order to obtain ZVS commutation in the main switch, it is necessary that the voltage across C_1 becomes zero at the end of third stage. The voltage across C_1 for the third stage is given by

$$V_{C1}(t) = \frac{V_o}{n} + V_o \cdot \left(\frac{n-1}{n}\right) \cdot \cos(\omega_0 t) \tag{1}$$

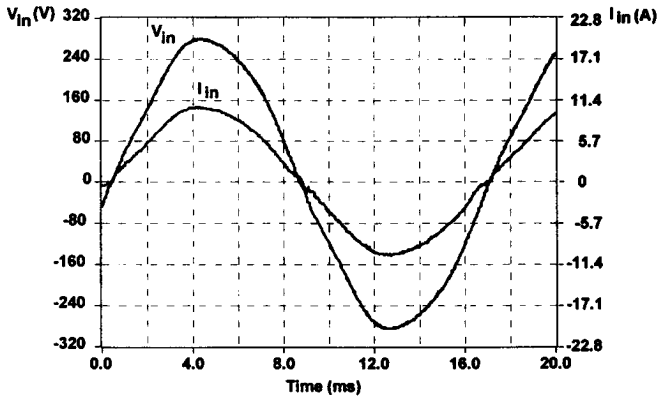


Fig. 8. Input voltage (V_{in}) and input current (I_{in}).

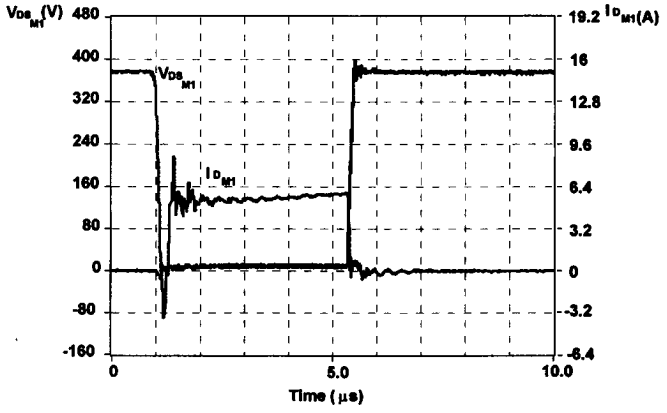


Fig. 9. Commutation detail in the main MOSFET M_1.

where

$$\omega_0 = \sqrt{\frac{1}{L_r \cdot (C_1 + C_3)}} = \sqrt{\frac{1}{L_r \cdot C_r}} \tag{2}$$

n—auto-transformer turns ratio

V_o—output voltage

C_r—equivalent capacitance.

Thus, through (1) it is possible to determine the minimum value of n.

$$\Delta t_3 = \frac{1}{\omega_0} \cdot \cos^{-1}\left(\frac{1}{1-n}\right) \tag{3}$$

$$n \geq 2. \tag{4}$$

B. Conduction Time of Auxiliary Switch

The on-time of auxiliary switch is defined by

$$\begin{aligned}\Delta t_{\text{on}} &= \Delta t_2 + \Delta t_3 + \Delta t_4 + \Delta t_5 \\ &= \frac{1}{\omega_0} \cdot \left\{ \frac{\alpha \cdot n}{n-1} + \cos^{-1}\frac{1}{1-n} \right. \\ &\qquad \left. + \sqrt{n \cdot (n-2)} + \alpha \cdot n \right\}\end{aligned} \tag{5}$$

where

$$\alpha = \frac{\sqrt{\frac{L_r}{C_r}}}{V_o} \cdot I_i. \tag{6}$$

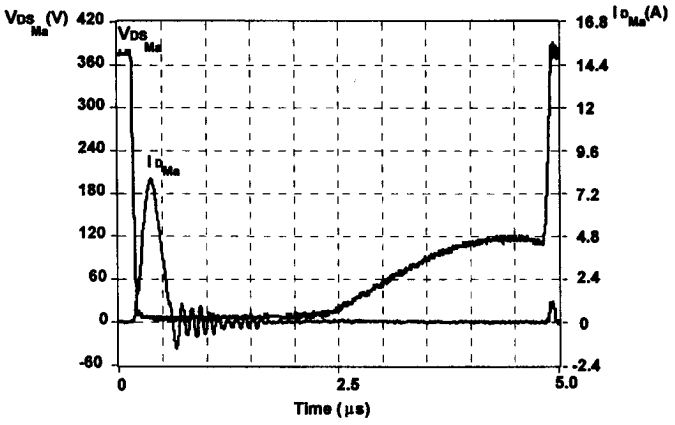


Fig. 10. Commutation detail in the auxiliary MOSFET M_a.

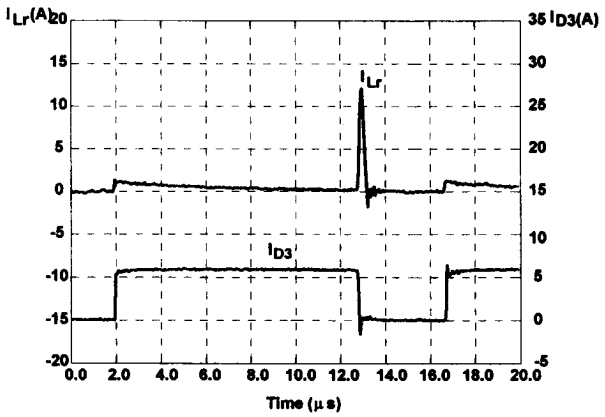


Fig. 11. Current through resonant inductor and through diode D_3.

The α parameter can be defined as a function of the resonant inductor peak current.

$$I_{Lrpk} = I_i + \frac{I_i}{\alpha} \cdot \frac{n-1}{n} \tag{7}$$

$$\alpha = \frac{I_i}{I_{pk} - I_i} \cdot \frac{n-1}{n} \tag{8}$$

$$\alpha = \frac{n-1}{n} \cdot \frac{1}{(K_I - 1)} \tag{9}$$

where

$$K_I = \frac{I_{Lrpk}}{I_i} \tag{10}$$

I_{Lrpk}—resonant inductor peak current

I_i—peak input current.

However, the maximum conduction time of auxiliary switch must be respected. This time must be less than the minimum conduction time of the main switch.

$$\Delta t_{\text{on}} \leq \Delta t = \frac{D_{\min}}{f_s} = \frac{1}{f_s} \cdot \left(1 - \frac{V_{\text{Ip}}}{V_0}\right) \tag{11}$$

where

$D_{\min}$—minimum duty-cycle on the main switch imposed by the control ciruitry

V_{Ip}—peak input voltage

f_s—switching frequency.

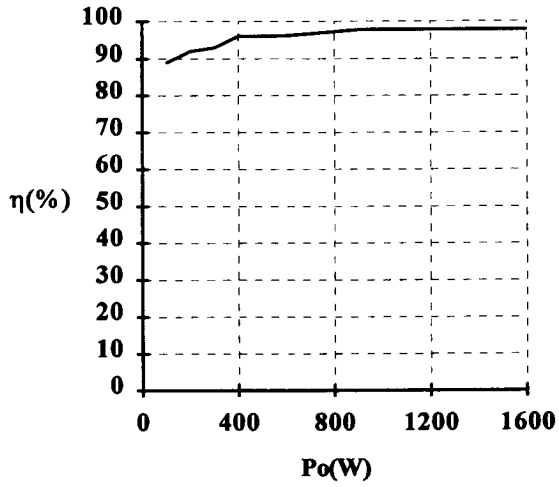


Fig. 12. Efficiency of the ZVS-PWM high power factor boost converter.

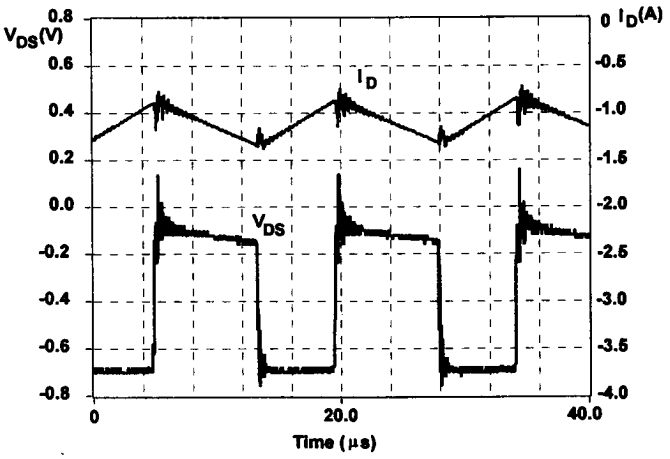


Fig. 13. Reduction of the drain-to-source voltage in main MOSFET when it is gated-on.

C. Resonant Parameters

The resonant parameters are given by (12) and (13)

$$L_r = \alpha \cdot \frac{V_o}{2 \cdot \pi \cdot f_r \cdot I_i} \tag{12}$$

$$C_r = \frac{I_i}{2 \cdot \pi \cdot f_r \cdot \alpha \cdot V_o}. \tag{13}$$

IV. Control Strategy

The converter operates in continuous current mode with constant switching frequency, making it suitable to the employment of the Unitrode PFC controller, UC3854 [6]. The block diagram of the control circuit, along with the power stage is shown in Fig. 7.

The UC3854 presents a synchronism feedback loop to define the shape and the frequency of the input current. In order to obtain almost unity power factor, the synchronism signal must be a rectified sinusoidal waveform referenced to the negative terminal of the output capacitor. This signal is accessible at the output of the rectifier bridge in the usual PFC boost converters [6]. However, in this case, it is necessary to use a small insulation transformer T_1 and a signal bridge rectifier in order

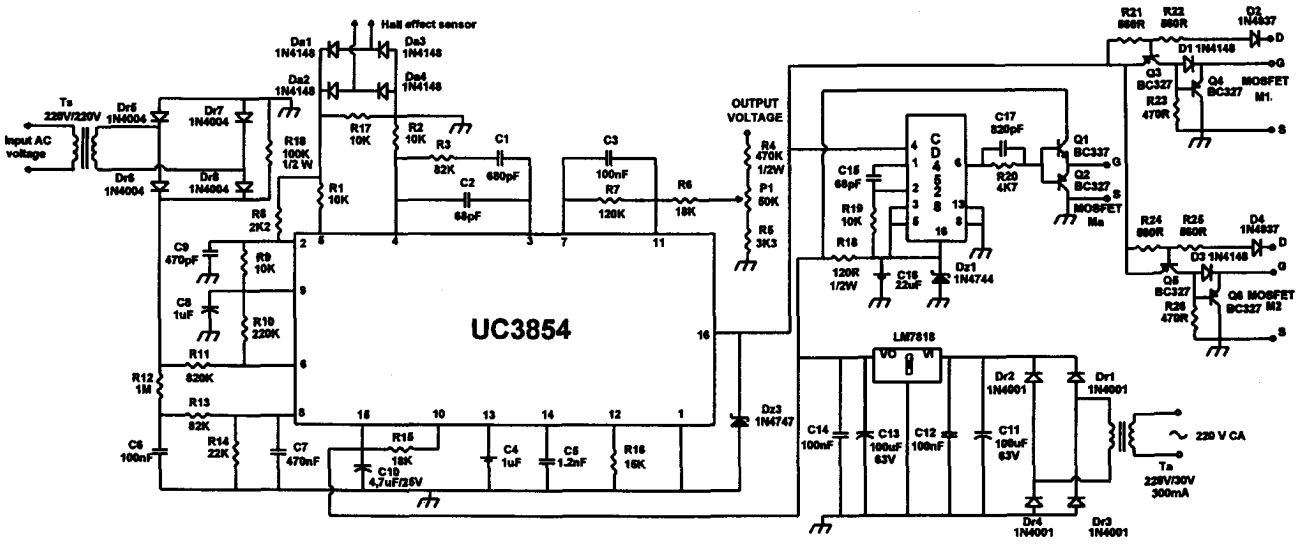


Fig. 14. Complete control circuit of the proposed converter.

to obtain the desired synchronism signal and the rms input voltage for the control IC.

A sample of the input current is monitored by a Hall effect sensor and then rectified, in order to accomplish the signal requirements for the UC3854. The reference current is then generated by a multiplier/divider combination of the synchronism feedback loop, output voltage feedback loop and input voltage feedforward loop. Since only one main MOSFET will be effective at each input half cycle, the output of UC3854 (pin 16) can be the control signal for both M_1 and M_2 drive circuits. However, this control signal will be at the gate terminals of each MOSFET only when each drain-to-source voltage is approximately equal to zero, due to the employment of the dual-thyristor circuit. The gate signal for the auxiliary MOSFET M_a is generated by a monostable circuit triggered with the rising edge of the control signal.

V. Simplified Design Example

A. Input Data

$V_i = 220$ Vrms($\pm 15\%$) $\quad P_o = 1600$ W
$V_o = 400$ V $\quad f_s = 70$ kHz
$I_i = 10.5$ A $\quad V_{\text{Ip}} = 220 \times \sqrt{2} \times 1.15 = 357.65$ V

B. Design Procedure

The minimum conduction time of the main switch is defined by (11). Thus

$$\Delta t \leq \frac{1}{70.10^3} \cdot \left(1 - \frac{357.65}{400}\right) = 1.5\ \mu\text{s}. \qquad (14)$$

Choosing $\Delta t_{\text{on}} = 0.5\ \mu\text{s}, n = 3$ and assuming that the overcurrent through the auxiliary switch is very small ($K_I \approx 1$), the following parameters are obtained:

$$f_r = 3.13 \text{ MHz}$$
$$L_r = 2.5\ \mu\text{H}$$
$$C_r = 1.5 \text{ nF}.$$

The MOSFET that will be used has an intrinsic capacitance of 522 pF. Therefore, the value of C_3 can be determined

$$C_3 = 1 \text{ nF}.$$

The pulse width of the gate signal of the auxiliary switch must meet the following relation:

$$\Delta t_{\text{on}} < t_{\text{on}} < \frac{D_{\min}}{f_s}$$
$$0.5\ \mu\text{s} < t_{\text{on}} < 1.5\ \mu\text{s}.$$

The pulse width of this gate signal is then selected to be equal to 1 μs.

VI. Experimental Results

In order to experimentally verify the principle of operation and the theoretical analysis, a 1.6 kW, 70 kHz ZVS high power factor converter has been implemented. This prototype is regulated at 400 V dc output with 220 V ac input.

It is important to notice that the body diodes and parasitic capacitances of main MOSFET's are utilized. The component specifications are as follows:

- M_1, M_2, M_a–APT 5025
- $D_3, D_4, D_{a1} - D_{a4}$–MUR 850
- C_3, C_4–1 nF/630 V (polypropylene)
- C_0–680 μF
- $L_{\text{in}} = 450\ \mu$H–65 turns (2 x 15 AWG) on EE-65/26 core
- $L_r = 2\ \mu$H–7 turns (5 x 24 AWG) on EE-25 bobbin air core
- Auto-transformer: EE-42/15 core
- $N = 20$ turns, $nN = 60$ turns

The auto-transformer presents a leakage inductance of 3.5 μH that will be added to the resonant inductance. Thus, the effective resonant inductance will be 5.5 μH. This effective inductance will increase the conduction time of the auxiliary switch but will not affect the proper operation of the converter, once the pulse width of this gate signal is equal to 1 μs.

The complete control circuit for the proposed converter is shown in Fig. 14.

It can be noticed that the auxiliary commutation cell is rated at a very low power. The input voltage and input current for the prototype operating at 1.6 kW are presented in Fig. 8. The input voltage presents some distortion. Therefore the input current will be a little distorted too. The THD of the input voltage is about 3.1%. The power factor obtained for 1.6 kW was 0.999 with a THD of 3.9% in the input current. Thus, the distortion introduced by the controller is equal to 2.36%.

The commutation detail of the auxiliary MOSFET M_a is shown in Fig. 10, where it can be noticed the zero-current-switching. If the pulse width of the gate signal of the auxiliary MOSFET is not large enough to ensure the ZCS, voltage stresses in diode D_{a4} will be expected.

The current through resonant inductor L_r and through diode D_3 are shown in Fig. 11. It can be noticed that there is an alternative path for the output current during the boost stage (D_3 or D_4 conducting). The amount of current flowing through this alternative path depends on the resonant inductance value. However, this current is negligible and decreases to nearly zero before the auxiliary MOSFET M_a is turned on.

This high efficiency is obtained from three important factors:

- There is soft-switching commutation.
- There are only two semiconductor voltage drops in the power flow path at any time.
- The conduction losses in the main MOSFET's are reduced if the gate-to-source voltage is high when the current is flowing from source-to-drain.

The last affirmation is evidenced in Fig. 13. When the current is flowing from source-to-drain and the gate-to-source voltage is high, the voltage drop across the MOSFET (VDS) is reduced from 0.7 V to 0.1 V, decreasing the conduction losses during this interval.

VII. Conclusion

This paper presents a new technique to improve the efficiency of power factor correction rectifiers, by eliminating the commutation losses and reducing the conduction losses. Therefore, a great reduction of weight and size of the heat sink is achieved.

Other features of this converter include:

- PWM control at constant frequency;
- Voltage stresses for all power semiconductor that are fixed under all load situations;
- ZVS commutation of the main MOSFET's and ZCS commutation of auxiliary MOSFET.

The new technique is suitable for high power applications, particularly for 1.5 kW and 3 kW power supplies, which are standard values for telecommunications.

References

[1] R. Streit and D. Tollik, "High efficiency telecom rectifier using a novel soft-switched boost-based input current shaper," in *IEEE INTELEC Records*, pp. 720–726, 1991.

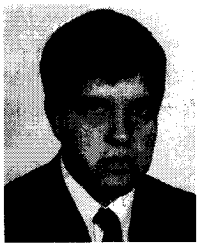
[2] G. Hua, C. S. Leu, and F. C. Lee, "Novel zero-voltage-transition PWM converters," in *IEEE PESC Records*, pp. 55–61, 1992.

[3] P. N. Enjeti and R. Martinez, "A high performance single-phase ac to dc rectifier with input power factor correction," in *IEEE APEC Records*, pp. 190–196, 1993.

[4] D. C. Martins, F. J. M. Seixas, J. A. Brilhante, and I. Barbi, "A family of dc-to-dc PWM converters using a new ZVS commutation cell," in *IEEE PESC Records*, pp. 524–530 1993.

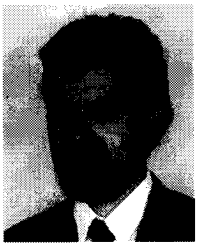
[5] P. R. Gaidzinski, A. F. Souza, and I. Barbi, "Analysis and design of a new ZVS-boost PWM converter for high power factor applications," in *COBEP Records*, Brazil, 1993, pp. 162–166.

[6] C. S. Silva, "Power factor correction with the UC3854," Unitrode Application Note.



Alexandre Ferrari de Souza (S'90–M'92) was born in Florianópolis, Santa Catarina, Brazil, in 1967. He received the B.S. degree in 1990 and the M.S. degree in 1992, both in electrical engineering, from the Federal University of Santa Catarina, Florianópolis, Brazil.

From 1992 to early 1994, he was Assistant of Research in the Power Electronics Institute of the Federal University of Santa Catarina, involved in power factor correction techniques and dc/dc converters for telecommunications. He is currently working toward the Ph.D. degree in electrical engineering at the Power Electronics Institute of the Federal University of Santa Catarina, His interests include power factor correction techniques, dc/dc converters, and soft-switching techniques.



Ivo Barbi (M'78–M'87–SM'90) was born in Gaspar, Santa Catarina, Brazil, in 1949. He received the B.S. and M.S. degrees in electrical engineering from Federal University of Santa Catarina,, Brazil, in 1973 and 1976, respectively, and the Ph.D. degree from the Institute National Polytechnique de Toulouse, France, in 1979.

He founded the Brazilian Power Electronics Society and the Power Electronics Institute of the Federal University of Santa Catarina, where he currently works as a professor. Since January of 1992, he has been Associate Editor in the Power Converters area of the IEEE Transactions on Industrial Electronics.