A New Current-Fed, Isolated PWM DC–DC Converter

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***Abstract*— This paper introduces a new current-fed dc–dc power converter circuit whose features are as follows: 1) two active switches gated in a complementary and asymmetrical way, connected to the same ground; 2) inherent high reliability provided by the input boost inductor; 3) isolation by a high-frequency transformer; and 4) output filter purely capacitive. Circuit operation, theoretical analysis, and design procedure are presented. Experimental results taken from a prototype, rated at 48 V/300 W, are also included in the paper to demonstrate the validity of the theoretical analysis**

I. Introduction

CURRENT-FED dc–dc converters have several properties, such as inherent high reliability and boost characteristics, which make them commonly employed in power factor correction.

There are three basic single-ended current-fed dc-dc converters, namely boost, sepic, and cuk. The common attribute of these three converters is the existence of the input inductor, which makes possible to draw continuous current from the input voltage source.

The push-pull current-fed dc-dc converter is the only one with two active switches connected to the same ground that has similar properties to the boost converter. It has been employed in the design of isolated battery chargers with high power factor [1], [2]. The four above-mentioned converters are shown in Fig. 1.

In this paper, a new basic current-fed, isolated two-switches converter is introduced (shown in Fig. 2). The analysis of this converter and of one topological variation are detailed in the subsequent sections of this paper.

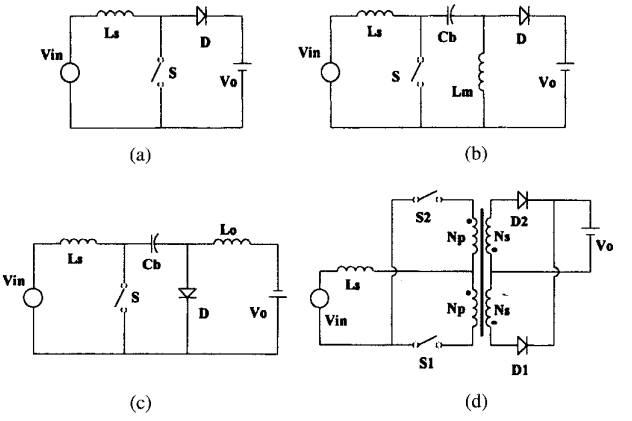

Fig. 1. Four basic current-fed converters: (a) boost, (b) sepic, (c) cuk, and (d) push-pull.

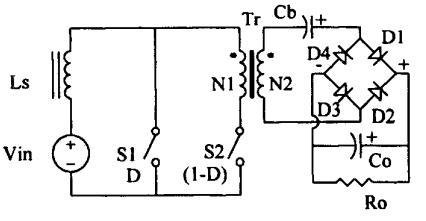

Fig. 2. The proposed current-fed, isolated PWM dc–dc converter.

II. Topology and Qualitative Analysis

A. Circuit Description

The inductor L_s placed in series with the voltage source V_{in} gives an instantaneous current source characteristic to the converter input. The power switches are gated at constant frequency and asymmetrical duty cycle, i. e., switch S_1 operates with duty cycle D during the switching period and S_2 operates complementary to S_1. The circuit is isolated by transformer T_r and, due to the operation with asymmetrical duty cycle, the converter requires the capacitor C_b to ensure magnetic flux balance in the transformer. Diodes D_1, D_2, D_3, and D_4 form the output rectifier and C_o represents the output filter capacitor.

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B. Modes of Operation

In order to simplify the analysis, the following assumptions are made:

- the power semiconductors are ideal;
- capacitors C_b and C_o are assumed as constant voltage sources during a switching period;
- the analysis is based on the circuit reflected to the primary side of the transformer.

The converter may assume four different circuit configurations during a switching period T_s, as shown in Fig. 3. Switch S_1 is closed when the converter assumes the first and second configurations. Otherwise, if the converter assumes the third and fourth configurations, switch S_1 is open. Switch S_2 operates complementary to S_1.

Taking into account the configurations shown in Fig. 3, it is possible to combine them and generate the converter operation

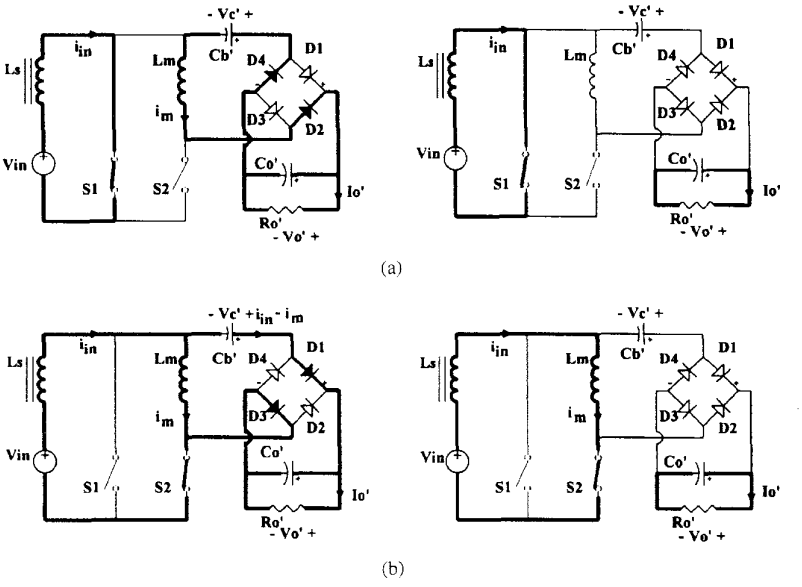


Fig. 3. Possible circuit configurations.

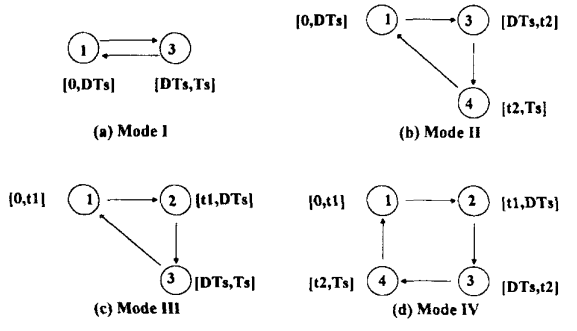


Fig. 4. Converter operation modes. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV.

modes as depicted in Fig. 4. The arrows are showing the circuit configuration that is assumed by the converter and the time interval is indicated in square brackets.

1) Mode I, Fig. 4(a): During the time interval $(0, DT_s)$ the converter assumes the first configuration. Switch S_1 is turned-on and complementary S_2 is turned-off. The input current i_{in} rises linearly, while the magnetizing current i_m is linearly decreasing. During this time interval, it is stored energy in L_s and L_m is demagnetizing through the output section and capacitor C_b'.

In the next interval (DT_s, T_s), switch S_1 is turned-off and S_2 is turned-on and the converter assumes the third configuration. The energy previously stored in L_s is delivered to magnetize the transformer and to the output section through diodes D_1 and D_3.

2) Mode II, Fig. 4(b): During the time interval $(0, DT_s)$ the converter assumes the first configuration. At the instant DT_s, the converter starts operating under the third configuration. The current i_m rises linearly until the instant t_2. At that instant, the magnetizing current equals the input current and the rectifier diodes D_1 and D_3 are blocked. The converter assumes the fourth configuration, and during the interval (t_2, T_s) the input current and the magnetizing current rise together with the same slope.

3) Mode III, Fig. 4(c): During the time interval $(0, t_1)$ the converter assumes the first configuration, whose behavior has already been described. At the instant t_1, the magnetizing current i_m achieves zero, the even rectifier diodes are blocked, and the converter assumes the second configuration until the time DT_s.

At the moment DT_s, switch S_1 is turned-off and S_2 is turned-on. The converter assumes the third configuration until the end of the switching period T_s.

4) Mode IV, Fig. 4(d): During the interval $(0, t_1)$ the converter assumes the first configuration. When the magnetizing current achieves zero, the converter start operating under the second configuration.

At the instant DT_s, S_1 is turned-off and S_2 is turned-on and the converter assumes the third configuration. When i_m equals i_{in}, diodes D_1 and D_3 are blocked and the converter assumes the fourth configuration until the instant T_s.

Discontinuous conduction is characterized when all rectifier diodes are blocked. Thus, discontinuity can be observed in modes II–IV, because these modes contain the second and/or fourth circuit configurations (which present all rectifier diodes blocked). Mode I is the only one that presents continuous conduction and will be discussed in more detail later.

The theoretical main waveforms of the converter operating in continuous conduction mode (mode I) are shown in Fig. 5.

III. Output Characteristics

To obtain the output characteristics we can perform the magnetic flux balance in the magnetic devices and the electric charge balance in the capacitors.

1) Mode I: To maintain the magnetic flux balance in the input inductor L_s, the average voltage across it must be zero.

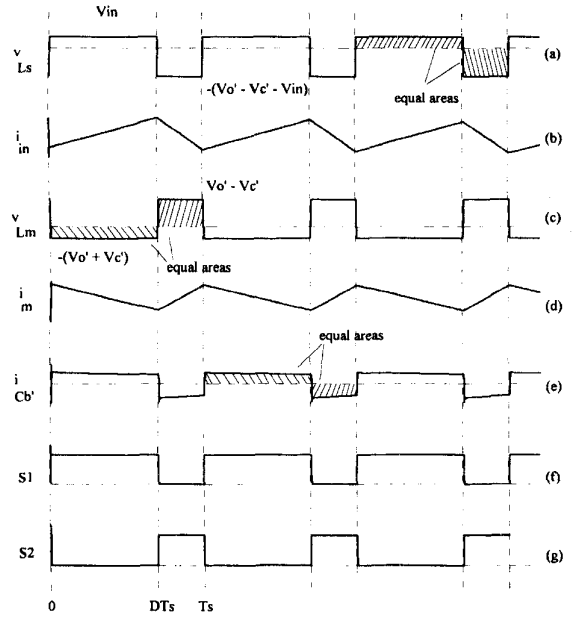


Fig. 5. Typical theoretical waveforms presented by the asymmetrical PWM dc–dc converter operating in mode I (continuous conduction).

Thus, from Fig. 5(a)

$$V_{\text{in}} DT_s = (V_o' - V_c' - V_{\text{in}})(1-D)T_s. \tag{1}$$

Similarly, from the magnetic flux balance in the transformer, results in

$$(V_o' + V_c')DT_s = (V_o' - V_c')(1-D)T_s. \tag{2}$$

We can derive from (1) and (2) the following expressions:

$$q \equiv \frac{V_o'}{V_{\text{in}}} = \frac{1}{2D(1-D)} \tag{3}$$

$$\beta \equiv \frac{V_c'}{V_{\text{in}}} = \frac{1-2D}{2D(1-D)}. \tag{4}$$

Equation (3) represents the dc–dc voltage gain of the asymmetrical converter. As can be observed, the asymmetrical PWM topology operates as a step-up converter, where the minimum output voltage reflected to the primary side of the transformer is twice the input voltage. Equation (4) represents the normalized voltage across capacitor C_b' as a function of the duty cycle.

The power switches of the proposed converter are subjected to the following voltage stresses:

$$V_{S_1} = V_o' - V_c' \tag{5}$$

$$V_{S_2} = V_o' + V_c'. \tag{6}$$

Substituting (3) and (4) in (5) and (6) will result in

$$V_{S_1} = \frac{V_{\text{in}}}{1-D} \tag{7}$$

$$V_{S_2} = \frac{V_{\text{in}}}{D}. \tag{8}$$

The average magnetizing current of the transformer is given by $(1-D)I_{\text{in}}$. If the duty cycle is increased, preserving I_{in} at a constant level, the average magnetizing current is decreased. For this reason, in order to facilitate the transformer operation, the duty cycle will be set higher than 0.50.

TABLE I
COMPARISON BETWEEN ASYMMETRICAL PWM dc-dc CONVERTER AND PUSH-PULL CURRENT-FED TOPOLOGY

Converter	DC-DC voltage gain	Switch voltage stress
Asymmetrical PWM DC-DC Converter	$G_{asy} \equiv V_o'/V_{in} = 1/2D(1-D)$	$V_{S_1}/V_{in} = 1/1-D$
Push-Pull Current-Fed DC-DC Converter	$G_{pp} \equiv V_{o_{pp}}'/V_{in_{pp}}' = 1/1-D_{pp}$	$V_{S_{pp}}/V_{in_{pp}} = 2/1-D_{pp}$

As can be seen from (7) and (8), if the duty cycle is higher than 0.5, the voltage across switch S_1 will be greater than the voltage across S_2. It is important to compare the worst stress with the classical current-fed push-pull topology. The dc–dc voltage gain and the voltage stress across the power switches of the push-pull current-fed converter are well known from the literature. These relations are given by expressions outlined in Table I.

We refer to Fig. 1(d) in order to obtain the push-pull dc–dc voltage gain and the voltage stress across the power switches, where the push-pull duty cycle (D_{pp}) in Table I is defined as being the total conduction overlap time between the power switches in relation to the switching period D_{pp} and can be changed from zero up to one.

The relations of Table I are graphically illustrated in Fig. 6. The comparison will be made taking into account the operation range of the duty cycle of the proposed converter, i. e., $D > 0.5$. If we suppose that $G_{\text{asy}} = G_{pp}$, for instance $G_{\text{asy}} = G_{\text{pp}} = 3$, we can verify from Fig. 6 that the duty cycle of the proposed converter will be approximately $D \cong 0.79$ and the push-pull duty cycle will be $D_{pp} \cong 0.67$. It can be notice that the voltage across switch S_1 of the asymmetrical converter in relation to the input voltage will be $V_{S_1}/V_{\text{in}} \cong 4.73$ for the proposed converter and $V_{S_{pp}}/V_{\text{in}_{pp}} \cong 6$ for the push-pull topology. If the input voltage of both converters are taken as $V_{\text{in}} = V_{\text{in}_{pp}}$, we can conclude from the analysis that $V_{S_1} < V_{S_{pp}}$. Therefore, for identical dc–dc voltage gain, output voltage, and input voltage, the asymmetrical converter subjects the active power switches to lower voltage stress in comparison to the classical push-pull current-fed topology.

2) Mode II: Modes II–IV present discontinuous conduction. Therefore, the output voltage is a function of the load. This renders the mathematical analysis longer than the analysis of mode I. For this reason, we will present only the final equations for the referred modes.

The resulting equations for mode II are summarized below. The normalized output voltage (q) and the normalized voltage

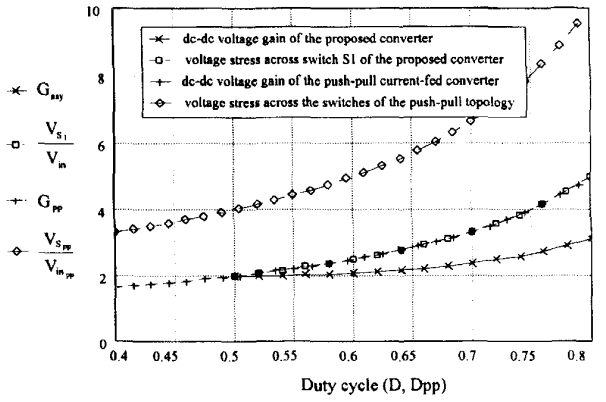


Fig. 6. Graphical comparison between asymmetrical PWM dc–dc converter and push-pull, current-fed topology.

across $C_b'(\beta)$ are described as a function of the normalized output current (γ) reflected to the primary side of the transformer, duty cycle (D), and inductance factor (K)

$$q = \frac{K(KD+K+1)}{2KD(1+K)} + \frac{D(KD+1)^2}{2KD(1+K)\gamma} \tag{9}$$

$$\beta = -\frac{K(KD-K-1)}{2KD(1+K)} - \frac{D(KD+1)^2}{2KD(1+K)\gamma} \tag{10}$$

where

$$\gamma \equiv \frac{I_o' L_s}{V_{\text{in}} T_s} \tag{11}$$

$$K \equiv \frac{L_m}{L_s}. \tag{12}$$

3) Mode III: The final equations for mode III are

$$q = \frac{1}{2(1-D)} + \frac{1-KD}{2(1-D)\gamma} \tag{13}$$

$$\beta = -\frac{1}{2(1-D)} + \frac{1-KD}{2(1-D)\gamma}. \tag{14}$$

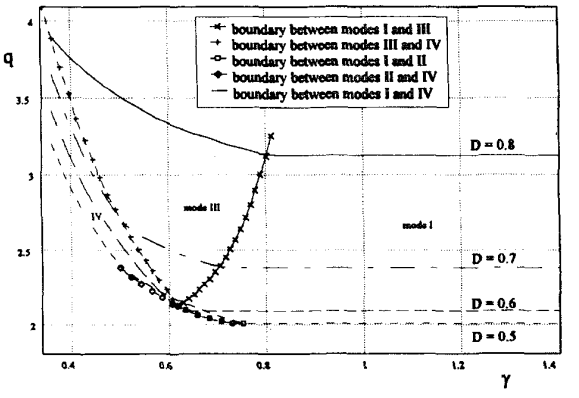
4) Mode IV: The flux balance in the magnetic devices and the electric charge balance in the capacitors give the following expressions for mode IV:

$$q = \frac{K^2}{2K(1+K)} + \frac{DK(DK+2)+2+K}{2K(1+K)\gamma} \tag{15}$$

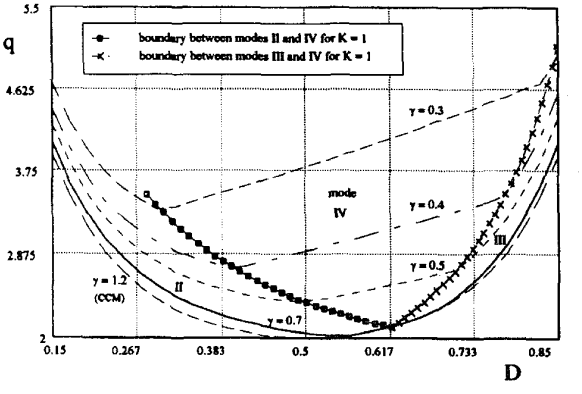
$$\beta = -\frac{K}{2(1+K)} - \frac{D(DK+2)-1}{2(1+K)\gamma}. \tag{16}$$

From the previously obtained equations, we can represent graphically the output characteristics, as shown in Fig. 7. Fig. 7(a) shows the normalized output voltage (q) as a function of the normalized output current (γ) both reflected to the primary side of the transformer, taking the duty cycle (D) as parameter and for $K = 1$.

At high load, the characteristics are completely flat and the converter output impedance is zero. On the other hand, at low load the characteristics rise abruptly because the converter is operating in discontinuous conduction mode. The control variable is the duty cycle and the converter requires a minimum load to operate properly.



(a)



(b)

Fig. 7. Output characteristics for $K = 1$. (a) Normalized output voltage (q) as a function of the normalized output current (γ), taking the duty cycle (D) as parameter. (b) Normalized output voltage (q) as a function of the duty cycle (D), taking the normalized output current (γ) as parameter.

Fig. 7(b) shows the normalized output voltage (q) as a function of the duty cycle (D), taking the normalized output current (γ) as parameter and for $K = 1$. If $\gamma = 1, 2$, the converter is operating in continuous conduction mode and the curve of $q \times D$ represents the dc–dc voltage gain described by (3). Note that for this condition the function $q \times D$ is symmetrical with regard to $D = 0.5$. Hence, to operate the converter in closed loop we must choose one of the sides of the curve. As can be seen in Fig. 7(b), this symmetry is not held when the converter operates in one of the discontinuous conduction modes. Moreover, taking the curve of $q \times D$ for $\gamma = 0.7$ [solid line in Fig. 7(b)], to produce a given output voltage inside the interval $0.5 < D < 0.617$, we could obtain two different values of duty cycle. Consequently, if we want to operate the converter in discontinuous conduction mode, it is important to limit the operation in modes III and IV when $D > 0.5$, and naturally in modes II and IV when $D < 0.5$.

Fig. 8 shows the influence of the factor K on the output characteristics. In this figure, the duty cycle has been set to $D = 0.5$ and the factor K has been changed from 0.2 to 1.0. It can be verified that the operation range in mode I (conduction continuos mode) is expanded as the factor K is increased. Thus, if the converter operation must be limited in

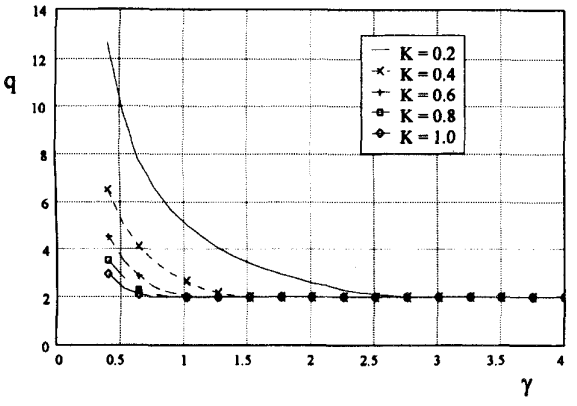


Fig. 8. Influence of the factor K on the output characteristics.

mode I, it is important to take the factor K as high as possible. However, the factor K depends on the magnetizing inductance L_m and the input inductance L_s. The value of the magnetizing inductance is generally limited by the transformer design. On the other hand, the value of the input inductance is determined taking into account the specified input current ripple. From (12) we can see that the higher the factor K is, the lower the input inductance and as a consequence the greater the input current ripple. Thus, to avoid large input current ripple and expand the operation range in continuous conduction mode, the factor K has been chosen $K = 1$.

IV. Design Considerations and Example

The input data for the design of the converter are as follows:

input voltage:	$V_{\text{in}} = 48$ V
output voltage:	$V_o = 48$ V
switching frequency:	$f_s = 40$ KHz
rated output power:	$P_{\text{nom}} = 300$ W
minimum output power in mode I:	$P_{\min} = 150$ W

1) Duty Cycle: From (7) and (8), we can notice that the voltage stress across the switches are increased as the duty cycle becomes more asymmetrical. Thus, to prevent large stress on the power switches, the duty cycle has been chosen $D = 0.7$.

2) Output Voltage, Input Current and Output Current: After choosing the duty cycle, from (3) we have

$$q = \frac{1}{2D(1-D)} = \frac{1}{2 \times 0.7 \times (1-0.7)} = 2.38.$$

The output voltage reflected to the primary side of the transformer is

$$V_o' = qV_{\text{in}} = 2.38 \times 48 = 114.24 \text{ V}.$$

Thus, the transformer turns ratio is

$$n = \frac{V_o'}{V_o} = \frac{114.24}{48} = 2.38.$$

The rated input and output currents are

$$I_{\text{in}} = P_{\text{nom}}/V_{\text{in}} = 300/48 = 6.25 \text{ A}$$
$$I_o = P_{\text{nom}}/V_o = 300/48 = 6.25 \text{ A}$$
$$I_o' = I_o/n = 6.25/2.38 = 2.63 \text{ A}.$$

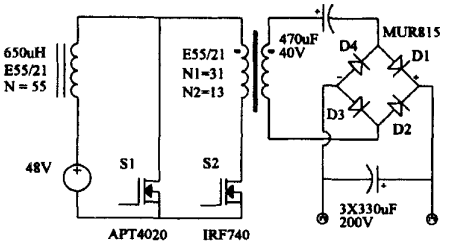


Fig. 9. Power stage diagram of the implemented converter.

The average current through the magnetizing inductance of the transformer is given by

$$I_m = (1-D)I_{\text{in}} = (1-0.7) \times 6.25 = 1.88 \text{ A}.$$

The minimum input and output currents are

$$I_{\text{in}_{\min}} = P_{\min}/V_{\text{in}} = 150/48 = 3.125 \text{ A}$$
$$I_{o_{\min}} = P_{\min}/V_o = 150/48 = 3.125 \text{ A}$$
$$I_{o_{\min}}' = I_{o_{\min}}/n = 3.125/2.38 = 1.3 \text{ A}.$$

3) Operation Range: We intend to limit the converter operation in mode I. From Fig. 7(a), for the chosen duty cycle $D = 0.7$ the minimum normalized output current $\gamma_{\min}$ in mode I is approximately 0.70. Then, the inductances L_s and L_m can be determined as follows:

$$L_s = \gamma_{\min} V_{\text{in}} T_s / I_{o_{\min}}' = 0.7 \times 48 \times 2510^{-6}/1.3$$
$$= 646 \ \mu\text{H}$$
$$L_m = KL_s = 1 \times 646 \times 10^{-6} = 646 \ \mu\text{H}.$$

4) Voltage and Current Through Switch S_1: The voltage across switch S_1 during its off-time is

$$V_{S_1} = V_{\text{in}}/(1-D) = 48/(1-0.7) = 160 \text{ V}$$

The average and rms currents are determined as follows:

$$I_{1_{\text{avg}}} = DI_{\text{in}} = 0.7 \times 6.25 = 4.38 \text{ A}$$
$$I_{1_{\text{rms}}} = \sqrt{D} I_{\text{in}} = \sqrt{0.7} \times 6.25 = 5.23 \text{ A}.$$

5) Voltage and Current Through Switch S_2: Similarly, during its off-time, the voltage across S_2 is

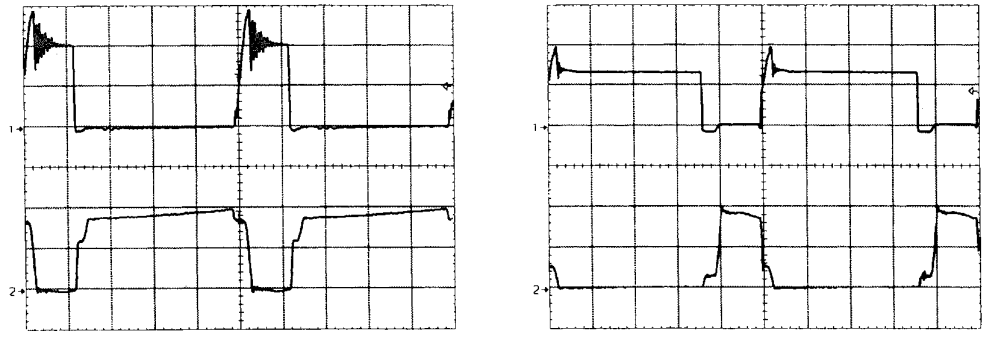
$$V_{S_2} = V_{\text{in}}/D = 48/0.7 = 68.6 \text{ V}.$$

The average and rms currents are

$$I_{2_{\text{avg}}} = (1-D)I_{\text{in}} = (1-0.7) \times 6.25 = 1.88 \text{ A}$$
$$I_{2_{\text{rms}}} = \sqrt{(1-D)} I_{\text{in}} = \sqrt{(1-0.7)} \times 6.25 = 3.42 \text{ A}.$$

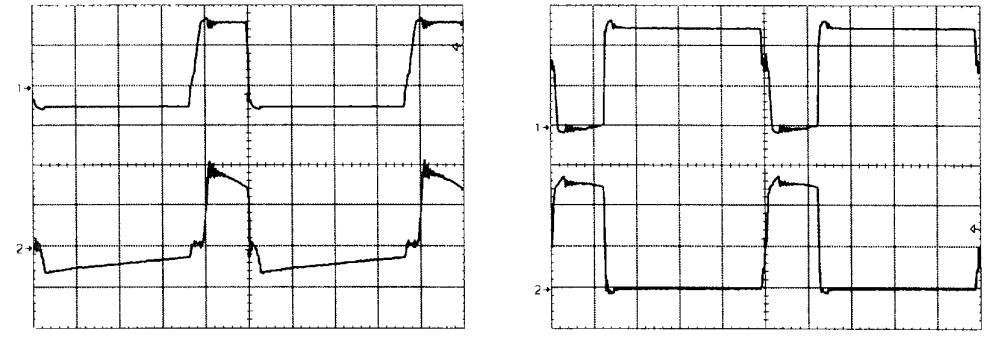
6) Capacitor C_b: The average voltage across capacitor C_b is determined from (4)

$$V_c' = \frac{1-2D}{2D(1-D)} V_{\text{in}} = \frac{1-2 \times 0.7}{2 \times 0.7 \times (1-0.7)} \times 48$$
$$= -45.7 \text{ V}$$
$$V_c = \frac{V_c'}{n} = \frac{-45.7}{2.38} = -19.2 \text{ V}.$$



(a) (b)

Fig. 10. Experimental waveforms. (a) Voltage [100 V/div.] and current [5 A/div.] through switch S_1. (b) Voltage [50 V/div.] and current [5 A/div.] through switch S_2. Time scale [5 s/div.].



(a) (b)

Fig. 11. Experimental waveforms. (a) Voltage [50 V/div.] across the secondary side of the transformer and current [10 A/div.] through capacitor C_b. (b) Voltage [20 V/div.] across the rectifier diodes; upper trace odd diodes and lower trace even diodes. Time scale [5 μs/div.].

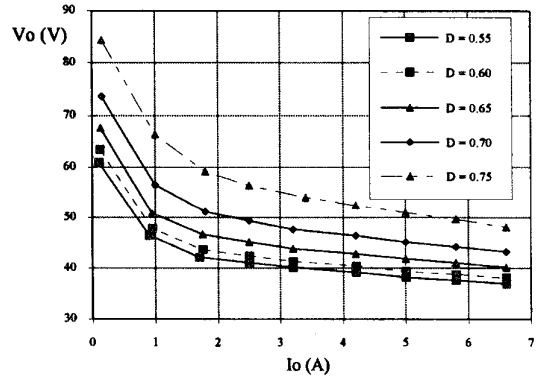


Fig. 12. Experimental output characteristics of the proposed converter.

The voltage ripple across C_b determines its capacitance. Limiting the voltage ripple at 2% of its average value, yields

$$C_b \geq \frac{nD(1-D)I_{\text{in}}}{\Delta V_{C_b} f_s} \geq \frac{2.38 \times 0.7 \times (1-0.7) \times 6.25}{0.02 \times 19.2 \times 40 \times 10^3} \geq 205\ \mu\text{F}.$$

7) Capacitor C_o: During the first interval $(0, DT_s)$ the current through C_o is given by $I_x = (nI_m - I_o)$, and during the second interval (DT_s, T_s) by $I_y = (nI_{\text{in}} - nI_m - I_o)$.

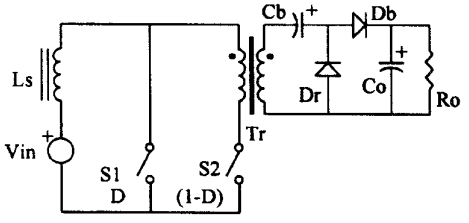


Fig. 13. Topological variation of the proposed PWM dc–dc converter.

Then, the current ripple is calculated as follows:

$$\Delta I_{C_o} = I_y - I_x = nI_{\text{in}}(2D-1) = 2.38 \times 6.25 \times (2 \times 0.7 - 1) = 5.95\ \text{A}.$$

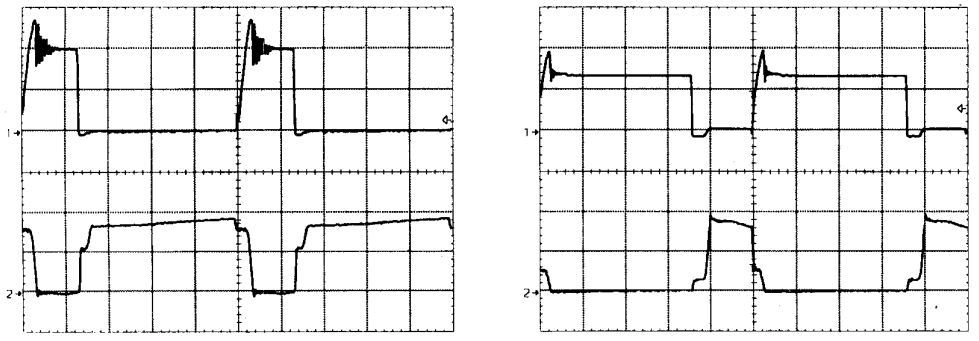
The equivalent series resistance (esr) of the capacitor limits the output voltage ripple. Taking the output voltage peak-to-peak ripple as 1% of its average value, yields

$$\text{esr} \leq 0.01 V_o / \Delta I_{C_o} = 0.01 \times 48/5.95 \leq 80\ \text{m}\Omega$$

The capacitance value also affects the output ripple. Thus

$$C_o \geq \frac{[I_o - nI_{\text{in}}(1-D)]}{\Delta V_{C_o} f_s} \times D$$

$$C_o \geq \frac{[6.25 - 2.38 \times 6.25 \times (1-0.7)]}{0.01 \times 48 \times 40 \times 10^3} \times 0.7 \geq 65\ \mu\text{F}.$$



(a) (b)

Fig. 14. Experimental results of the topological variation. (a) Voltage [100 V/div.] and current (5 A/div.) through switch S_1. (b) Voltage [50 V/div.] and current (5 A/div.) through switch S_2. Time scale [5 μs/div.].

V. Experimental Results

To verify the practical aspects of the asymmetrical PWM dc–dc converter, a laboratory prototype has been assembled and tested (power stage diagram is shown in Fig. 9). The relevant waveforms taken from the converter operating at rated power are shown in Figs. 10 and 11. The experimental duty cycle has been set to 0.74 in order to supply the losses inside the converter.

Snubber circuits have been used to avoid overvoltages during the switches turn-off (not shown in Fig. 9).

The voltage across S_1 (upper trace) and its corresponding current (lower trace) are shown in Fig. 10(a), while the voltage across S_2 (upper trace) and its current (lower trace) are shown in Fig. 10(b). The waveforms are quite similar to those presented by the conventional current-fed PWM dc–dc converters.

The voltage across the secondary side of the transformer (upper trace) and the current through capacitor C_b are shown in Fig. 11(a). The upper trace of Fig. 11(b) shows the voltage across diodes D_1 and D_3, while the lower trace is showing the voltage across diodes D_2 and D_4. It is noticed that there is no overvoltage across the rectifier diodes.

The experimental output characteristics are shown in Fig. 12 representing the output voltage as a function of the output current, both reflected to the secondary side of the transformer, and the duty cycle as parameter. It can be seen that the duty cycle controls the output power and regulates the output voltage. Due to the on-resistance of the switches, the voltage drop across the rectifiers, and the leakage inductance of the transformer the experimental characteristics are slightly different from those theoretical presented in Fig. 7(a).

VI. Topological Variation

A topological variation of the circuit shown in Fig. 2 is represented in Fig. 13, which utilizes an output rectifier with only two diodes instead of four.

Assuming continuous conduction mode, during the first time interval, S_1 conducts the input current. Energy is stored in L_s, while the transformer is demagnetizing through diode D_r and capacitor C_b. After the first time interval, S_1 is turned off and S_2 is turned on. The energy previously stored in L_s is delivered to magnetize the transformer and to the output section through diode D_b.

The dc–dc voltage gain of the topological variation is described by (17). It can be observed that the reflected output voltage (V_o') is at least four times the input voltage (V_{in}).

$$\frac{V_o'}{V_{\text{in}}} = \frac{1}{D(1-D)}. \tag{17}$$

The experimental results were taken from the topological variation at rated conditions as described in Section IV, except for the output voltage, which is specified to 96 V.

Fig. 14(a) shows the voltage across S_1 (upper trace) and its corresponding current, while Fig. 14(b) is showing the voltage across S_2 (upper trace) and its current (lower trace).

The upper trace of Fig. 15(a) shows the voltage across the secondary side of the transformer and the lower trace shows the current through C_b. Finally, the voltage across diode D_r is represented by the upper trace of Fig. 15(b), while the lower trace is showing the voltage across diode D_b.

The waveforms are quite similar to those presented by the original converter. The difference is the voltage across the rectifier diodes, which is multiplied by two.

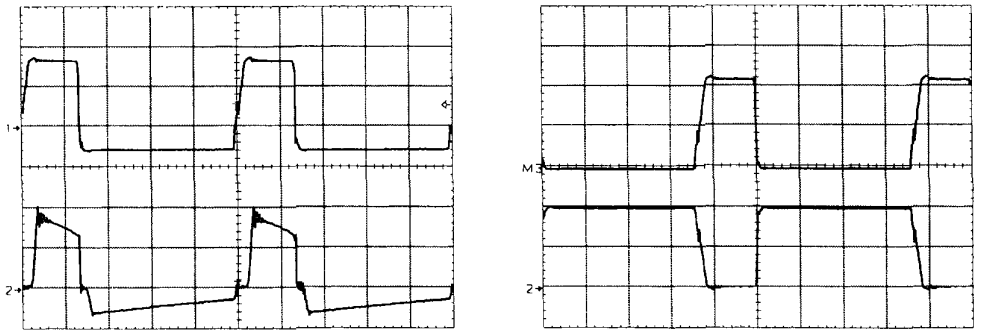
The experimental output characteristics reflected to the secondary side of the transformer are shown in Fig. 16, representing the output voltage as a function of the output current and taking the duty cycle as parameter.

The proposed PWM converter and the topological variation efficiency curves are shown in Fig. 17. Although the current levels presented in the secondary side of the transformer are the same in both cases, the topological variation efficiency is slightly better, because it has only two rectifier diodes.

VII. Conclusion

From the theoretical and experimental results presented in this paper, related to the new current-fed, isolated PWM dc–dc converter, we can draw the following conclusions:

1) the results obtained by theoretical analysis represent the behavior of the converter and can be used to design and predict its performance;



(a) (b)

Fig. 15. Experimental waveforms. (a) Voltage [50 V/div.] across the secondary side of the transformer and current [10 A/div.] through capacitor C_b. (b) Voltage [50 V/div.] across the rectifier diodes, upper trace D_r and lower trace D_b. Time scale [5 μs/div.].

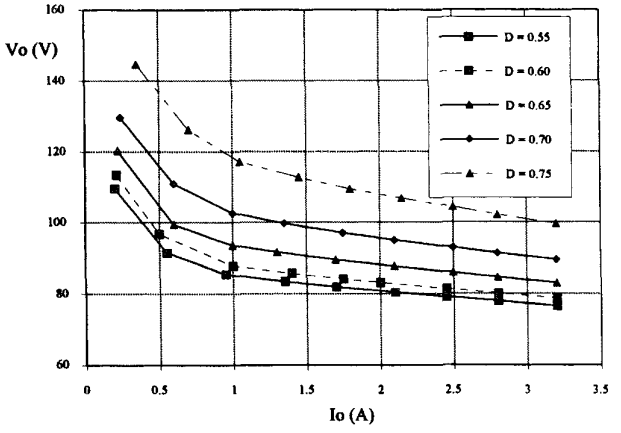


Fig. 16. Experimental characteristics of the topological variation.

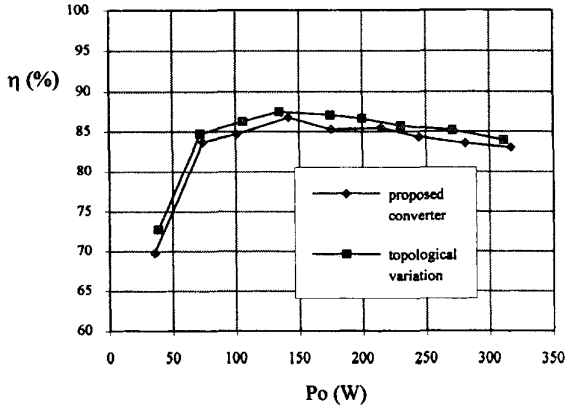


Fig. 17. Efficiency curves.

2) the new converter has all the basic characteristics of the classical current-fed isolated boost converters, such as input inductor, low-input current ripple, isolation, and regulation by pulse width modulation;

3) for identical dc–dc voltage gain, input voltage, and output voltage, the new converter subjects the active power switches to lower voltage stress compared to the classical push-pull current-fed topology.

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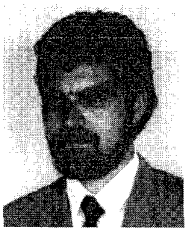

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