A Family of ZVS-PWM Active-Clamping DC-to-DC Converters: Synthesis, Analysis, Design, and Experimentation

Cláudio Manoel C. Duarte, *Student Member, IEEE*, and Ivo Barbi, *Senior Member, IEEE*

***Abstract*—This paper presents a technique to generate a complete family of two-switch pulsewidth-modulated (PWM) with active clamping dc/dc converters, featuring soft commutation of the semiconductors at zero-voltage (ZVS). The main purpose of this technique is to integrate these converters under a same theoretical principle to derive the topologies in a comprehensive form and generate new circuits. All the converters have the advantage of soft commutation (ZVS) with minimum switch voltage stress due to the clamping action. Besides operating at constant frequency and with reduced commutation losses, these converters have output characteristics similar to the PWM hard-switching counterpart, which means that there is no circulating reactive energy that would cause large conduction losses. Principle of operation, theoretical analysis, simulation and experimental results of one particular converter taken as an example, are provided in this paper.**

***Index Terms*— Active clamping, dc-to-dc converters, power supplies, soft commutation.**

I. Introduction

THE TWO TRANSFORMER active reset circuits presented in [1] and shown in Fig. 1 were employed in a Forward converter to operate over a wide input voltage range. These circuits recover transformer magnetizing and leakage inductance energies, reduce dc flux in the core, and minimize peak voltage on the power transistor. One of these circuits, Fig. 1(b), was employed in a Flyback converter [2] to achieve soft switching too. In [3], the other circuit, Fig. 1(a), was employed in a Forward converter with some modifications and the soft switching was obtained too. The circuit shown in Fig. 1(a) was used in [4] as a switched snubber for the switch and the diode of high frequency PWM converters. In [5], the interrelationships among two switch soft-switched converters were analyzed and a generalization was searched by a generalized two-switched converter.

In this paper, the concept of fundamental ZVS-PWM cells was employed to generate a complete family of two-switch clamped mode ZVS-PWM dc-dc converters. This technique allows the generation, in a comprehensive form, of six basic family converters. The generation of the cells is described hereafter.

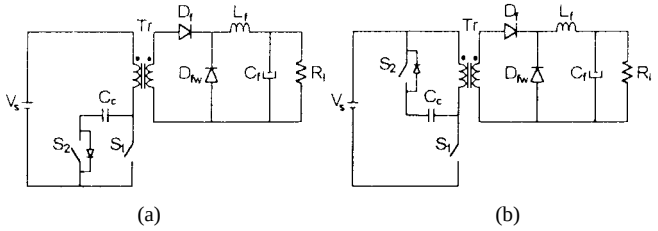

Fig. 1. (a) Forward converter with a transformer active reset circuit (1). (b) Forward converter with a transformer active reset circuit (2).

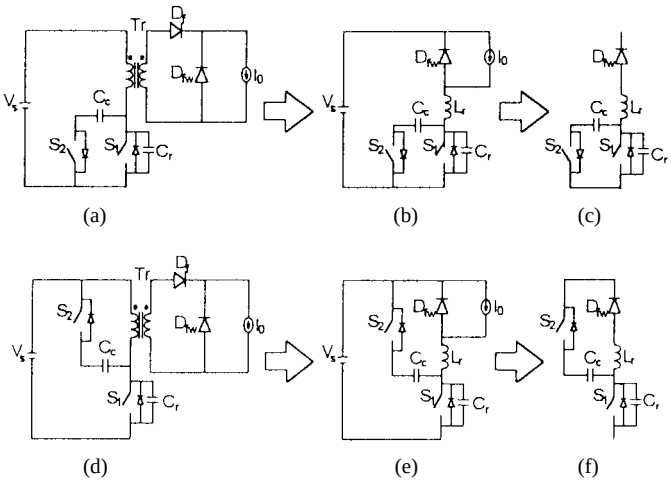

Fig. 2. (a) Clamped mode ZVS-PWM forward converter (boost). (b) Clamped mode ZVS-PWM Buck converter (boost). (c) The ZVS-PWM commutation cell (boost) taken from the buck converter. (d) Clamped Mode ZVS-PWM forward converter (buck-boost). (e) Clamped mode ZVS-PWM Buck converter (buck-boost). (f) The ZVS-PWM commutation cell (buck-boost) taken from the Buck converter.

II. Generation of the New Family of Converters

A. Generation of Six Fundamental Clamped Mode ZVS-PWM Cells

Let us consider the Fig. 2, where two ZVS-PWM commutation cells are obtained. From the two Forward converters shown in Fig. 2(a) and (d) it is possible to derive two Buck converters as shown in Fig. 2(b) and (e), and, from these converters, like in Hard-switched PWM converters, it is possible

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C. M. C. Duarte is with the Engineering School, UCPel-Catholic University of Pelotas, 96010-000-Pelotas-RS, Brazil.

I. Barbi is with the Power Electronics Institute-INEP, Federal University of Santa Catarina, 88040-970-Florianópolis-SC, Brazil.

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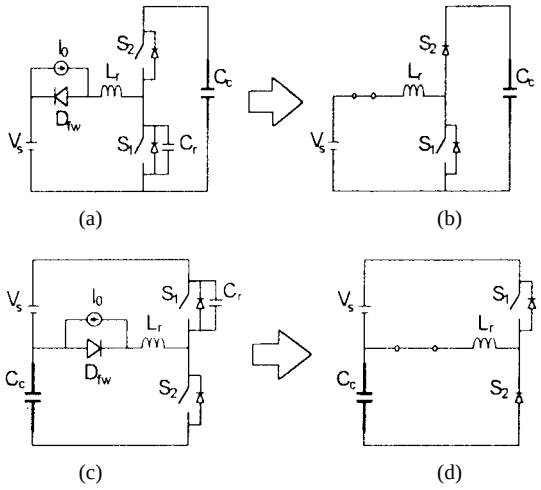


Fig. 3. (a) Buck-boost converter. (b) Boost clamping circuit. (c) Buck-buck-boost converter. (d) Buck-boost clamping circuit.

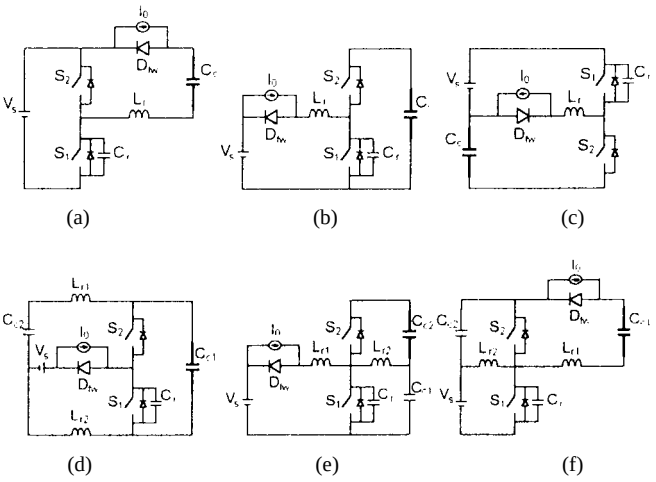


Fig. 4. Clamped Mode ZVS-PWM Buck converters. (a) Buck-buck. (b) Buck-boost. (c) Buck-buck-boost. (d) Buck-cuk. (e) Buck-sepic. (f) Buck-zeta.

to isolate the fundamental commutation cells, as shown in Fig. 2(c) and (f).

If we draw the circuits shown in Fig. 2(b) and 2(e) in a different way [Fig. 3(a) and 3(c)], so that clamping capacitors are put in evidence, it can be noticed that they are charged by a boost stage (Fig. 3(b) or by a buck-boost stage [Fig. 3(d)]. In this way, according to the converter shown in Fig. 3(a), the power transferred to the load is processed by a buck stage, while the clamping action is performed by a boost stage and, in the converter shown in Fig. 3(c), the clamping action is performed by a buck-boost stage, while the power transferred to the load is processed by a buck stage too. For the same buck based power transfer, six clamped circuits, namely Buck, Boost, Buck-boost, Cuk, Sepic, and Zeta can be employed; they are shown in Fig. 4. Therefore, these circuits will be named for Buck-buck [Fig. 4(a)], Buck-boost [Fig. 4(b)], Buck-buck-boost [Fig. 4(c)], Buck-cuk [Fig. 4(d)], Buck-sepic [Fig. 4(e)], and Buck-zeta [Fig. 4(f)]. These circuits, when drawn in a different way, as shown in Fig. 5, lead to the identification of the fundamental ZVS-PWM cells. The new cells are represented in Fig. 6.

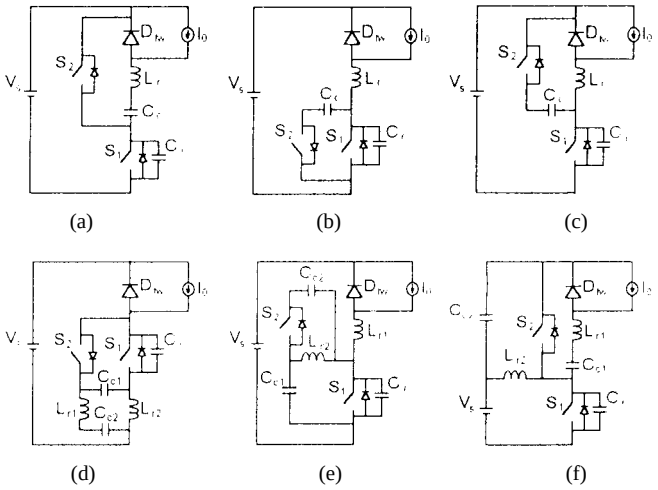


Fig. 5. Clamped Mode ZVS-PWM Buck converters. (a) Buck-buck. (b) Buck-boost. (c) Buck-buck-boost. (d) Buck-cuk. (e) Buck-sepic. (f) Buck-zeta.

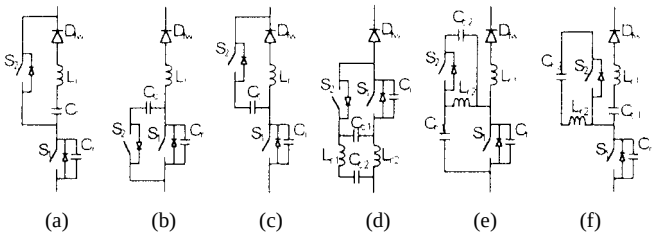


Fig. 6. Fundamental ZVS-PWM cells. (a) Buck clamping action. (b) Boost clamping action. (c) Buck-boost clamping action. (d) Cuk clamping action. (e) Sepic clamping action. (f) Zeta clamping action.

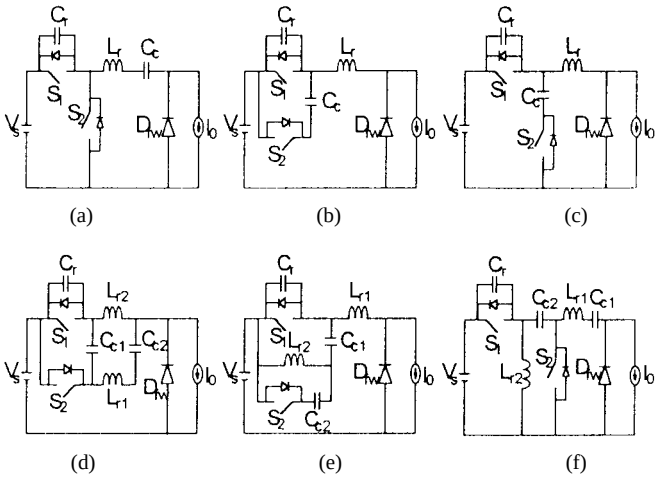


Fig. 7. (a) Buck-buck. (b) Buck-boost. (c) Buck-buck-boost. (d) Buck-cuk. (e) Buck-sepic. (f) Buck-zeta.

B. Generation of the Family of New Converters

Each of the commutation cells identified above by a proper connection of voltage and current sources generates six non-isolated circuits. Therefore, using this systematic approach, 36 topologies are obtained, divided in six groups according to their power transfer principle. Then, to help the understanding of this approach, the same group composed of six Buck converters is shown in Fig. 7. In Fig. 7, the circuits are drawn in a more usual way as to become easier the identification of the Buck converter. The Boost converters are shown in Fig. 8,

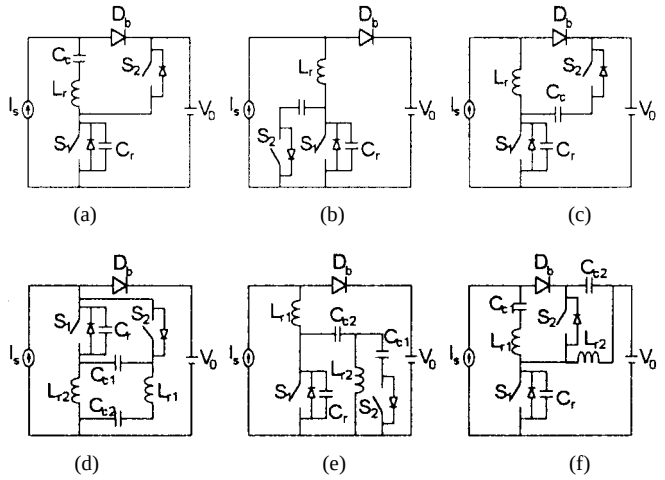


Fig. 8. (a) Boost-buck. (b) Boost-boost. (c) Boost-buck-boost. (d) Boost-cuk. (e) Boost-sepic. (f) Boost-zeta.

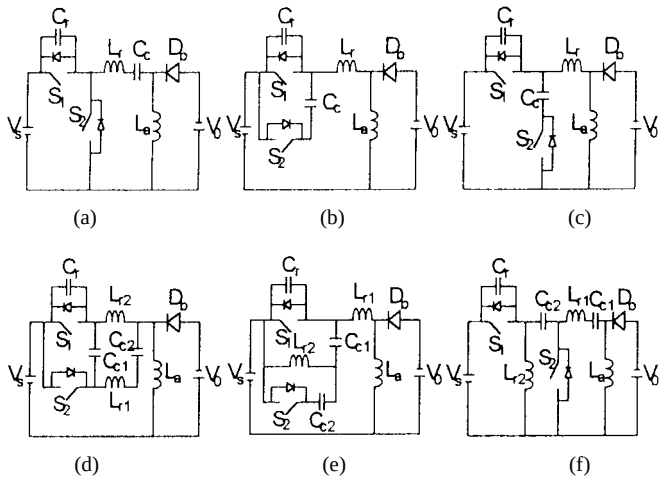


Fig. 9. (a) Buck-boost-buck. (b) Buck-boost-boost. (c) Buck-boost-buck-boost. (d) Buck-boost-cuk. (e) Buck-boost-sepic. (f) Buck-boost-zeta.

the Buck-boost converters, in Fig. 9, the Cuk converters, in Fig. 10, the Sepic converters, in Fig. 11, and the Zeta converters, in Fig. 12.

In the following sections, the Buck-buck-boost converter shown in Figs. 4(c), 5(c), and 7(c) is taken as an example to illustrate the operation of this family.

III. Operation and Analysis of the Buck-Buck-Boost Converter

This converter differs from a conventional Buck PWM converter by an additional auxiliary switch (S_2), a resonant inductor (L_r), a resonant capacitor (C_r), which includes the output capacitance of the power switch, and a clamping capacitor (C_c). S_1 is the main switch which is responsible for the power transferred to the load.

A. Principle of Operation

To simplify the analysis, the output filter inductance is assumed large enough to be considered as a current source (I_0).

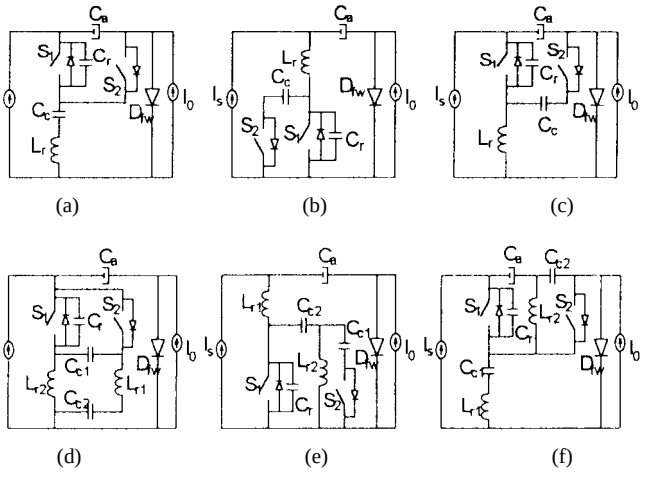


Fig. 10. (a) Cuk-buck. (b) Cuk-boost. (c) Cuk-buck-boost. (d) Cuk-cuk; (e) Cuk-sepic. (f) Cuk-zeta.

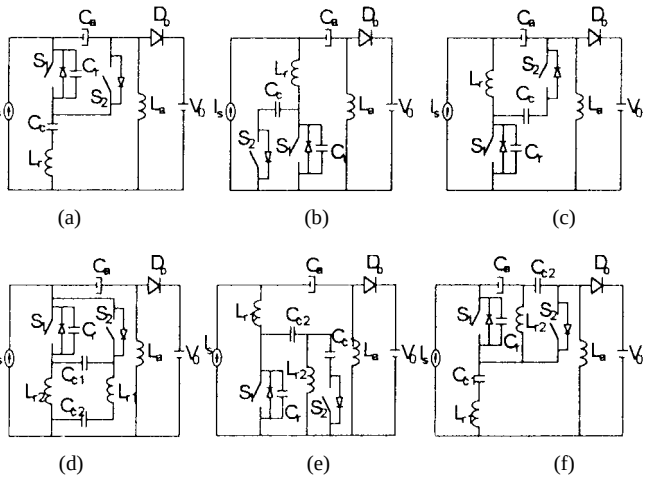


Fig. 11. (a) Sepic-buck. (b) Sepic-boost. (c) Sepic-buck-boost. (d) Sepic-cuk. (e) Sepic-sepic. (f) Sepic-zeta.

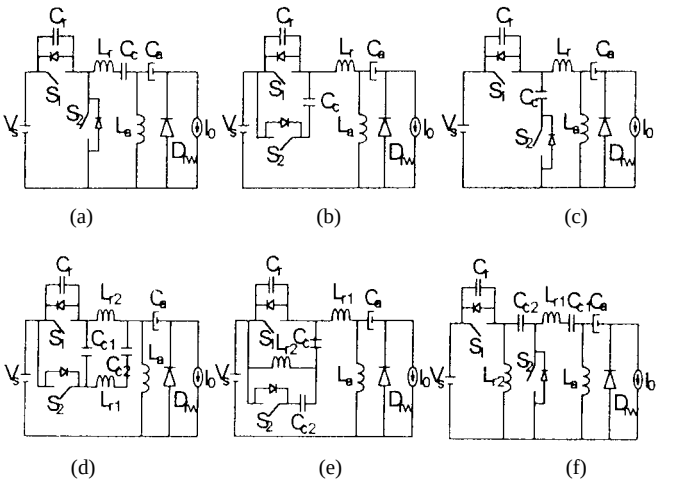


Fig. 12. (a) Zeta-buck. (b) Zeta-boost. (c) Zeta-buck-boost. (d) Zeta-cuk. (e) Zeta-sepic. (f) Zeta-zeta.

The capacitor C_c is selected to have a large capacitance so that the voltage V_c across its terminals could be considered as a constant one. The six topological stages and key waveforms

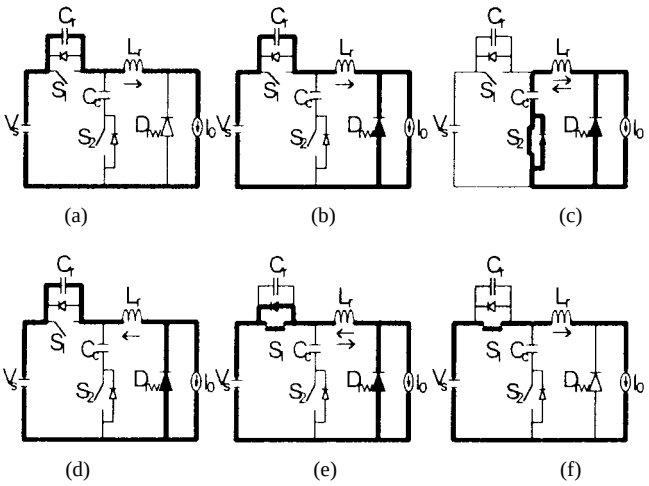


Fig. 13. Topological stages assumed by Buck-buck-boost converter.

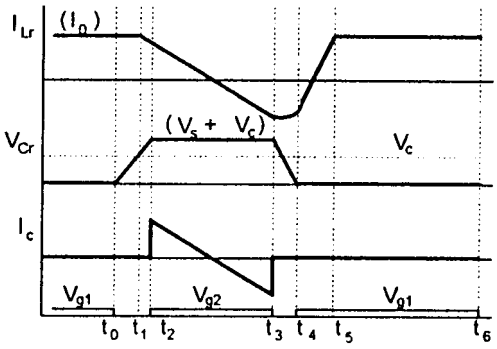


Fig. 14. Relevant ideal waveforms.

of the Buck-buck-boost converter to one switching cycle are shown in Figs. 13 and 14. In those figures, it can be seen that the two switches are switched in a complementary way. The main switch (S_1) is turned off at $t = t_0$, when the switching period starts.

Stage 1 (t_0, t_1)*, Fig. 13(a):* Prior to t_0, the main switch (S_1) is on and the auxiliary switch is off. When S_1 is turned off, at $t = t_1$, the capacitor C_r is linearly charged by I_0, to V_s. Due to the presence of C_r, S_1 is turned off with no switching losses. This stage ends when $V_{Cr}(t) = V_s$.

Stage 2 (t_1, t_2)*, Fig. 13(b):* When V_{Cr} reaches V_s, the free-wheeling diode (D_{fw}) starts conducting. The current through L_r and V_{Cr} evolves in a resonant way and V_{Cr} rises from V_s up to $V_c + V_s$. After that, the voltages are clamped. This stage ends when $V_{Cr}(t) = V_s + V_c$.

Stage 3 (t_2, t_3)*, Fig. 13(c):* As $V_{Cr}(t) = V_c + V_s$, the voltage across S_2 is zero, thus S_2 turns on with no losses (ZVS). The L_r current ramps down until it reaches zero, when it changes its direction and rises again. This stage ends when S_2 is turned off at $t = t_3$. Due to the presence of C_r, S_2 is turned off with no switching losses.

Stage 4 (t_3, t_4)*, Fig. 13(d):* The voltage across C_r falls, due to the resonance between L_r and C_r, until it reaches zero at $t = t_4$, when this stage ends.

Stage 5 (t_4, t_5)*, Fig. 13(e):* In stage 5, S_1 is turned on with no switching losses (ZVS) because V_{Cr} became null. The current through L_r changes its polarity and ramps up to reach I_0. This stage ends when $I_{Lr}(t) = I_0$.

Stage 6 (t_5, t_6)*, Fig. 13(f):* At $t = t_5$, the diode D_{fw} becomes reversibly biased and power is transferred to the load. This stage ends when S_1 is turned off at the end of the switching cycle.

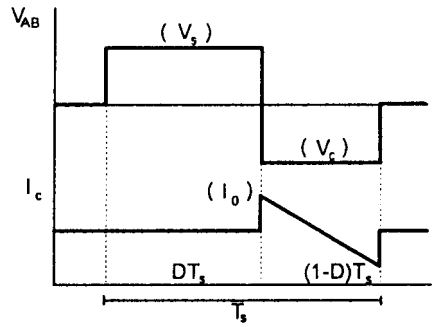


Fig. 15. Current through C_c and voltage across points **A** and **B**.

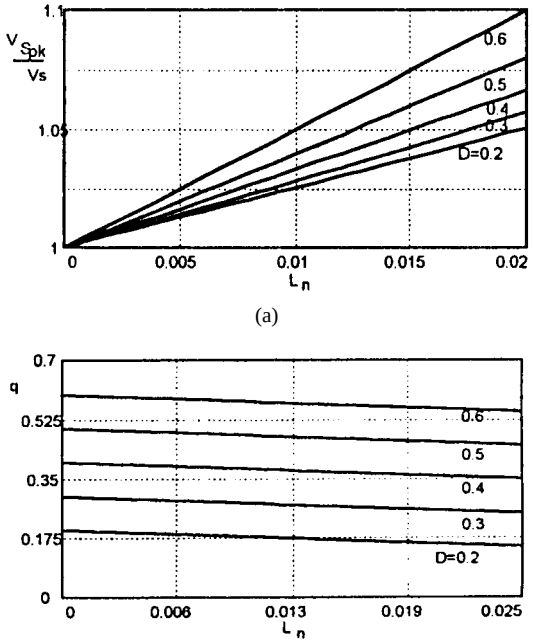


Fig. 16. (a) Theoretical dc voltage clamping ratio across switches. (b) Theoretical dc voltage conversion ratio.

B. DC Voltage Conversion Ratio and DC Voltage Clamping Ratio

As the time intervals $\Delta t_1, \Delta t_2$ and Δt_4 are very short in relation to the switching cycle, they will not be considered in this analysis. Thus, let us consider the current waveform shown in Fig. 15.

The power that flows in the clamping capacitor must be zero in a switching cycle, for the operation being steady. The voltage across C_c is constant so its average current must be zero. Thus

$$\int_0^{(1-D)T_s} \left[\frac{-V_c}{L_r}t + I_0\right] dt = 0 \qquad (1)$$

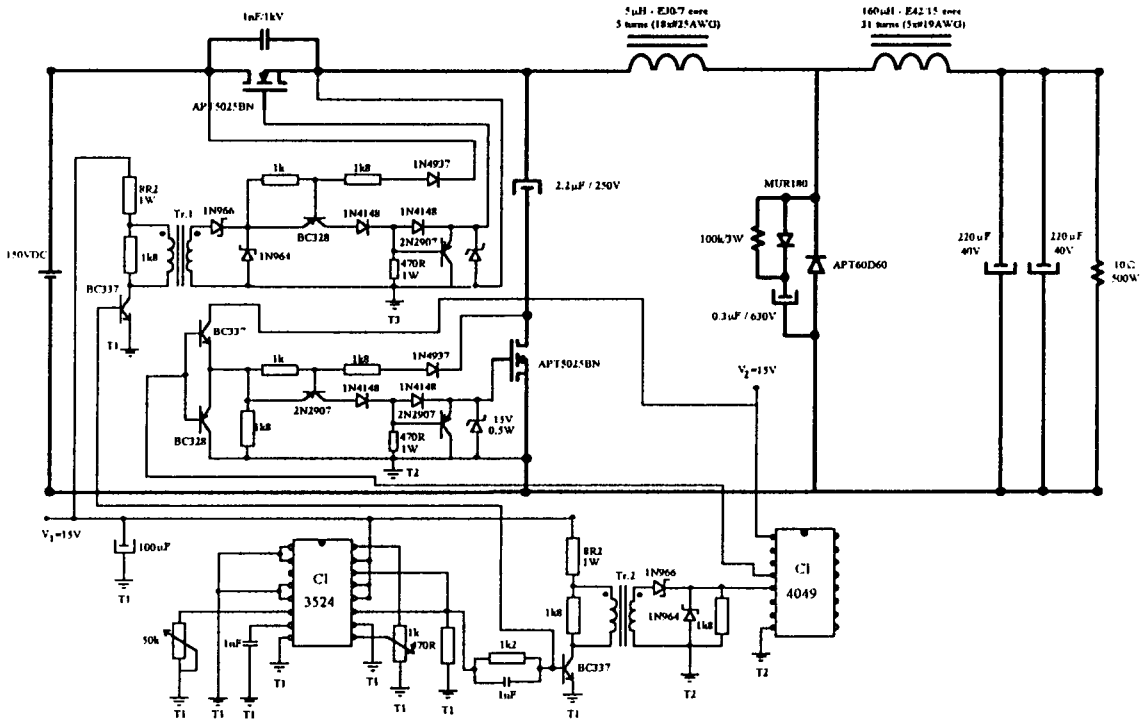


Fig. 17. Complete circuit of the implemented prototype.

then

$$\beta = \frac{V_c}{V_s} = \frac{2L_n}{(1-D)} \tag{2}$$

$$\frac{V_{S_{Pk}}}{V_s} = \beta + 1 = 1 + \frac{2L_n}{(1-D)}. \tag{3}$$

From Fig. 15 (voltage waveform), we know that

$$q = \frac{V_0}{V_s} = \frac{V_{\mathrm{AB}}}{V_s} = D - (1-D)\frac{V_c}{V_s} \tag{4}$$

then

$$q = \frac{V_0}{V_s} = D - 2L_n \tag{5}$$

where

$$L_n = L_r \frac{I_0}{V_s T_s} \tag{6}$$

and V_{Spk} is the maximum voltage across S_1 and S_2.

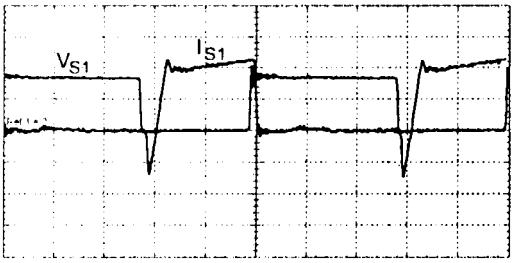
The dc voltage clamping ratio given by (03) is graphically represented in Fig. 16(a), and the dc voltage conversion ratio (q) is shown in Fig. 16(b), for different duty cycles (D).

IV. Experimental Results of Buck-Buck-Boost Converter

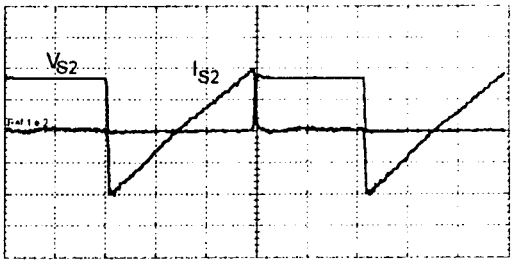
A Buck-buck-boost converter was implemented, with the following specifications:

1) output power $P = 500$ W and switching frequency $f_s = 100$ kHz;
2) input voltage $V_s = 150$ V and output voltage $V_0 = 50$ V.

The complete circuit diagram of the converter is shown in Fig. 17 and experimentally obtained waveforms of the switches current and drain-to-source voltages are shown in Fig. 18.



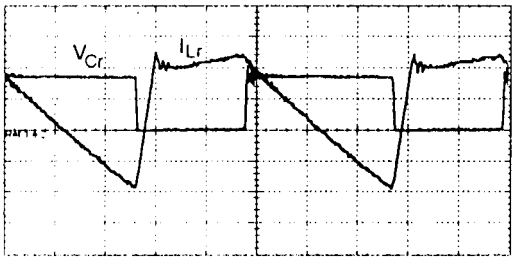
(a)



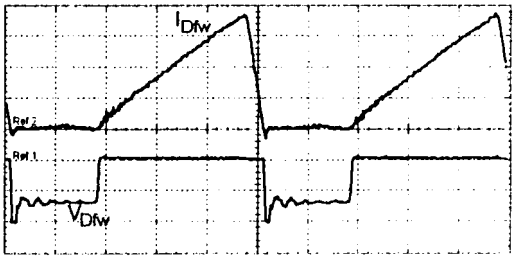
(b)

Fig. 18. (a) Drain-to-source voltage across S_1 and current through S_1 and C_r. (b) Drain-to-source voltage across S_2 and current through S_2; (voltage: 100 V/div; current: 5 A/div; time scale: 2 μs/div).

The resonant inductor current and the voltage across the resonant capacitor are shown in Fig. 19(a), while the current through the diode D_{fw} and the voltage across that diode are shown in Fig. 19(b). These waveforms agree with those theoretically predicted, and, as it can be noted from the waveforms shown in Fig. 18, the main switches (S_1 and S_2) present ZVS commutation and their voltages are clamped at a specified value. The load range with integral soft commutation in S_1, obtained experimentally, was from 29.2 to 100% of full load.

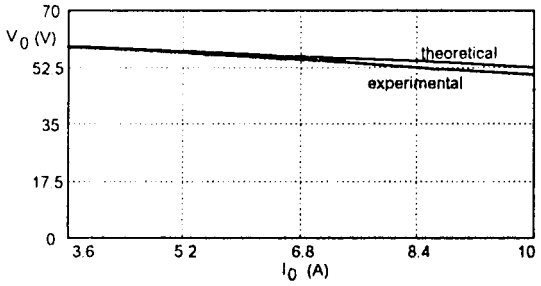


(a)

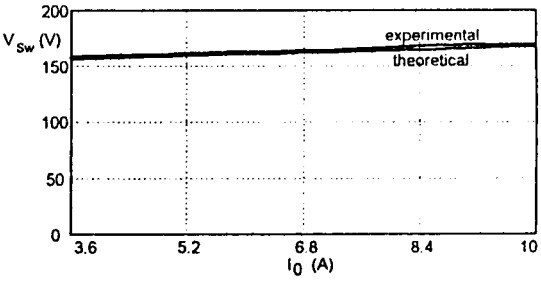


(b)

Fig. 19. (a) Voltage across C_r and current through L_r. (b) Voltage across D_{fw} and current through D_{fw}; (voltage: 100 V/div; current: 5 A/div; time scale: 2 μs/div).



(a)



(b)

Fig. 20. (a) Theoretically and experimentally obtained output voltage. (b) Maximum voltage across switches with different load conditions and nominal duty cycle.

In Fig. 20, the output voltage theoretically and experimentally obtained, as a function of output current can be noted, as well as the maximum voltage across switches, for the same conditions. The experimental efficiency curve of the converter is shown in Fig. 21. The experimental results are therefore in agreement with the results predicted theoretically.

V. Conclusion

This paper presented a technique to generate a complete family of ZVS-PWM Active-Clamping dc-to-dc Converters.

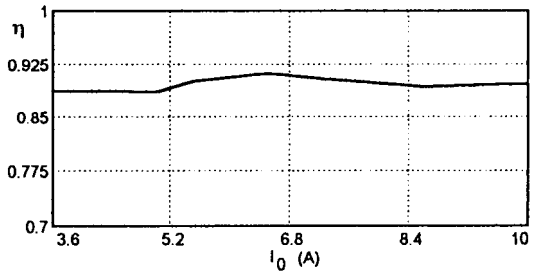


Fig. 21. Experimental curve of efficiency with different load conditions and nominal duty cycle.

With this technique it is possible to generate 36 nonisolated topologies, where the most of them are new. Those topologies were derived in a comprehensive form, and one Buck converter was analyzed as an example.

Theoretical studies and experimental results lead us to the following conclusions:

1) soft-commutation (ZVS) is achieved for the active switches;
2) the converters are regulated by the conventional PWM technique, at constant frequency;
3) under the studied conditions the converters presented high efficiency in a wide load range.

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Cláudio Manoel C. Duarte (S'94) was born in Pelotas, Rio Grande do Sul, Brazil, in 1960. He received the B.S. degree in 1982 from the Catholic University of Pelotas-UCPel, Pelotas(RS), Brazil, and the M.S. degree in 1993 from the Federal University of Santa Catarina, Florianópolis(SC), Brazil, both in electrical engineering.

From August 1983 to 1994, he was Assistant Professor, and, since March 1994, has been an Adjunct Professor with the Department of Electrical Engineering, Catholic University of Pelotas. He is currently working towards the Ph.D. degree in electrical engineering at the Power Electronics Institute of Federal University of Santa Catarina. His interests include soft-switching techniques, dc/dc converters, and power factor correction techniques.

Ivo Barbi (M'78–SM'90) was born in Gaspar, Santa Catarina, Brazil, in 1949. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina, Brazil, in 1973 and 1976, respectively, and the Ph.D. degree from the Polytechnic National Institute of Toulouse, France, in 1979.

He founded the Brazilian Power Electronics Society and the Power Electronics Institute of the Federal University of Santa Catarina, where he currently works as a Professor.

Dr. Barbi was an Associate Editor in the Power Converters area of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS from 1992 to 1996.