A New Technique for Parallel Connection of Commutation Cells: Analysis, Design, and Experimentation

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***Abstract*— A new technique useful for parallel connection of commutation cells is introduced in this paper. It consists of using small inductances in order to ensure dynamic and static share of the commutated current among the different switches. Operation principle, theoretical analysis, and design procedure are presented. Experimental results, obtained from a 400-W buck prototype using two commutation cells, have been used to validate the theoretical analysis and demonstrate the effectiveness of the proposed technique. Several experiments have been also accomplished to clear up the advantages of this new technique in comparison to the conventional one. Results from a three-cell buck dc–dc converter delivering 4.5 kW are also presented, revealing a balanced current sharing among cells and an excellent dynamic behavior, as foreseen in the theoretical analysis.**

I. Introduction

ALTHOUGH the last decades have witnessed a great development in the power semiconductors field, power electronics designer frequently deals with high power applications for which no actual switch is feasible. A similar situation may occur when budget directives restrict the use of high rating switches. If the application involves high currents, the most common solution consists of paralleling a suitable number of devices. This procedure is very simple but it is device dependent. This means that for each kind of switch there is a set of recommendations that must be observed, otherwise a reasonable distribution of total current among the chosen number of cells will not be met (for both, dynamic and static conditions). In the following is a small list of important procedures, considering several device technologies, which are employed to make this technique possible:

- establishment of a good driving circuit;
- introduction of small inductors in series with the switches;
- choice of paired devices (for both, dynamic and static parameters);
- minimization of wiring imbalance (layout optimization).

During the last few years a number of alternative solutions to the conventional paralleling technique have arisen in the technical literature. An important method has shown the possibility of increasing the power capability of an inverter by means of current sharing reactors [1]. Using this technique one can implement a multiphase inverter using only an even number of parallel devices. Another alternative allows great output power by connecting any number of inverters in parallel (also using sharing reactors) [2]. Several power semiconductor industries are now working to produce power modules that meet almost all the conditions described above [3], [4]. However, those solutions are normally very expensive and commonly determine a special design conducted by the semiconductor maker.

Manuscript received November 16, 1995; revised September 3, 1996. This paper was presented at IEEE PESC'95.

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Publisher Item Identifier S 0885-8993(97)01843-7.

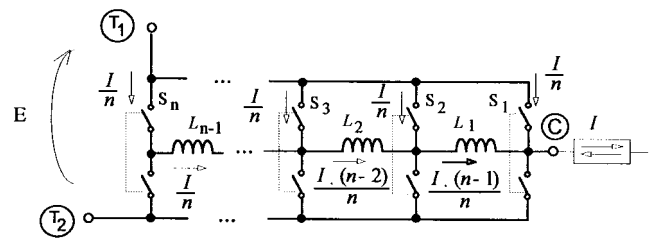

Fig. 1. Generic cell for the new paralleling technique.

This paper shows that it is possible to make any number of pulse width modulation (PWM) cells share the total current of a converter by using small balance inductors, as shown in Fig. 1. Each inductor has its specific (and fixed) current level, assuming a continuous conduction situation with negligible ripple. The other conditions that must be observed to make this assumption true will be listed in the next section. This figure also presents the expected ideal values of the peak steady-state currents related to each branch of the generalized cell. These quantities, as well as the n current levels, will be proved in the subsequent sections. In the meanwhile, it can be concluded by inspection that each switch current depends only on the two inductor currents to which it is connected. Dotted lines in Fig. 1 represent the complementary relationship between two switches of an individual cell. Depending on the nature of the current source at point C, S_n cell can have different arrangements. For a bidirectional source the cell will be implemented with two active switches (IGBT's, MOSFET's, etc.), while for a unidirectional source it must be designed with an active and a passive switch (diode).

As for a single PWM switch the new paralleling generic cell has two points to which a voltage source, or a capacitive branch, should be connected (T_1 and T_2) and one point

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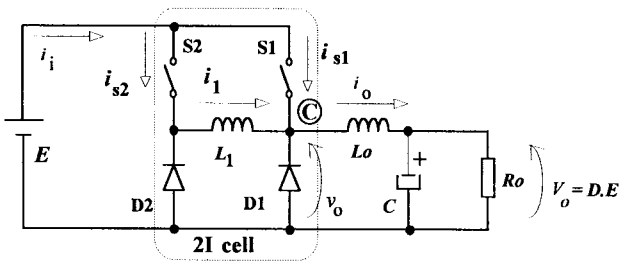


Fig. 2. DC–DC 2I buck converter.

to which a current source or an inductive loop should be connected (the common point C). According to the current quantities of Fig. 1, the peak value of the steady-state current for each individual switch is the output current divided by the number of used cells. This statement and another details of this new structure are going to be explained in the next sections.

II. Principle of Operation

Fig. 2 shows the application of the new technique to a buck dc–dc converter, using two parallel PWM switches. This circuit is going to be named "2I buck," because two cells have been used to share the total (output) current. To simplify the analysis, one may consider that:

- S_1 and S_2 are gated by the same PWM signal of duty cycle D;
- all the switches are represented by small single resistances, r;
- inductor currents are in continuous conduction mode, assumed ripple free in this section.

Some conclusions can be stated by simple inspection of Fig. 2. The cell formed by S_1–D_1 acts in such a way that the output characteristics are the same as those found in a conventional buck converter. For this reason, the output circuit at node C can be considered a dc current source. Moreover, due to the employed gate strategy and continuous conduction current, L_1 is always in series with a switch and this branch is in parallel with another switch. The output of this parallel circuit is always attached to a dc current source at point C. Then, due to a well-known linear circuit ruler, L_1 can be assumed to have no dc drop voltage, what leads to a balanced current distribution between any couple of devices (since they have the same impedance). Therefore, L_1 acts as a current source having the half of the output current. This important feature makes a great difference when comparing the procedure above with the conventional parallel technique. In the present case, an eventual lag in turn-on or turn-off of any switch never allows another device to support total output current. The situation explained here is represented by the equivalent circuit of Fig. 3(a), which is useful for describing the current distribution at steady-state among the significant branches. Using the same procedure one can obtain the generic simplified equivalent circuit, as shown in Fig. 3(b). Such a circuit can be easily used to prove the generic intermediate voltage levels stated in Fig. 1.

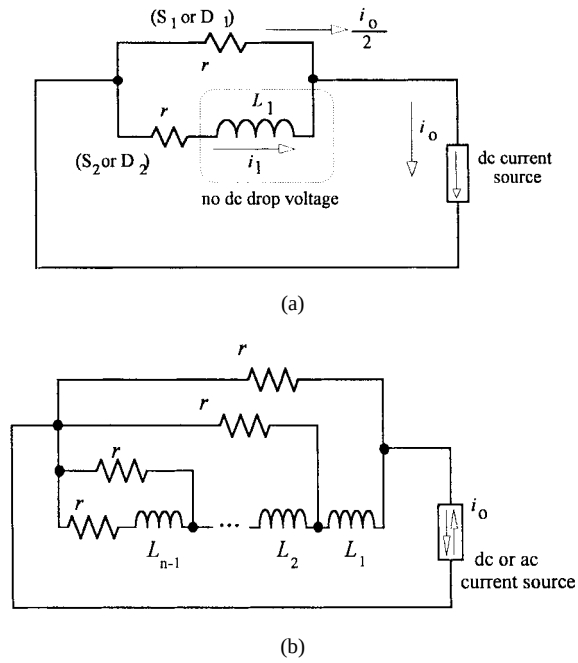


Fig. 3. Simplified equivalent circuit for: (a) 2I buck and (b) generic structure.

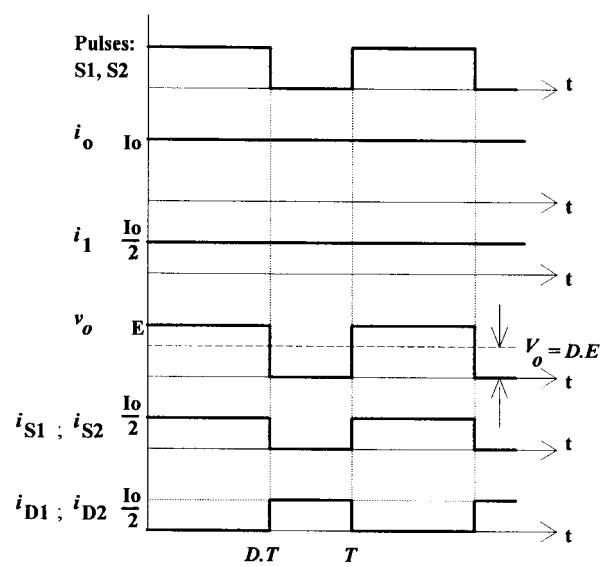


Fig. 4. Selected basic ideal waveforms.

The previous simplified analysis did not take into account the series resistance of the balance inductor. If this parameter assumes a small value when compared to the device on-resistances it has a negligible effect in current distribution. In fact, it is possible to have an inductor resistance as small as 2 mΩ, which is less than 5% of a conventional switch resistance. In the same way, device threshold voltages have not been taken into account too. A deeper discussion about the influence of those parameters takes place at the end of Section V.

Fig. 4 shows the expected ideal waveforms based on the simplified assumptions, which have been made for the circuit of Fig. 2. Note that the output current, i_o, has been assumed a constant dc current, I_o. The average value of output voltage, v_o, has been named V_o.

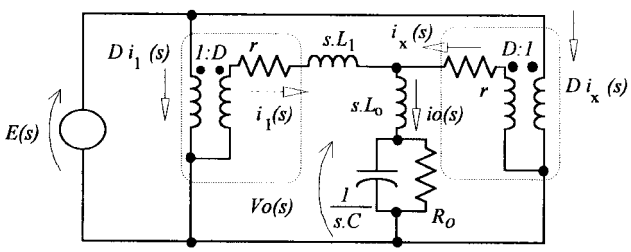


Fig. 5. Line-to-output model for 2I buck converter.

III. Mathematical Modeling and Computer Simulation

A quantitative analysis of the new technique can be achieved by using some kind of switching converter modeling method. A satisfactory approach is found in [5] consisting on a small-signal linear model, and due to its simplicity it is going to be adopted here. Since no closed-loop control is concerned to the new technique (at least on the current distribution viewpoint), suitable information can be drawn by using the line-to-output circuit model. Fig. 5 employs this concept and shows the equivalent circuit of Fig. 2, in which the PWM cells have been substituted by their "PWM switch models." In this figure, the dashed lines indicate the models for the PWM cells with inclusion of device resistances. Here, the parameter r is a "time-average" value of the active and passive switch resistance and stands for a more accurate model [5].

Finally, the circuit of Fig. 5 can be solved for the output and balance inductor currents. These parameters constitute the minimum set of variables that stands for a good perception of the current distribution. Using conventional circuit laws one can eliminate the auxiliar variables $V_o(s)$ and $i_x(s)$ and write

$$i_1(s) = i_o(s) - \frac{DE(s) - i_o(s)\left[sL_o + \left(\frac{R}{RCs+1}\right)\right]}{r} \quad (1)$$

$$i_1(s) = \frac{DE(s) - i_o(s)\left[sL_o + \left(\frac{R}{RCs+1}\right)\right]}{r + sL}. \quad (2)$$

Equations (1) and (2) have only two unknown variables: $i_1(s)$ and $i_o(s)$, because $E(s)$ is the input voltage. Thus, solving them simultaneously it is possible to find the transfer functions as follows:

$$\frac{i_o(s)}{E(s)} = \frac{(R_oCs+1)(2r+sL_1)D}{H(s)} \quad (3)$$

$$\frac{i_1(s)}{E(s)} = \frac{(R_oCs+1)rD}{H(s)} \quad (4)$$

where

$$\begin{aligned} H(s) = {} & L_1L_oCR_os^3 \\ & + (rL_1R_oC + L_1L_o + 2L_oCR_or)s^2 \\ & + (2L_or + rL_1 + r^2R_oC + R_oL_1)s \\ & + 2R_or + r^2. \end{aligned} \quad (5)$$

The equations above can be used to build up the time variations of interest variables. To simplify this task one may consider a null capacitor and disregard some terms assuming $r \ll R_o$. This consideration lead to neglecting in (3) the $r.L_1$ *and* r^2 terms, as well as the terms that include the C parameter. So, the time variations of i_o and i_1 for a voltage step input are

$$i_o(t) = \frac{DE}{R_o}\left[1 - e^{(-R_o/L_o)t}\right] \quad (6)$$

$$\begin{aligned} i_1(t) = {} & \frac{DE}{2R_o} + \frac{DE}{2rL_o - R_oL_1} \\ & \cdot \left[\frac{L_1}{2}e^{(-2r/L_1)t} - \frac{rL_o}{R_o}e^{(-R_o/L_o)t}\right]. \end{aligned} \quad (7)$$

A similar procedure can be carried out for the 3I buck converter, the one with three PWM cells. In this case two balance inductors should be used: L_1 and L_2, which are associated to the currents i_1 and i_2, respectively. To simplify algebraic manipulation L_1 has been made equal to L_2, and both equal to L. The final time variations of interest variables are

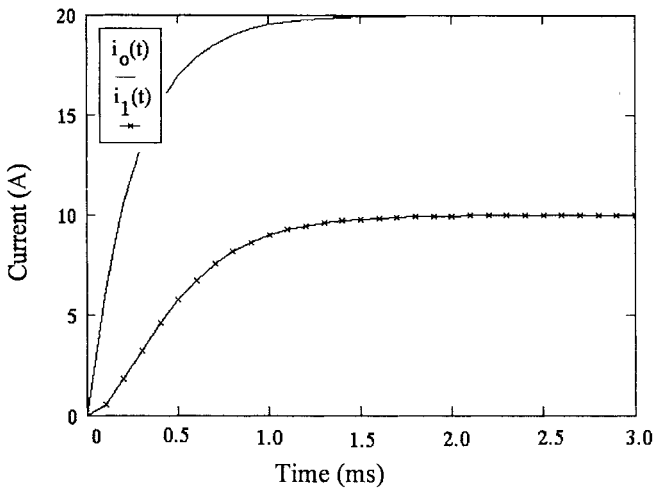
$$i_o(t) = \frac{DE}{R_o}\left[1 - e^{(-R_o/L_o)t}\right] \quad (8)$$

$$\begin{aligned} i_1(t) = {} & \frac{2}{3}\frac{DE}{R_o} + \frac{DE}{(3rL_o - R_oL)(rL_o - R_oL)} \\ & \cdot \left\{\frac{-(2rL_o - R_oL)rL_o}{R}e^{(-R_o/L_o)t}\right. \\ & + \frac{(3rL_o - R_oL)L}{2}e^{(-r/L)t} \\ & \left. + \frac{(rL_o - R_oL)L}{6}e^{(-3r/L)t}\right\} \end{aligned} \quad (9)$$

$$\begin{aligned} i_2(t) = {} & \frac{1}{3}\frac{D.E}{R_o} + \frac{D.E}{(3rL_o - R_oL)(rL_o - R_oL)} \\ & \cdot \left\{\frac{r^2L_o^2}{R}e^{(-R_o/L_o)t}\right. \\ & + \frac{(3rL_o - R_oL)L}{2}e^{(-r/L)t} \\ & \left. + \frac{(rL_o - R_oL)L}{6}e^{(-3r/L)t}\right\}. \end{aligned} \quad (10)$$

Equations (6)–(10) show that the output current does not depend on the internal parameters (like r, L_1, etc.) of the new converter. Moreover, steady-state quantities for i_1 and i_2 authenticate the ideal values predicted in last section for both 2I and 3I converters. It must be noted that, for each converter, a set of time constants define the time variations of the variables. Fig. 6(a) shows the graphical representation of the (4) and (5) (2I buck converter) considering $E = 50$ V, $f = 20$ kHz, $D = 0.6$; $L = 50\,\mu$H, $L_o = 400\,\mu$H, $r = 0,1\,\Omega$, and $R_o = 1,5\,\Omega$. On the other hand, Fig. 6(b) is concerned to the (8)–(10), thus for the 3I buck converter, using the same parameters.

Fig. 7 shows the digital simulation results carried out for the 2I buck converter, using the same parameters of Fig. 6. It reveals a good agreement between these waveforms and those obtained from mathematical modeling, meaning that the simplified considerations did not cause any drawback to the adopted model. Furthermore, Fig. 7(b) reveals a good current distribution among devices, what agrees with the ideal sketch of Fig. 4. It can also be noted that the PWM cell closer to the output node (S_1-D_1) assumes part of the output current ripple, having a slight different peak current value.



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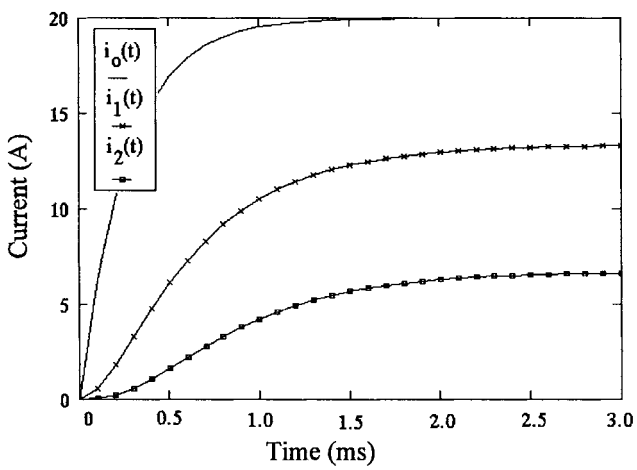
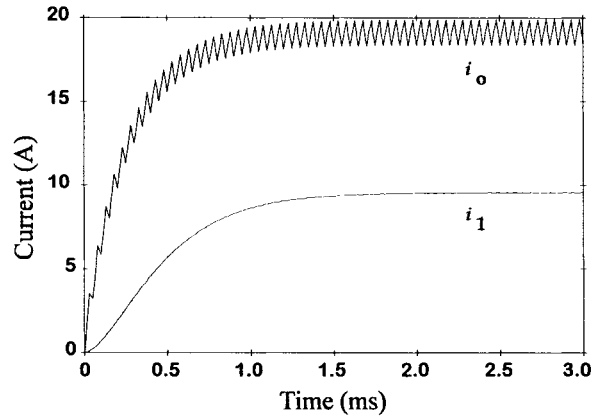
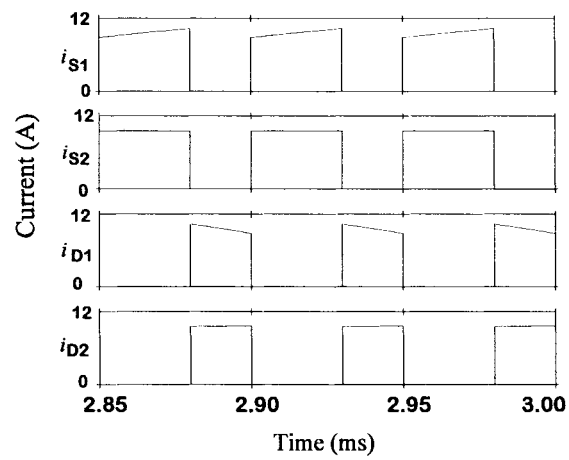


(b)

Fig. 6. Voltage-step response for: (a) 2I buck converter and (b) 3I buck converter ($E = 50$ V, $f = 20$ kHz, $D = 0.6$; $L = 50\,\mu$H, $L_o = 400\,\mu$H, $r = 0,1\,\Omega$, and $R_o = 1,5\,\Omega$).



(a)



(b)

Fig. 7. Simulation results for 2I buck converter using the same parameters of Fig. 6: (a) voltage-step response and (b) steady-state devices current comparison.

IV. Design Considerations

The last results have shown that the new technique owns a useful set of modeling equations, enabling anyone to predict the circuit behavior and to choose design rules.

In fact, the design procedure have much in common with conventional switching regulator design. The most significant difference consists in choosing appropriate balance inductors. This task grounds on searching of suitable inductances that restricts current ripple in the presence of nonideal device switching parameters. Therefore, the choice of balance inductors must take into account the following parameters:

- maximum applied voltage, E;
- maximum spread on turn-off and turn-on devices parameters, Δt;
- maximum balance inductors current ripple, Δi.

At this point the well-known inductance electric rule can be adapted to determine the appropriate value of the balance inductances:

$$L = \frac{E.\Delta t}{\Delta i}. \tag{11}$$

Parameter Δt is not so simple to be determined because common devices data books do not bring up this information. Although some semiconductor makers inform minimum, typical, and maximum expected switching parameters, these numbers cannot have a strict consideration, since they involve a great amount of components. In other words, from a same set of commercial devices the switching parameters spread is too small, allowing a more economic and appropriate design.

Even though (11) ensures a desired ripple over balance inductor current, it does not guarantee the same for the device currents, since they also depend on the output current. This is true specially for those switches near the output node. So, it is important to limit the output current ripple at a reasonable value, in order to reduce divergences on device peak currents (if these differences play an important role on the converter safety, i.e., when the devices work near their absolute maximum ratings).

It must also be noted that each balance inductor have its own current level. If it is necessary a more economic design it is possible to choose smaller inductances for higher level currents (in the case of the n-level converter), in order to get the same relative ripple on all inductors. However, there is no problem if one adopts the same inductance value for all

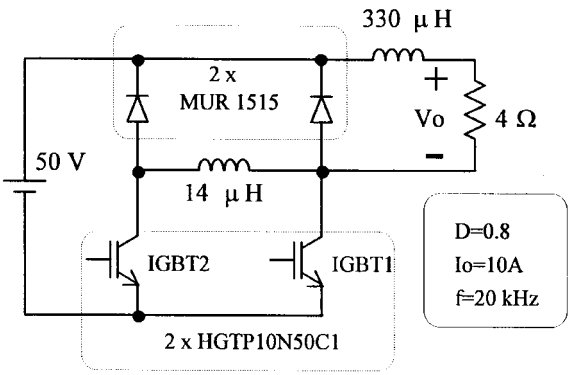


Fig. 8. Laboratory circuit.

inductors. In this case, the design must be carried out using the minimum current level, I_o/n.

V. Laboratory Verification

In order to check up the statements and conclusions of the last two sections a laboratory prototype, of a 2I buck converter, has been implemented using the following parameters: $E = 50$ V; $f = 20$ kHz; $D = 0.8$; $L_o = 330\,\mu$H; $R_o = 4\,\Omega$. These values determine a 10-A output current and a 5-A balance inductor current. IGBT's HGTP10N50C1, from Harris Co., have been chosen as active switches and previous tests revealed that they had a 60-ns maximum spread of switching parameters. Allowing a 5% current ripple over the balance inductor, (11) leads to a 12-μH inductor. A 14-H inductor has been used, which stands for a smaller ripple. Fig. 8 shows more details of this circuit including the device specifications.

Fig. 9 shows the basic selected waveforms that must be compared to the ones in Fig. 4. Clearly, these waveforms validate the theoretical assumptions stated in the last sections. The waveforms of Fig. 9 also show that the new technique has allowed a good current distribution among devices.

Fig. 10 shows the transient response of inductor currents due to a step in input voltage. Note that this figure presents a great similarity to Figs. 6(a) and 7(a), despite their different current levels.

In order to verify the performance of the circuit, on the dynamic viewpoint, under more uncomfortable conditions, a small inductance of 100 nH has been introduced in the emitter of transistor S_1. This emulates a very common situation, where a wiring imbalance can even damage a device in a conventional parallel circuit [6]. The same parameters of Fig. 8 have been used. Fig. 11 confronts collector currents of transistors for $L_1 = 0$ (conventional paralleling technique) and $L_1 = 14\,\mu$H, respectively. Note that transistor S_2 is under a worse condition than transistor S_1, since it conducts first. Another situation has been created by generating two nonsimultaneous gate pulses. In this case, the gate pulse to S_2 has been delayed at turn-on by 300 ns and at turn-off by 200 ns. Waveforms equivalent to those of Fig. 11 are shown in Fig. 12.

Figs. 11 and 12 show that the new technique has an improved dynamic current balance characteristic. This means that even during transient stage the switch currents do not reach destructive peaks. However, as for the conventional parallel technique, steady-state performance depends on the use of devices having close on-state behaviors (on-resistance for MOSFET, threshold voltage for IGBT, etc.) to ensure a good current balance. The last experiments have been conducted using different device technologies (and ratings) and no steady-state imbalance has been observed for the same lot of components. Some recent works have shown that a parallel-connection imbalance (at steady state) can be considered a low-power phenomenon, at least for the IGBT device [7]. That is to say, under full load (when a device works near its absolute maximum rating of current) the current distribution imbalance tends to be negligible. Of course it is advisable to place all semiconductor components on the same heatsink in order to achieve a tight thermal feedback.

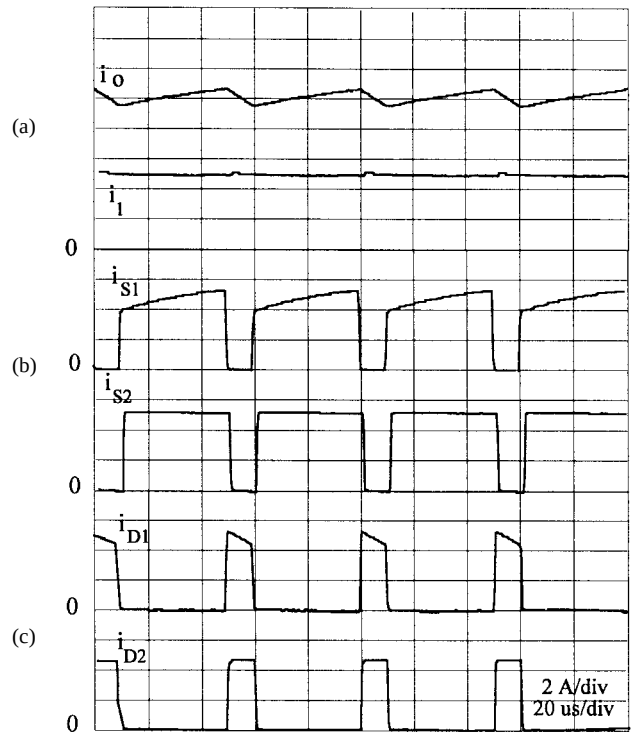


Fig. 9. Experimental selected waveforms for the 2I buck converter: (a) inductor currents, (b) IGBT collector currents, and (c) diode currents.

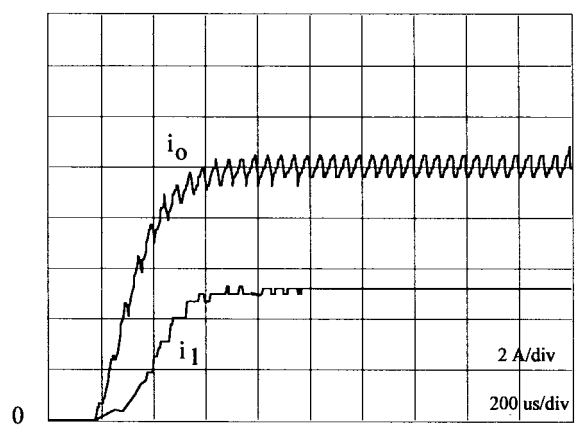
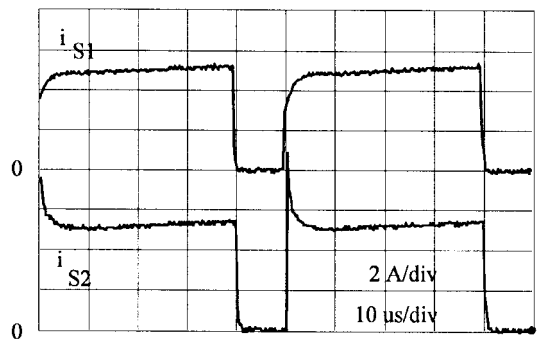
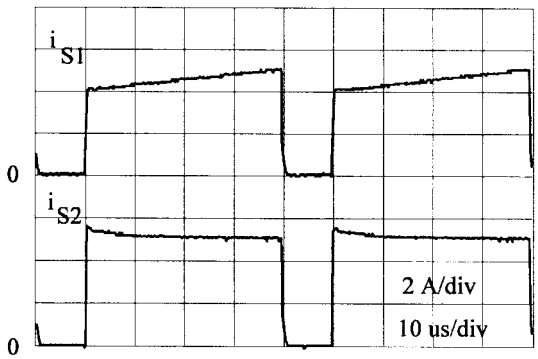


Fig. 10. Step-voltage response for the 2I-buck converter.

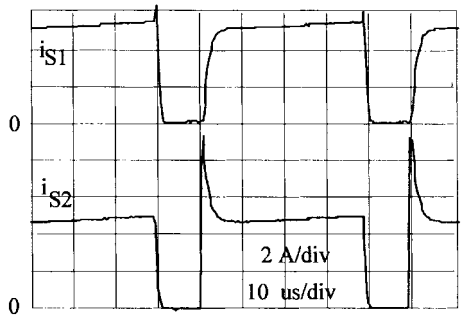


(a)



(b)

Fig. 11. Unbalanced emitter-ground experiment: (a) collector currents for $L_1 = 0$ and (b) collector currents for $L_1 = 14\,\mu$H.



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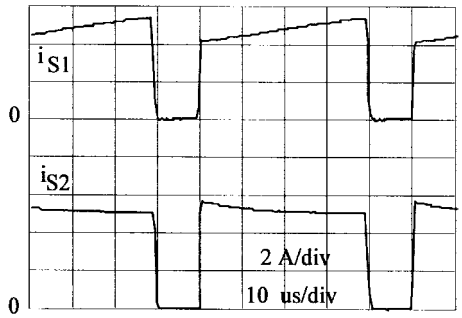

(b)

Fig. 12. Collector currents for nonsimultaneous gate pulses: (a) $L_1 = 0$ and (b) $L_1 = 14\,\mu$H.

On the other hand, the balance inductor resistance is a parameter that could interfere in the steady-state current equilibrium. This parasitic element depends on some inductor

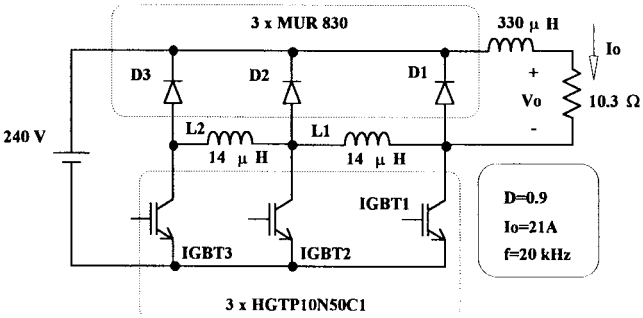

Fig. 13. 3I buck converter (experimental circuit).

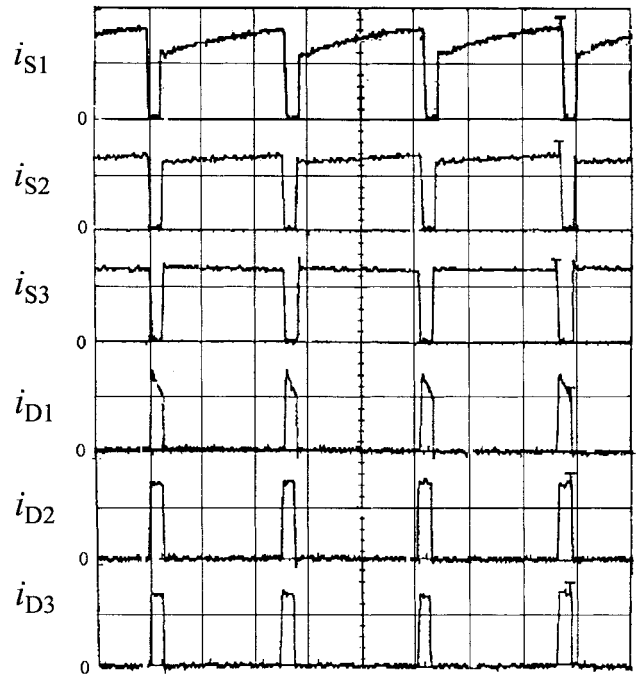

Fig. 14. Comparison among device currents (5 A/div, 20 μs/div).

design features, such as wiring material, number of turns and so one. If, for any reason, this parameter comes close to the semiconductor on-resistance, the designer could choose to provide a greater duty-cycle to devices that appear in series with the balance inductors (see Fig. 3). This stands for a more sophisticated procedure (and gate circuitry) and takes advantage of the two degrees of freedom of the new structure. It could also be used to solve a steady-state imbalance of currents caused by a variety of reasons (including those mentioned in the beginning of this paragraph). It is easy to conclude that this approach could not be used in the conventional parallel-connection technique. Taking the 2I converter as an example, S_2 duty-cycle (D_{S2}) should be:

$$D_{S2} = D_{S1}.\frac{2.R_o + r_L + r}{r + 2.R_o} \tag{12}$$

where r_L is the balance inductor resistance and R_o should correspond to the maximum load condition, where the current equilibrium is more important. Equation (12) has been derived by solving the circuit of Fig. 5 (using different duty-cycles for the active switches and including the balance inductor

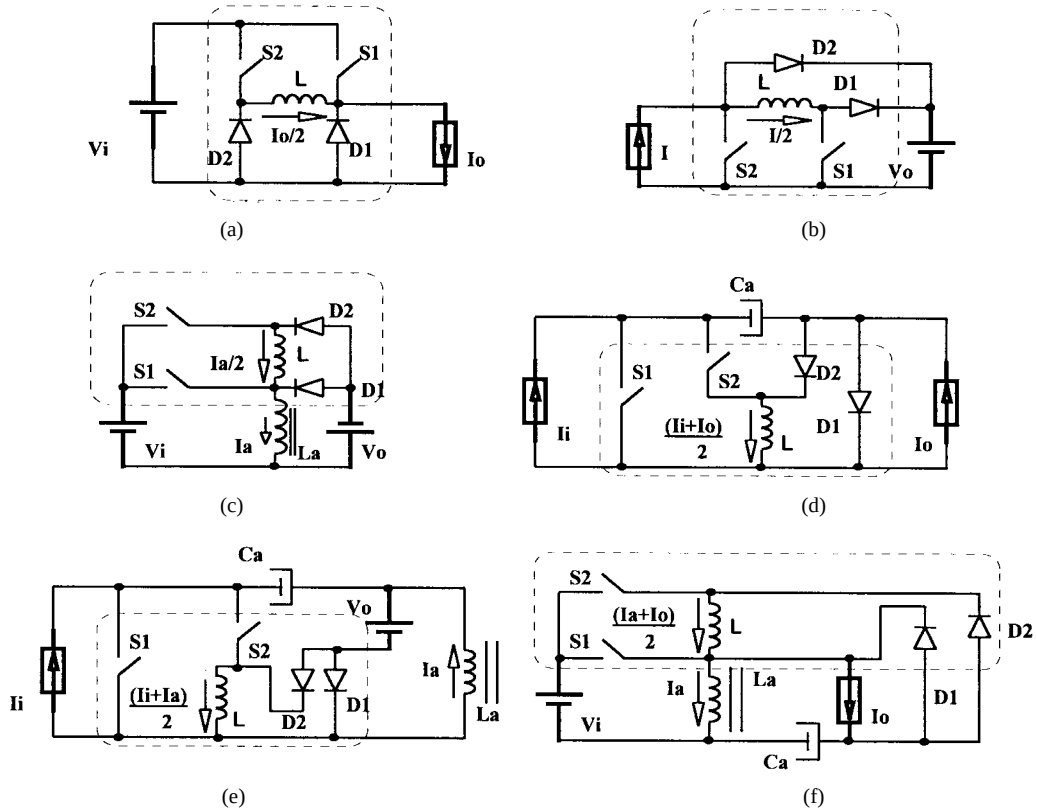

Fig. 15. The 2I dc–dc converters family: (a) buck, (b) boost, (c) buck-boost, (d) cuk, (e) sepic, and (f) zeta.

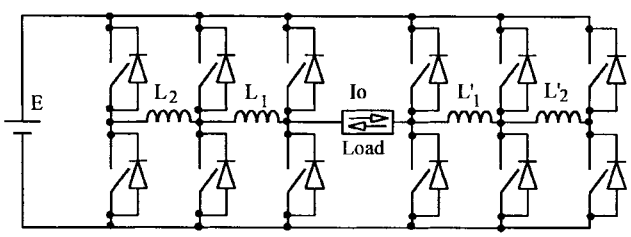

Fig. 16. Full-bridge 3I voltage source inverter.

resistance). A more detailed discussion about this subject can be found in [8], where the solution above is crucial.

Several medium-power experiments have been carried out in laboratory and no dynamic or steady-state problems have taken place. Fig. 13 shows the experimental circuit of a three-cell buck converter, which process 4.5 kW at a 20-kHz switching frequency and 90% of duty-cycle. Fig. 14 shows the current waveforms of each passive and active device of the structure, where it is possible to observe a good peak and steady-state distribution of currents. Of course, the ideal current sharing would occur at a 50% duty-cycle, in which all devices would process approximately the same average current. In spite of the absence of snubber circuits, negligible voltage and current spikes have been observed in this experiment [9].

VI. Applications

The generic cell of Fig. 1 can be adapted to any dc–dc converter as well as to inverters, as exemplified in Figs. 15 and 16.

TABLE I
Design Directives for the 2I DC–DC Converters

Converter Type	Maximum Applied Voltage, E	Shared Current
Buck	Input Voltage	Output Current
Boost	Output Voltge	Input Current
Buck-Boost	Input Voltage plus Output Voltage	Storage Inductor Current
Cuk	Storage Capacitor Voltage	Input Current + Output Current
Sepic	Output Voltage plus Storage Capacitor Voltage	Input Current + Storage Inductor Current
Zeta	Input Voltage plus Storage Capacitor Voltage	Output Current + Storage Inductor Currrent

The dc–dc converters of Fig. 14 are described by equation sets similar to those derived in Section III. In this figure, the input and output elements have been represented in a very simplified way in order to concentrate focus on the 2I commutation cell, which is enclosed by dashed lines in each converter of the figure. Design (11) can be also adapted to all dc–dc, 2I converters. To do so, Table I shows important information about parameter distinctiveness.

Considering the dc–ac VSI converters, another point must be mentioned. These converters differ from the dc–dc converters because, instead of having a dc current, they impose an alternating current to the load. As has been clear in theoretical

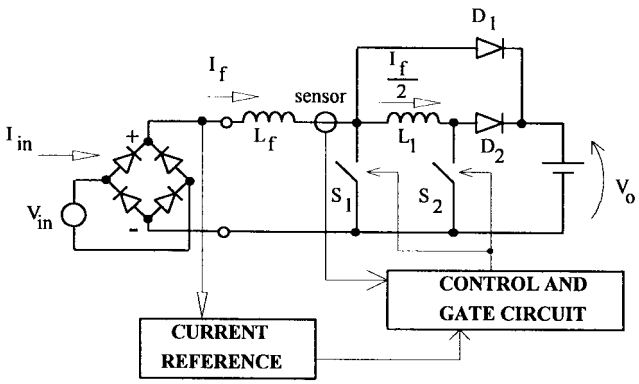

Fig. 17. A unity power factor rectifier based on a 2I boost converter.

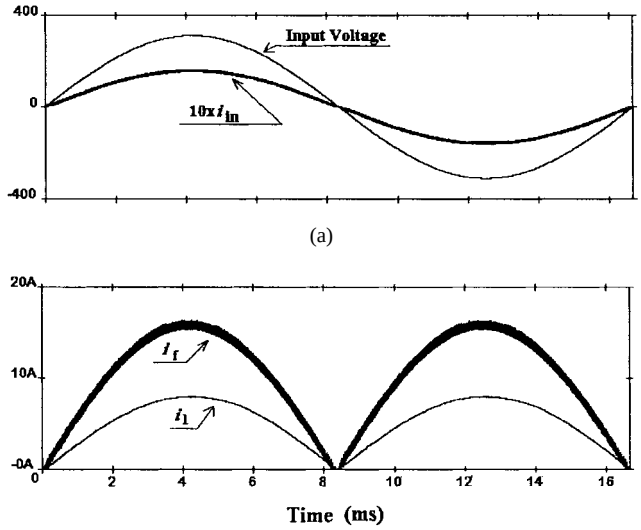

Fig. 18. Waveforms from computer simulation: (a) utility voltage and current and (b) boost and balance inductor currents.

analysis of Section III, balance inductor currents obey certain time constants. In order to have a fast response on the current sharing process, one need to choose inductor time constants (the relationship between their inductances and parasitic resistances) much smaller than the output current period time. On the other hand, fast time constants (or smaller inductances) may allow greater current spikes due to the switching nonideal operation. In other words, there is a compromise between proper current damping and maximum output frequency for VSI converters.

The new structure can also be applied to rectifiers with unity power factor based on a two-cell boost converter, as shown in Fig. 17. This application has the purpose of distributing the total processed power between two smaller commutation cells [10]. Doing so one can expect a reliable converter with an improved performance. Moreover, it is also possible to reduce the losses caused by current sensing simply moving the sensor to the balance inductor branch. Figs. 18 and 19 show the waveforms obtained from computer simulation, from which one can see a good current distribution between semiconductor elements.

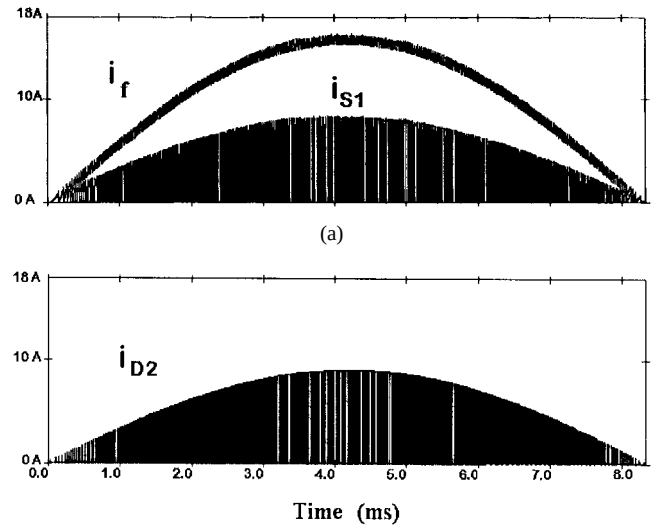

Fig. 19. Waveforms from computer simulation: (a) input inductor and S_1 currents and (b) D_2 current.

VII. Conclusion

This paper has presented a new paralleling technique that can be applied to any kind of power electronics converter. Simplified analysis and modeling have been introduced. The new technique appears to have better characteristics as compared to the conventional ones since it is simple and cheap, has no need of controlling strategy, and is more independent of device switching times, by damping device current spikes (even in the presence of wiring unbalance).

The new technique presented here can be applied to several technologies of semiconductor devices and can be extended to a great number of paralleled elements. However, the selected devices must have similar conduction (on-state) behavior, while looser specifications can be tolerated concerning the switching parameters of devices, gate drive, and circuit layout.

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