Zero-Voltage Switching for Three-Level Capacitor Clamping Inverter

Xiaoming Yuan, *Member, IEEE,* and Ivo Barbi, *Senior Member, IEEE*

***Abstract*—A zero-voltage switching (ZVS) scheme for a three-level capacitor clamping inverter based on the true pulsewidth modulation (PWM) pole is proposed in this paper. With this scheme, the main switches work with ZVS through the assistance of a small rating zero-current switching (ZCS) lossless auxiliary circuitry without imposing any voltage/current spikes on the main devices or any extra control complexities. Consequently, a three-level capacitor clamping inverter system can operate at a promoted switching frequency and becomes more eligible to be considered for high-power advanced applications, for example, in high-speed drives or power active filter areas. In this paper, the main circuit operation issues as regards the clamping voltage stability, clamping capacitor stress, and output voltage spectrum are shortly reviewed first, after which the commutation principle, auxiliary circuitry stress analysis, and auxiliary circuitry designing methodology are presented in details. Experimental results from a 700-V supply 3-kW half-bridge three-level capacitor clamping inverter are demonstrated which conform well to the proposal.**

***Index Terms*—Soft-switching, three-level inverter.**

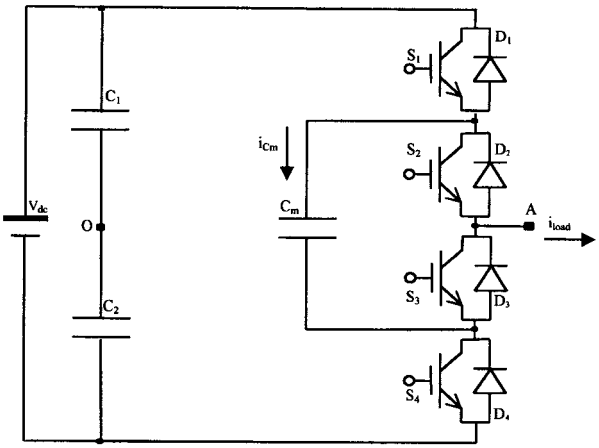

Fig. 1. Configuration of a half-bridge three-level capacitor clamping inverter. S_2 and S_3 form the first switching cell whereas S_1 and S_4 form the second switching cell.

I. Introduction

THE neutral-point-clamped (NPC) inverter has in recent years been receiving growing attention from industry for drive or utility applications due to the extended capacity with existing devices without the problematic series association [1]–[3]. Such problems, however, are outstanding with this topology [4], [5]:

- extra two clamping diodes per leg with the same requirements as the main freewheeling diodes;
- extra regulation loop for stabilization of the neutral potential;
- indirect clamping of the inner devices and the resultant overblocking voltage.

An alternative topology capable of three-level inversion is the capacitor clamping inverter [6], [7]. Instead of the two extra diodes, a flying storage capacitor is used in each leg across the inner two devices, one leg of which is shown in Fig. 1. The clamping voltage can be established and stabilized through a inherent feedback mechanism without any further active regulation [8], which enables direct clamping and thus tight control of all the four devices in the leg. These features render the capacitor clamping inverter a potential match of the NPC inverter in future drive or power system applications where high-voltage high-power installation (>1 MVA) is demanded.

On the other hand, hard-switching frequency of the present high-power IGBT components is severely limited to a few kilohertz or even less [9], [10] due to the enormous switching loss. Besides the voltage/current spikes resulting from turn-on/turn-off snubber interactions, a dissipative snubber is particularly limited by its significant snubber loss, which is proportional to the switching frequency and more than proportional to the installation power. The optimized regenerative snubber [11], [12] seems to solve the problems, but also leads to a substantial increase of components. The series reactor in the main current path as well as the polarizing diode in the turn-off snubbing path cause extra problems.

In the meanwhile, several zero-voltage switching (ZVS) high-power two-level inverter topologies have been explored in the past replacing the conventional snubber and improving the performance, among which the auxiliary resonant commutated pole inverter (ARCP) [13], [14] has been mostly applauded in the literature for its small power auxiliary circuitry, full pulsewidth modulation (PWM), and good device utilization. However, transducers for load current and resonant inductor current monitoring must be installed so that the "boost" stage is controlled [14], [15] to ensure true ZVS. The transducers and the associated control complexity give rise to cost and reliability problems [16]. A simplified control scheme intending to eliminate the transducers and the "boost" stage [17] results in considerable loss, and ZVS is lost.

Such simplification, however, is obtainable with the scheme of a true PWM pole [18], [19], as shown in Fig. 2. Unlike the

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X. Yuan is with the Power Electronics and Electrometrology Laboratory, Swiss Federal Institute of Technology, Zurich, Switzerland.

I. Barbi is with the Power Electronics Institute, Federal University of Santa Catarina, 88040-970 Florianópolis (SC), Brazil (e-mail: ivo@inep.ufsc.br).

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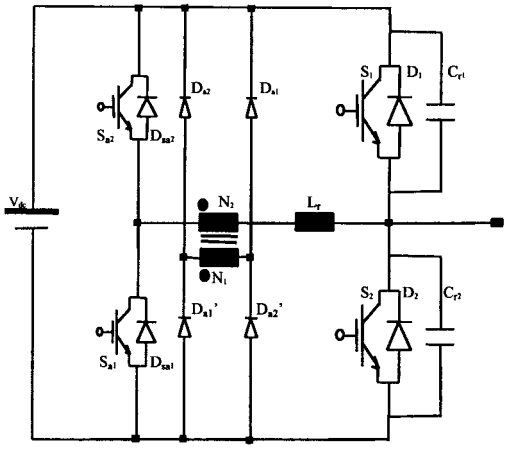


Fig. 2. The true PWM pole soft-switching scheme, consisting of a main switching cell (S_1, S_2) and an auxiliary branch (S_{a1}, S_{a2}).

ARCP, the auxiliary voltage source in the true PWM pole for the resonance is acquired with the help of a transformer. When the transformer ratio is set at a value less than 1/2 depending on the resonance loop losses, an auxiliary voltage source higher than half the dc rail voltage is obtained. The extra energy compensates the commutation losses and enables the pole voltage swinging to the rail level during the resonance. ZVS is therefore guaranteed.

This paper proposes a true PWM pole three-level capacitor clamping inverter which can be used to advantage in high-power advanced applications. With the assistance of a small rating lossless auxiliary circuitry, ZVS is achieved for the main devices with easy control and without provoking any switching spikes on the main devices.

II. Main Circuit Modulation Strategy and the Proposed ZVS Topology

The half-bridge three-level capacitor clamping inverter main circuit shown in Fig. 1 can be decomposed into two two-level switching cells. S_2 and S_3 work alternatively and form the first switching cell, whereas S_1 and S_4 work alternatively and form the second switching cell. Modulation of the main circuit will have major effects on the following aspects of circuit performance:

- steady-state stability of the clamping capacitor voltage V_{C_m};
- rms current through and ripple voltage across the clamping capacitor;
- output voltage V_{AO} spectrum;
- dynamic state stability of the clamping capacitor voltage.

The details of these effects under the half-bridge circumstance have been well explored [8]. Main circuit modulation scheme employed in this paper is shown in Fig. 3, where two triangular carriers (carriers 1 and 2) for the two switching cells are π phase shifted, intersecting with a sinusoidal modulating signal mod(t). Under this modulation pattern, the following results are obtained, which hold also for the three-phase case.

- Steady-state stability of the clamping voltage is ensured.
- RMS current through and ripple voltage across the clamping capacitor are dependent on the load power factor and will reach the maximum when $\cos\theta = 0$. Here, θ is the load impedance angle.
- Output voltage sees an optimal spectrum. The triangle carrier frequency components together with its cross-modulation harmonics are canceled.
- Clamping voltage dynamics exhibits typical one-order system characteristics. Load property, modulation index, and clamping capacitance decide the time constant. Dynamic stability is ensured so long as the load impedance angle meets $\cos\theta \neq 0$.

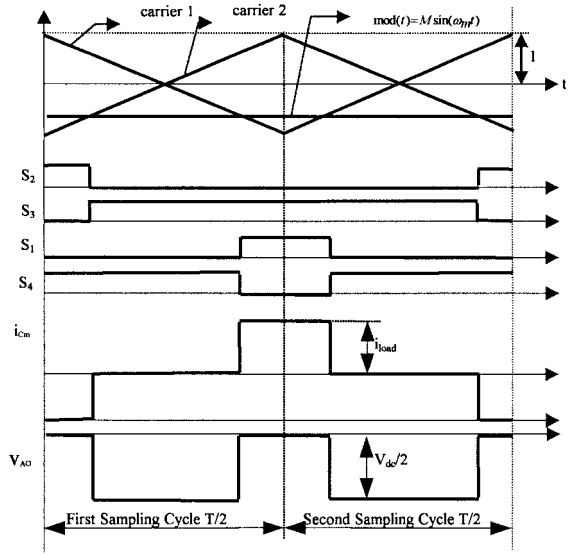


Fig. 3. Main circuit modulation strategy for the half-bridge three-level capacitor clamping inverter and the associated clamping capacitor current and output voltage waveforms (neglecting the commutation processes).

The proposed ZVS three-level capacitor clamping inverter (half bridge) is shown in Fig. 4. It consists of a main capacitor clamping half-bridge circuit and two auxiliary branches. The first auxiliary branch (S_{a2}, S_{a3}) assists the commutation of the first switching cell (S_2, S_3) and forms the first pole, whereas the second auxiliary branch (S_{a1}, S_{a4}) assists the commutation of the second switching cell (S_1, S_4) and forms the second pole. The two poles can be regarded independent from each other so far as the clamping capacitor voltage is maintained at $V_{\rm dc}/2$.

III. Commutation Principle of the True PWM Pole Three-Level Capacitor Clamping Inverter

Prior to discussion of the commutation process, the following conditions are assumed.

- Positive load current $i_{\rm load}$ is flowing and remains constant during the commutation.
- Capacitors C_1 and C_2 are treated as voltage sources during the commutation. Clamping capacitor voltage is stabilized at $V_{\rm dc}/2$.
- Transformer ratios are set to ensure sufficient energy for the pole voltage swinging to the rail level in the presence of commutation losses.
- Construction parasitics, device switching transience, and transformer imperfections are neglected.

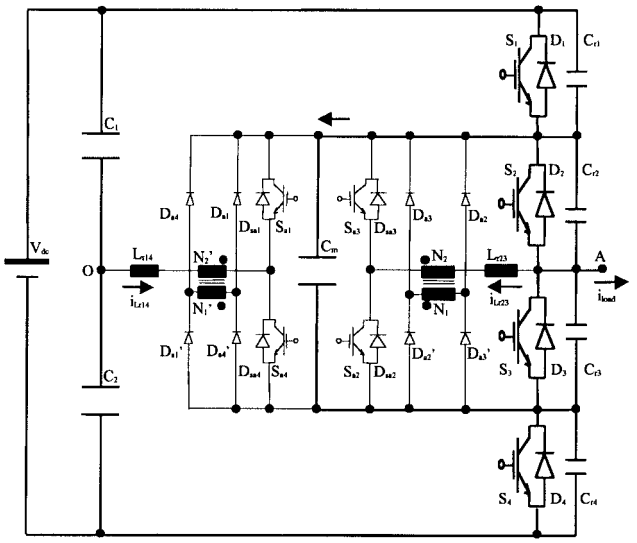


Fig. 4. The proposed half-bridge true PWM pole three-level capacitor clamping inverter. The two auxiliary branches assist the commutation of the two main switching cells, making up two true PWM poles.

- Main switch turn off and auxiliary switch turn on happen at the same instant decided from the modulation scheme shown in Fig. 3, while the main switch turn on happens until the detected voltage across the switch declining to zero. The conduction interval of the auxiliary switch is universally constant covering the maximum commutation duration as discussed later in Section IV.

Referring to the theoretical waveforms for the entire switching cycle shown in Fig. 5 and the commutation step diagrams for the first sampling cycle shown in Fig. 6, the commutation of the half-bridge inverter during the first sampling cycle consists of the next steps.

Step 1 ($t_o - t_1$): Circuit steady state. D_4 and S_2 carry load current discharging the clamping capacitor C_m. Output voltage $V_{AO} = 0$.

Step 2 ($t_1 - t_2$): S_2 turned off and S_{a2} turned on at t_1, which starts a resonance between L_{r23} and C_{r2}, C_{r3}. N_2 sees a voltage of $kV_{\rm dc}/2$ after turn on of S_{a2} and conduction of D_{a2} and D'_{a2}. C_{r2} is charged and C_{r3} is discharged.

Step 3 ($t_2 - t_3$): V_{Cr2} rises to $V_{\rm dc}/2$ at t_2 leading to conduction of D_3. Then S_3 is turned on at zero voltage. Snap on of D_3 may cause oscillation due to stray/internal inductances of the paths.

Step 4 ($t_3 - t_5$): i_{Lr23} falls to zero at t_3 allowing for turn off of S_{a2} at t_4. The circuit reaches another steady state. D_4 and D_3 carry load current. Clamping capacitor C_m is floating. Output voltage $V_{AO} = -V_{\rm dc}/2$.

Step 5 ($t_5 - t_6$): S_4 is turned off and S_{a4} is turned on at t_5, leading to conduction of D_{a4} and D'_{a4}. N'_2 sees a voltage of $kV_{\rm dc}/2$ which joins $V_{\rm dc}/2$ enforcing current decreasing in D_4.

Step 6 ($t_6 - t_7$): i_{Lr14} rises to the load current level at t_6 leading to blocking of D_4. Resonance among L_{r14}, C_{r4}, and C_{r1} is initiated. C_{r4} is charged while C_{r1} discharged. Recovery current of D_4 enhances the charging current and therefore facilitates the commutation process.

Step 7 ($t_7 - t_8$): V_{Cr4} rises to $V_{\rm dc}/2$ at t_7 leading to conduction of D_1. Then S_1 is turned on at zero voltage. Rapid current transfer from C_{r4} and C_{r1} to D_1 may cause oscillation.

Step 8 ($t_8 - t_9$): i_{Lr14} falls to load current at t_8. D_1 stops conduction and S_1 starts carrying current.

Step 9 ($t_9 - t_{11}$): i_{Lr14} extinguishes at t_9 allowing for turn off of S_{a4} at t_{10}. Circuit reaches another steady state. S_1 and D_3 carry load current charging the clamping capacitor C_m. Output voltage $V_{AO} = 0$.

The remaining two commutations in the second sampling cycle (D_3 to S_2 and S_1 to D_4) can be analogously inferred.

To summarize, for the proposed circuit, the main switch works with soft turn on and snubbed turn off, whereas the main freewheeling diode works with hard turn on and soft turn off. Superior to the conventional snubber, the snubbed turn-off loss of the main switch here can be minimized by optimizing the resonant capacitor to this end. Meanwhile, depending on its forward recovery property, the hard turn on of the main freewheeling diode does not introduce any considerable loss.

Moreover, all the auxiliary devices work with soft turn off. Yet voltage is only reapplied after turn on of the opposite auxiliary switch. Besides, despite the bridge configuration, the turn on of the auxiliary switch is actually snubbed by the resonant inductor since the opposite freewheeling diode carries no current beforehand and thus its reverse recovery is negligible. Transformer excitation is reset to zero after each commutation and no magnetic accumulation can happen.

In particular, by designing a transformer ratio less than 1/2, an auxiliary voltage of $(1-k)V_{\rm dc}/2$ higher than $V_{\rm dc}/4$ becomes available which delivers sufficient energy for the resonant pole to swing to the rail voltage. Thus, the "boost" stage and the associated control complexity are no longer necessary. Losses incurred from the extra turn-on/turn-off actions of the switch are further avoided.

IV. Theoretical Analysis of the Commutation Process

Analysis in this section takes the second pole (S_1 and S_4) as an example. The results remain valid for the first pole (S_2 and S_3). The following assumptions are made for the analysis.

- $L_{r14} = L_{r23} = L_r$, $C_{r1} = C_{r2} = C_{r3} = C_{r4} = C_r$, and $N'_2/N'_1 = N_2/N_1 = k < 1/2$.
- Resonance angle frequency $\omega_0 = 1/\sqrt{2C_rL_r}$, resonance impedance $Z_o = \sqrt{L_r/2C_r}$, and switching period T.
- Unit current $\overline{i} = iZ_o/(V_{\rm dc}/2)$, unit voltage $\overline{v} = v/(V_{\rm dc}/2)$, and unit time $\overline{t} = t\omega_0$.

Then the commutation process can be represented by a phase plane diagram as shown in Fig. 7. In correspondence with

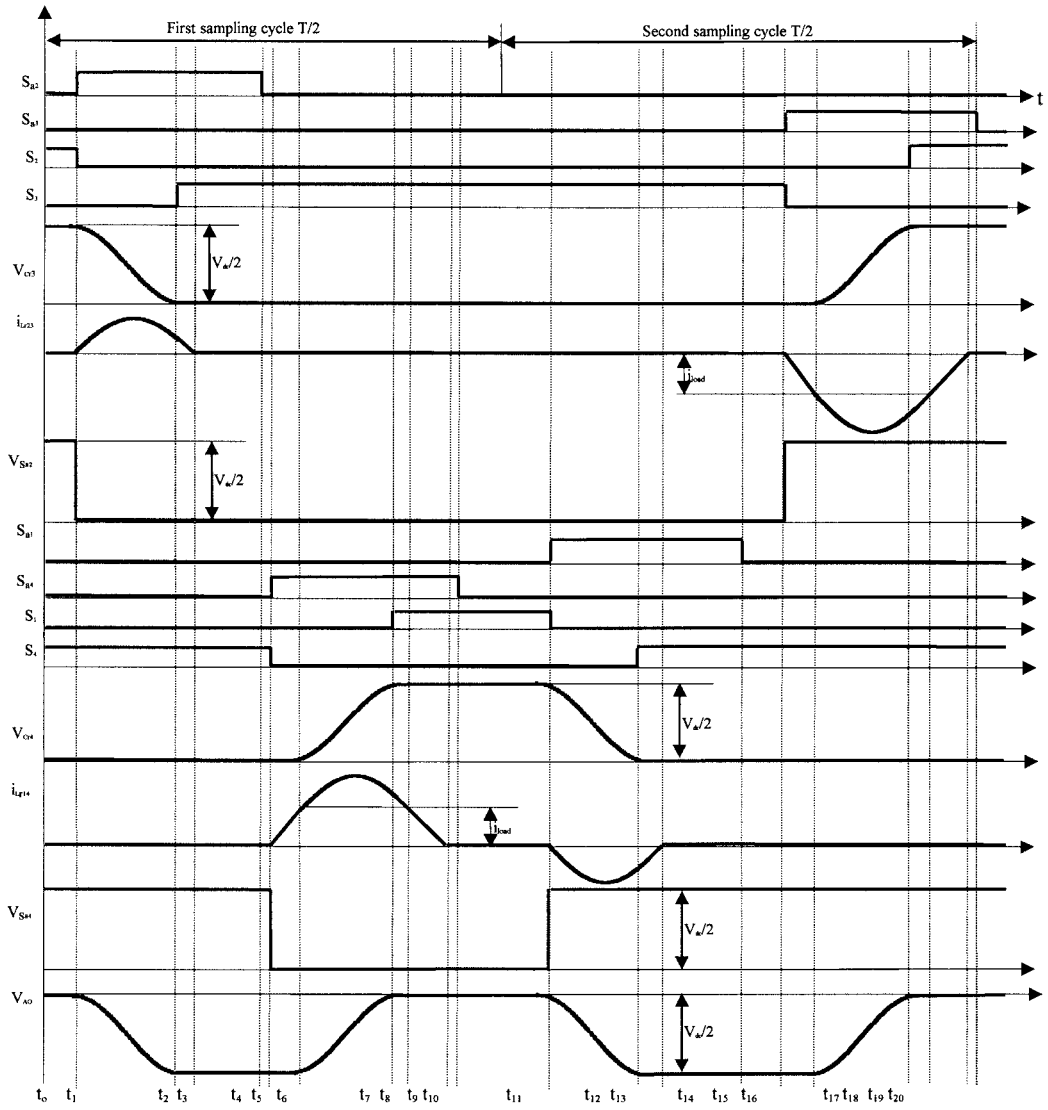


Fig. 5. Theoretical commutation waveforms for the proposed true PWM pole three-level capacitor clamping inverter in an entire switching cycle.

Fig. 5, diode-to-switch commutation ($D_4 - S_1$) and switch-to-diode commutation ($S_1 - D_4$) are depicted by $t_5 - t_9$ and $t_{11} - t_{13}$ in Fig. 7, respectively. The two arrows stand for the radiuses of the two resonances in the commutation process.

A. Total Commutation Duration

For diode-to-switch (D_4 to S_1) commutation, the unit value of the total commutation duration $t_{95} = t_9 - t_5$ is given by

$$\omega_o t_{95} = \frac{\overline{i_{\text{load}}}}{(1-k)} + \left(\pi - a\cos\frac{k}{1-k}\right) + \frac{\sqrt{1-2k}}{k} + \frac{\overline{i_{\text{load}}}}{k}. \tag{1}$$

For switch-to-diode (S_1 to D_4) commutation, the unit value of the total duration $t_{1311} = t_{13} - t_{11}$ is given by

$$\omega_o t_{1311} = \pi - a\cos\frac{k}{\sqrt{(1-k)^2 + \overline{i_{\text{load}}}^2}} - a\cos\frac{(1-k)}{\sqrt{(1-k)^2 + \overline{i_{\text{load}}}^2}} + \sqrt{1-2k+\overline{i_{\text{load}}}^2} - \overline{i_{\text{load}}}. \tag{2}$$

Equations (1) and (2) are graphically shown in Fig. 8(a) and (b).

B. Auxiliary Device Peak Current Stress

For diode-to-switch (D_4 to S_1) commutation, the unit value of the auxiliary switch (S_{a4}) peak current i_{sap1} can be represented by

$$\overline{i_{sap_1}} = \left(\overline{i_{\text{load}}} + 1 - k\right). \tag{3}$$

For switch-to-diode (S_1 to D_4) commutation, the unit value of the auxiliary switch (S_{a1}) peak current i_{sap2} can be represented by

$$\overline{i_{sap_2}} = \left(\sqrt{(1-k)^2 + \overline{i_{\text{load}}}^2} - \overline{i_{\text{load}}}\right). \tag{4}$$

As shown in Fig. 9(a) and (b), for diode-to-switch (D_4 to S_1) commutation, the peak current of the corresponding

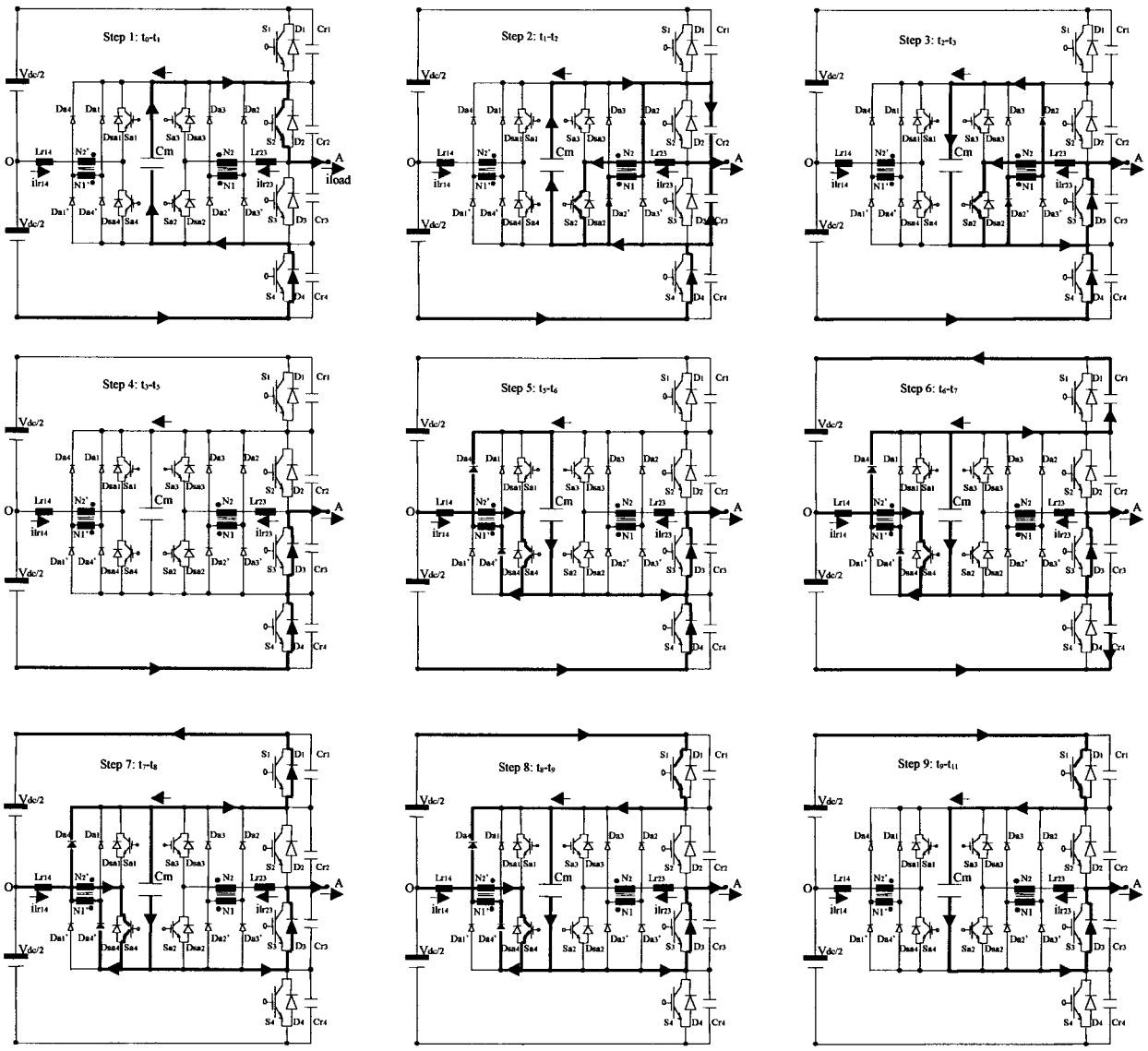


Fig. 6. Operation step diagrams for the first sampling cycle.

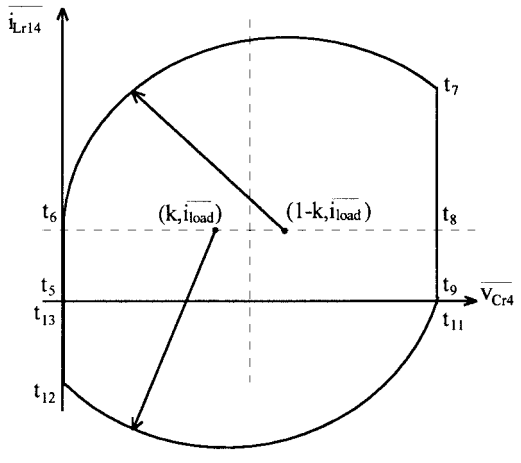


Fig. 7. Phase plane of the resonance between L_{r14} and C_{r4} during the whole commutation process of the second pole.

auxiliary switch increases with the load current. For switch-to-diode commutation (S_1 to D_4), however, it decreases with the load current.

C. Auxiliary Device RMS Current Stress

The resonant inductor rms current stress over switching period resulting from diode-to-switch commutation $\overline{i_{Lrprms}}$ can be expressed by

$$\left(\overline{i_{Lrprms}}\right)^2 = \frac{1}{\overline{T}}\int_0^{L_1}\left[(1-k)\bar{t}\right]^2 d\bar{t} + \frac{1}{\overline{T}}\int_0^{L_2}\left[\overline{i_{\text{load}}} + (1-k)\sin(\bar{t})\right]^2 d\bar{t} + \frac{1}{\overline{T}}\int_0^{L_3}\left[\sqrt{1-2k} - k\bar{t}\right]^2 d\bar{t} \quad (5)$$

where

$$L_1 = \overline{i_{\text{load}}}/(1-k)$$
$$L_2 = \pi - a\cos\left(\frac{k}{1-k}\right)$$
$$L_3 = \left(\overline{i_{\text{load}}} + \sqrt{1-2k}\right)\Big/k.$$

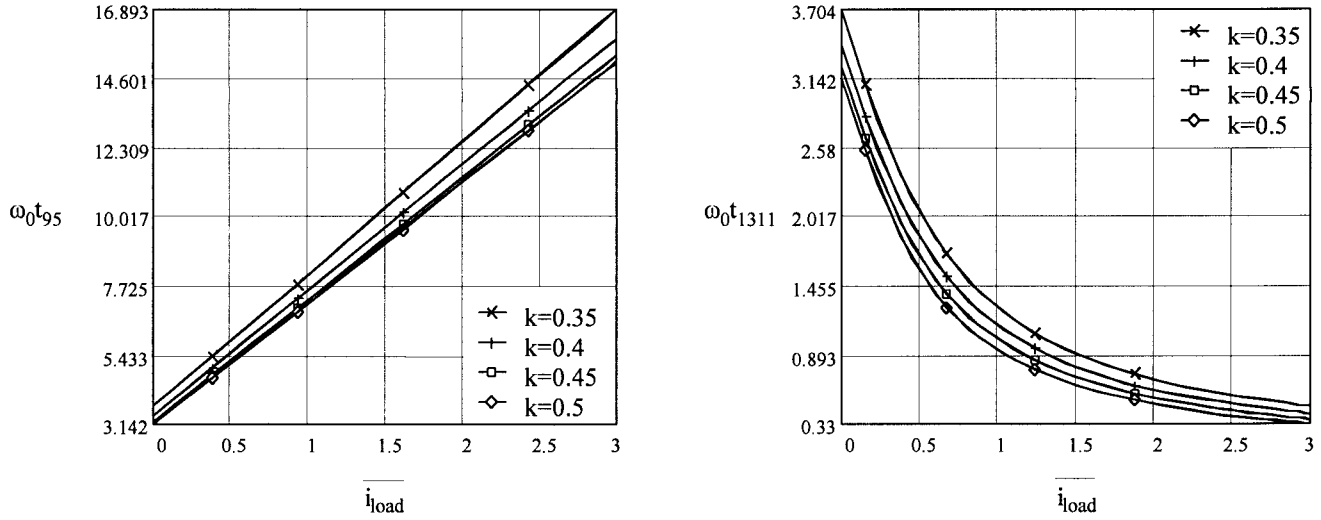


Fig. 8. Variations of commutation durations t_{95} and t_{1311} with load current and transformer ratio: (a) diode-to-switch commutation and (b) switch-to-diode commutation.

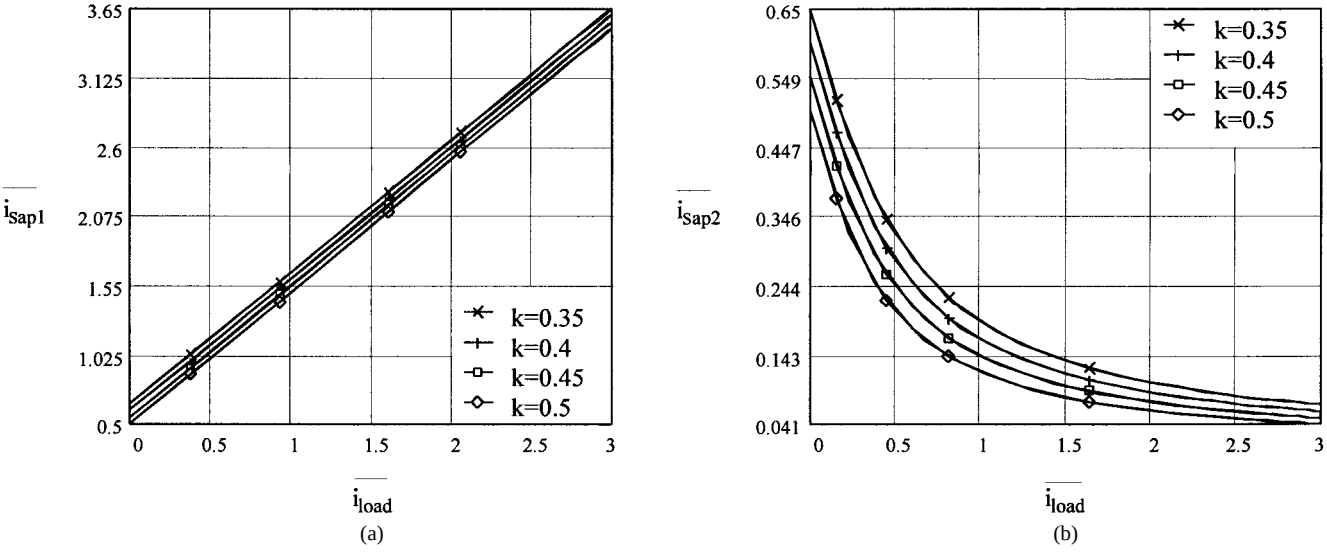


Fig. 9. Variations of the auxiliary switch peak currents with load current and transformer ratio: (a) diode-to-switch commutation and (b) switch-to-diode commutation.

Similarly, the resonant inductor rms current resulting from switch-to-diode commutation $\overline{i_{Lrn\mathrm{rms}}}$ is expressed by

$$\begin{aligned}\left(\overline{i_{Lrn\mathrm{rms}}}\right)^2 &= \frac{1}{\overline{T}}\int_0^{J_1}\left[\overline{i_{\mathrm{load}}}+(k-1)\sin(\bar{t})-\overline{i_{\mathrm{load}}}\cos(\bar{t})\right]^2 d\bar{t} \\ &\quad + \frac{1}{\overline{T}}\int_0^{J_2}\left[-\sqrt{1-2k+\left(\overline{i_{\mathrm{load}}}\right)^2}+\overline{i_{\mathrm{load}}}+k\bar{t}\right]^2 d\bar{t}\end{aligned} \tag{6}$$

where

$$J_1 = \pi - a\cos\frac{k}{\sqrt{(1-k)^2+\left(\overline{i_{\mathrm{load}}}\right)^2}} - a\cos\frac{1-k}{\sqrt{(1-k)^2+\left(\overline{i_{\mathrm{load}}}\right)^2}}$$

$$J_2 = \left(\sqrt{(1-k)^2+\left(\overline{i_{\mathrm{load}}}\right)^2}-\overline{i_{\mathrm{load}}}\right)\Big/k.$$

The auxiliary switch rms current during diode-to-switch commutation $\overline{i_{Sap\mathrm{rms}}}$ and switch-to-diode commutation $\overline{i_{San\mathrm{rms}}}$ are equal to $\overline{i_{Lrp\mathrm{rms}}}$ and $\overline{i_{Lrn\mathrm{rms}}}$, respectively, and the relationships are shown in Fig. 10(a) and (b). The resonant inductor rms current can then be described by

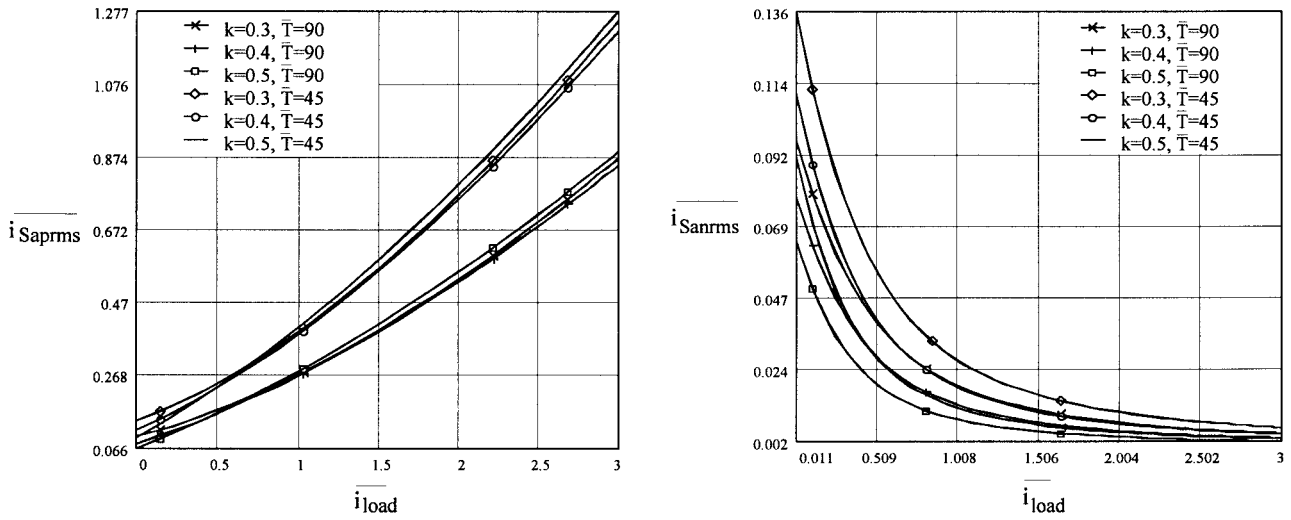
$$\overline{i_{Lr\mathrm{rms}}} = \sqrt{\overline{i_{Lrp\mathrm{rms}}}^2+\overline{i_{Lrn\mathrm{rms}}}^2}. \tag{7}$$

V. Design Methodology of the Auxiliary Circuitry

A. Autotransformer Ratio k

To ensure ZVS in the presence of losses (device conduction loss, resonant inductor loss, resonant capacitor loss, etc.), autotransformer ratio k should meet

$$(1-k)-\frac{1}{2}\geq\frac{1}{2}\frac{\pi}{4Q} \tag{8}$$



(a) (b)

Fig. 10. Variations of the auxiliary switch rms currents with load current, transformer ratio, and switching period: (a) diode-to-switch commutation and (b) switch-to-diode commutation.

where $Q = \omega_o L_r / R$ and R represents the equivalent resistance in the resonance loop. Equation (8) can be simplified to

$$k \leq \frac{1}{2} - \frac{\pi}{8Q}. \tag{9}$$

B. Resonant Frequency ω_o

The resonant frequency can be set by optimizing the rms stress of the auxiliary switch according to Fig. 10(a) based on the switching frequency of the system.

C. Resonant Capacitor C_r and Resonant Inductor L_r

The resonant capacitance should be optimized for the main switch turn-off loss [20]. Based on the resonant frequency and the resonant capacitance, the resonant inductance is decided.

D. Auxiliary Switch Gating Signal Width and Minimum PWM ON/OFF Time

The minimum width of the auxiliary switch gating signal must be set above the maximum value of the commutation duration, as demonstrated in Fig. 8(a). In the same sense, the minimum PWM ON/OFF time ($t_{11} - t_5$ and $t_{15} - t_1$ as shown in Fig. 5) should also be set above this value.

E. Rating of the Auxiliary Switch

Due to the zero-current switching (ZCS) in the auxiliary circuitry and due also to the high-switching frequency with respect to the thermal inertia of the device, the rating of the auxiliary switch should be chosen according to its rms stress as illustrated in Fig. 10(a). However, auxiliary switch peak current illustrated in Fig. 9(a) should not exceed the device peak output current rating.

VI. Experimentation

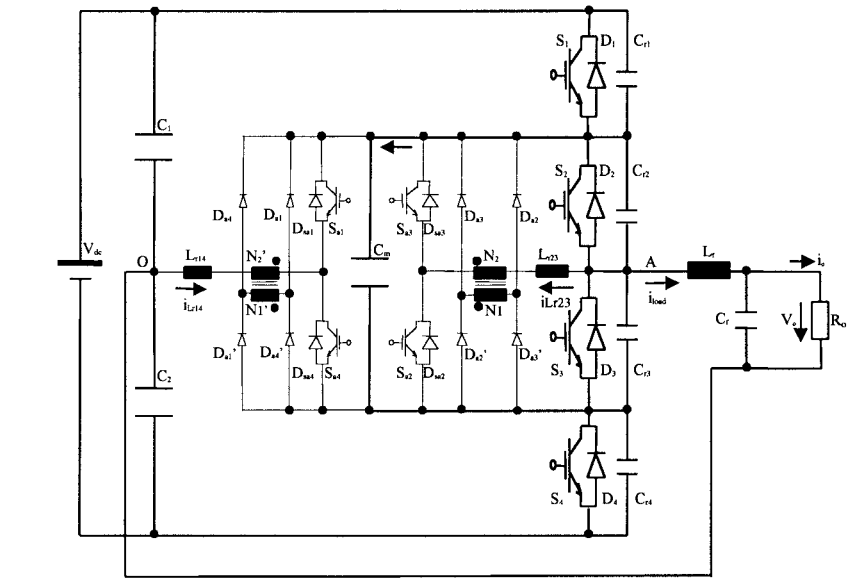
A proof-of-concept IGBT half-bridge inverter, as shown in Fig. 11(a), has been built with the specifications shown in Table I. Designing results of the resonant and transformer parameters according to Section V are shown in Table II.

As a result of the above designing, the resultant maximum commutation duration is 11.3 μs. The maximum peak and rms currents of the auxiliary switch are 54.2 and 8.4 A, respectively. Thus, the auxiliary switch gating signal width is set at 15 μs and the minimum PWM ON/OFF time is set at 25 μs. Four SEMIKRON IGBT modules (SKM50GB123D, 1200 V/50 A) are employed as the main and auxiliary switches, and eight ultrafast international rectifier diodes (HFA30TA60C, 630 V/30 A) work as the auxiliary diodes. Two storage capacitors C_1 and C_2 each rated at 360 V/3300 μF form the center tap. A low-pass filter ($L_f = 1.45$ mH, $C_f = 12$ μF) is installed at the output. Besides, a voltage monitoring circuit as shown in Fig. 11(b) is installed across each main device to release the turn-on gating signal when the detected voltage is zero. Such monitoring is essential for ensuring ZVS because of the load current dependant fraction in the pole dead time taken for the conducting diode to block which makes constant dead time setting not possible.

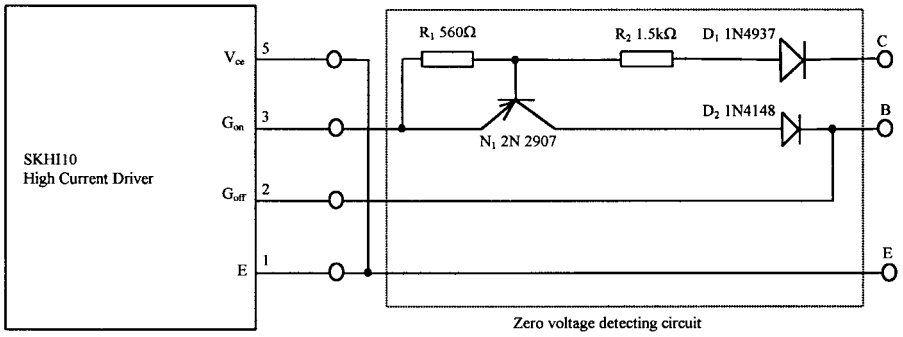
Fig. 12 shows the output load side voltage and filter inductor current waveforms. Fig. 13 shows the three-level output voltage V_{AO}.

Fig. 14 shows the ZVS commutation process of the main switch S_3 during switching cycle. Furthermore, in Fig. 15, the details of turning on at $i_{\text{load}} = 21$ A are shown. For a predicted dv/dt of 90 V/μs (averaged over $t_{12} - t_{11}$) and di/dt of 14 A/μs, the experimental values are about 90 V/μs and 13 A/μs, respectively. In Fig. 16, the details of turning-off at $i_{\text{load}} = 24$ A are shown. For a predicted dv/dt of 152 V/μs (averaged over $t_7 - t_6$), the experimental value is about 146 V/μs.

Fig. 17 shows the ZCS commutation process of the auxiliary switch (S_{a3}/D_{sa3}) at $i_{\text{load}} = 22$ A. For the predicated commutation duration of 9.8 μs according to Fig. 8(a) and the predicated peak current of 46.3 A according to Fig. 9(a), the experimental values are 9.5 μs and 46.5 A, respectively.



(a)



(b)

Fig. 11. (a) Prototype configuration of the half-bridge modified true PWM pole capacitor clamping inverter and (b) voltage monitoring circuit interfacing the SEMIKRON SKHI10 driver with the main IGBT device.

TABLE I
PROTOTYPE SPECIFICATIONS

DC input voltage	V_{dc}=700V	Output voltage (RMS)	V_o=140V	Modulation index	M=0.62
Output power	P_o=3kW	Load current (RMS)	I_o=21.5A	Switching frequency	f_c=6.5kHz

TABLE II
RESONANT AND TRANSFORMER DESIGNING RESULTS

Resonant capacitor	*1*. Capacitance: C_r=0.1uF, *2*. Type: low-loss polypropylene, *3*. Maximum turn-off loss 0.1W.
Resonant inductor	*1*. Inductance: L_r=15uH, *2*. Structure: 36 turns 15AWG copper wire wound on air core bobbin, *3*. Current rate of changing 14A/uS.
Transformer	*1*. Transformer ratio: k =0.4, *2*. Structure: 60 turns Litz wire (7 strands 24AWG) in the primary and 24 turns Litz wire (15 strands 24AWG) in the secondary wound on E65/29 ferrite core, *3*. allowed equivalent loop resistance around 2.2Ω.

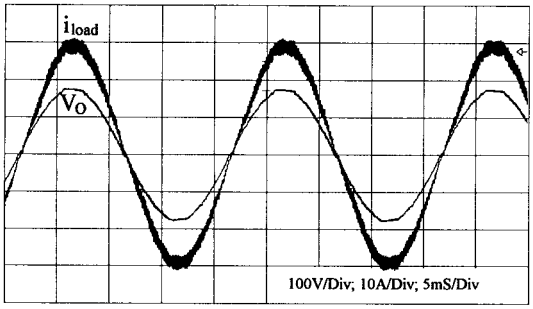


Fig. 12. Experimental output voltage and filter inductor current (V_O and $i_{\rm load}$).

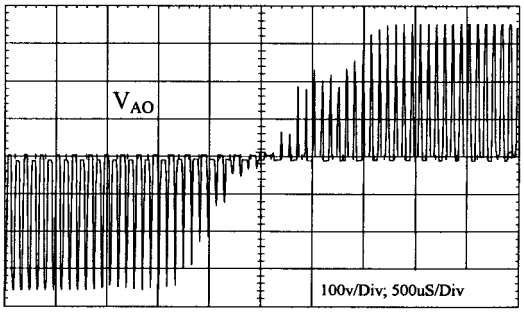


Fig. 13. Experimental inverter output voltage V_{AO}.

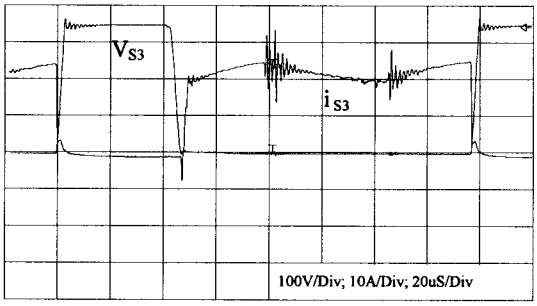


Fig. 14. ZVS commutation of the main switch (S_3).

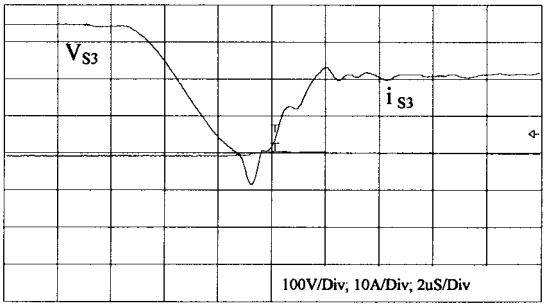


Fig. 15. Extended turn-on process of S_3.

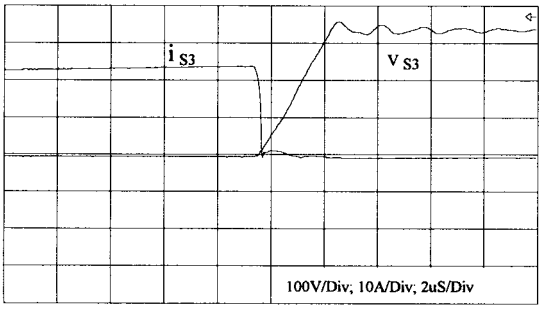


Fig. 16. Extended turn-off process of S_3.

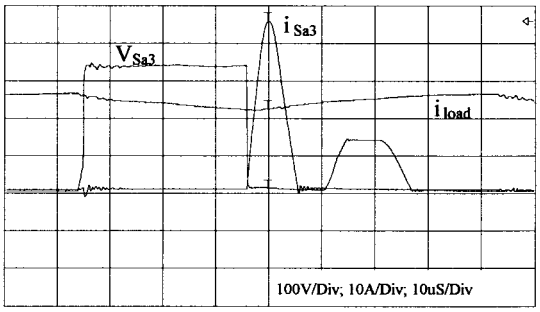


Fig. 17. ZCS commutation of the auxiliary switch (S_{a3}).

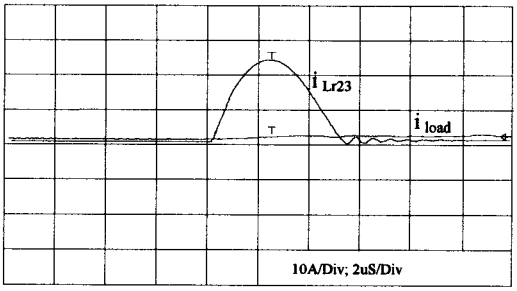


Fig. 18. Resonant inductor current waveform at $i_{\rm load} = 0$ A.

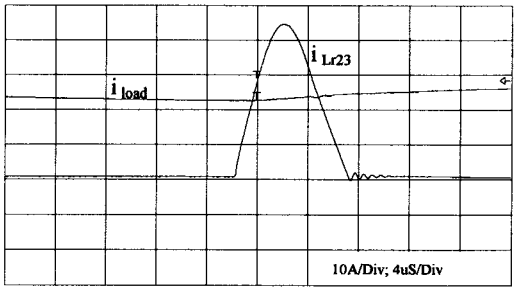


Fig. 19. Resonant inductor current waveform at $i_{\rm load} = 22$ A.

Fig. 18 shows the resonant inductor current waveform when $i_{\rm load} = 0$ A. For the predicated commutation duration of 5.9 μs and the predicated peak current of 24.1 A, the experimental values are about 5.5 μs and 23.5 A, respectively. In the meantime, Fig. 19 shows the resonant inductor current waveform when $i_{\rm load} = 22$ A. The experimental commutation duration and peak current are about 9.5 μs and 46.5 A, which are in accordance with the predicated values of 9.8 μs and 46.3 A according to Figs. 8(a) and 9(a), respectively.

Measured efficiency of the prototype reaches 95% at full load.

VII. Conclusion

From the theoretical and experimental studies reported above, the following conclusions can be drawn.

- The proposed technique achieves zero-voltage commutation of the main devices in the three-level capacitor clamping inverter with the help of a small rating zero current commutation auxiliary circuitry without incurring any additional spikes over the main devices and yet without necessitating any extra control complexities.
- The proposed technique assumes no modulation limitations except for a small duty-cycle loss comparable to that demanded by a conventional snubber.
- Validity of the theoretical analysis for the commutation process is verified by experimental results from a scaled prototype.
- The proposed technique is suitable for high-power advanced applications due to the reduced loss, increased operating frequency, and the widened system bandwidth.

APPENDIX
BRIEF DEDUCTION OF (1)–(6)

A. Total Commutation Duration

For diode-to-switch commutation, the total commutation duration is given by

$$t_{95}(t,k) = L_r\frac{i_{\rm load}(t)}{(1-k)V_{\rm dc}/2} + \frac{\pi}{\omega_o}\frac{\pi - a\cos\left(\dfrac{kV_{\rm dc}/2}{(1-k)V_{\rm dc}/2}\right)}{\pi} + L_r\frac{\sqrt{(1-k)^2-k^2}V_{\rm dc}/2}{Z_o kV_{\rm dc}/2} + L_r\frac{i_{\rm load}(t)}{kV_{\rm dc}/2}. \tag{A1}$$

The right-hand four components correspond to t_6-t_5, t_7-t_6, t_8-t_7, and t_9-t_8, respectively.

For switch-to-diode commutation, the total commutation duration is given by (A2) at the bottom of the page. The right-hand components correspond to $t_{12}-t_{11}$ and $t_{13}-t_{12}$, respectively.

Equations (1) and (2) can be obtained from (A1) and (A2) by multiplying both sides of each by ω_o.

B. Auxiliary Device Peak Current Stress

For diode-to-switch commutation, the peak current i_{sap1} is given by

$$i_{sap1}(t,k) = i_{\rm load}(t) + \frac{\sqrt{(1-k)^2(V_{\rm dc}/2)^2}}{Z_o}. \tag{A3}$$

For switch-to-diode commutation, the peak current i_{sap2} is given by

$$i_{sap2}(t,k) = \frac{\sqrt{(1-k)^2(V_{\rm dc}/2)^2 + [i_{\rm load}(t)Z_o]}}{Z_o} - i_{\rm load}(t). \tag{A4}$$

Equations (3) and (4) can be obtained by dividing both sides of (A3) and (A4) by $V_{\rm dc}/2Z_o$.

C. Auxiliary Device RMS Current Stress

The resonant inductor rms current stress over the switching period resulting from diode-to-switch commutation $i_{lrp\rm rms}$ is

$$t_{1311}(t,k) = \frac{\pi}{\omega_o}\frac{\pi - a\cos\dfrac{kV_{\rm dc}/2}{\sqrt{(1-k)^2(V_{\rm dc}/2)^2+[i_{\rm load}(t)Z_o]^2}} - a\cos\dfrac{(1-k)V_{\rm dc}/2}{\sqrt{(1-k)^2(V_{\rm dc}/2)^2+[i_{\rm load}(t)Z_o]^2}}}{\pi} + L_r\frac{\sqrt{(1-k)^2(V_{\rm dc}/2)^2+[i_{\rm load}(t)Z_0]^2-k^2(V_{\rm dc}/2)^2}-i_{\rm load}(t)Z_o}{kZ_oV_{\rm dc}/2} \tag{A2}$$

$$i_{lrp\rm rms}(t,k,T) = \sqrt{\frac{1}{T}\int_0^{k_{1p}(t,k)} i_{1p}(t_1,k)^2\,dt_1 + \frac{1}{T}\int_0^{k_{2p}(t,k)} i_{2p}(t_1,k)^2\,dt_1 + \frac{1}{T}\int_0^{k_{3p}(t,k)} i_{3p}(t_1,k)^2\,dt_1} \tag{A5}$$

$$\begin{aligned} i_{1n}(t_1,k) &= i_{\rm load}(t) - \frac{(1-k)\sin(\omega_o t_1)}{Z_o}V_{\rm dc}/2 - i_{\rm load}(t)\cos(\omega_o t_1) \\ k_{1n}(t,k) &= \frac{\pi - a\cos\dfrac{kV_{\rm dc}/2}{\sqrt{(1-k)^2(V_{\rm dc}/2)^2+[i_{\rm load}(t)Z_o]^2}} - a\cos\dfrac{(1-k)V_{\rm dc}/2}{\sqrt{(1-k)^2(V_{\rm dc}/2)^2+[i_{\rm load}(t)Z_o]^2}}}{\omega_o} \\ i_{2n}(t_1,k) &= -\frac{\sqrt{(V_{\rm dc}/2)^2[(1-k)^2-k^2]+[i_{\rm load}(t)Z_o]^2}}{Z_o} + i_{\rm load}(t) + \frac{kt_1V_{\rm dc}/2}{L_r} \\ k_{2n}(t,k) &= \left\{\sqrt{[(1-k)^2-k^2](V_{\rm dc}/2)^2+[i_{\rm load}(t)Z_o]^2} - i_{\rm load}(t)Z_o\right\}\frac{L_r}{kZ_oV_{\rm dc}/2} \end{aligned} \tag{A7}$$

given by (A5) at the bottom of the previous page, where

$$i_{1p}(t_1, k) = \frac{V_{\rm dc}(1-k)}{2L_r}\, t_1$$

$$k_{1p}(t, k) = i_{\rm load}(t)\, \frac{L_r}{(1-k)V_{\rm dc}/2}$$

$$i_{2p}(t_1, k) = i_{\rm load}(t) + (1-k)\, \frac{V_{\rm dc}/2}{Z_o}\, \sin(\omega_o t_1)$$

$$k_{2p}(t, k) = \frac{\pi - a\, \cos\left(\dfrac{k}{1-k}\right)}{\omega_o}$$

$$i_{3p}(t_1, k) = \frac{V_{\rm dc}/2}{Z_o}\, \sqrt{(1-k)^2 - k^2} - \frac{kt_1}{L_r}\, V_{\rm dc}/2$$

$$k_{3p}(t, k) = \frac{L_r i_{\rm load}(t)}{kV_{\rm dc}/2} + \frac{L_r\sqrt{(1-k)^2 - k^2}}{kZ_o}.$$

The right-hand three components in (A5) correspond to intervals $t_6 - t_5$, $t_7 - t_6$, and $t_9 - t_7$, respectively.

Similarly, the resonant inductor rms current over the switching period resulting from switch-to-diode commutation i_{lrnrms} is given by

$$i_{lrnrms}(t, k, T) = \sqrt{\frac{1}{T}\int_0^{k_{1n}(t,k)} i_{1n}(t_1, k)^2\, dt_1 + \frac{1}{T}\int_0^{k_{2n}(t,k)} i_{2n}(t_1, k)^2\, dt_1} \tag{A6}$$

as shown in (A7), given at the bottom of the previous page. The right-hand two components in (A6) correspond to $t_{12} - t_{11}$ and $t_{13} - t_{12}$, respectively.

Equations (5) and (6) can be obtained by dividing both sides of (A5) and (A6) by $V_{\rm dc}/2Z_o$.

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Xiaoming Yuan (S'97–M'99) was born in Anhui, China, on May 30, 1966. He received the B.Eng. degree from Shandong University of Technology, China, the M.Eng. degree from Zhejiang University, China, and the Dr.Eng. degree from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1986, 1993, and 1998, respectively, all in electrical engineering.

From 1986 to 1990, he was with Qilu Petrochemical Corporation, China, as a Commissioning Engineer for power system protective relay, adjustable-speed drives, and UPS systems. He is currently a Post-Doctoral Researcher with the Power Electronics and Electrometrology Laboratory, Swiss Federal Institute of Technology, Zurich, Switzerland, where he is working on flexible ac transmission system (FACTS) devices.

Ivo Barbi (M'78–SM'90), for a photograph and biography, see this issue, p. 635.