

A Novel Single-Phase ZCS-PWM High-Power-Factor Boost Rectifier

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Abstract—This paper presents a novel single-phase high-power-factor (HPF) pulsewidth-modulated (PWM) boost rectifier featuring soft commutation of the active switches at zero current (ZC). It incorporates the most desirable properties of conventional PWM and soft-switching resonant techniques.

The input current shaping is achieved with average current mode control and continuous inductor current mode.

This new PWM converter provides ZC turn on and turn off of the active switches, and it is suitable for high-power applications employing insulated gate bipolar transistors (IGBT's).

The principle of operation, the theoretical analysis, a design example, and experimental results from a laboratory prototype rated at 1600 W with 400-Vdc output voltage are presented. The measured efficiency and the power factor were 96.2% and 0.99%, respectively, with an input current total harmonic distortion (THD) equal to 3.94%, for an input voltage with THD equal to 3.8%, at rated load.

Index Terms—AC/DC converter, active power-factor correction, soft-commutation technique.

I. INTRODUCTION

IN THE LAST few years there have been increasing demands for high power factor (HPF) and reduced harmonic distortion in the current drawn from the utility, especially when forthcoming harmonic standards, such as the International Electrotechnical Commission (IEC) 1000-3-2, must be satisfied. Therefore, in these applications, ac/dc converters featuring almost unity power factor have been required.

A variety of circuit topologies are available for power-factor correction, and among the ones usually employed in single-phase power supplies are the boost derived topologies.

The constant switching frequency average current control is the most recommended control technique to achieve high-input power factor [1]. On the other hand, soft-commutation techniques have been of great interest for power quality in switching power supply applications. However, with few exceptions, circulating reactive energy that causes large conduction losses, and frequency modulation are two well-known drawbacks [2], [3].

The overall system efficiency and performance of the pulsewidth-modulated (PWM) converters have been improved by soft-commutation techniques, which limit switching losses. Therefore, with the switching losses removed, the switching

frequency can be increased to reduce the size of magnetic and capacitive components.

In this way, many different zero-voltage switching (ZVS) techniques have been analyzed in several papers [4]–[8]. However, the choice of the soft-switching technique is taking into account the technology of the semiconductor devices used as power switches.

The ZVS and zero-voltage transition (ZVT) techniques are naturally recommended for metal–oxide–semiconductor field-effect transistors (MOSFET's). However, for high-power applications (above 1 kW) insulated gate bipolar transistors (IGBT's) are preferred to power MOSFET's, which have much higher conduction losses than IGBT's. Furthermore, the turn-off losses are still a major part of the total switching losses in IGBT's, and zero-current switching (ZCS) or zero-current transition (ZCT) operation is the most effective for IGBT's [9], [10].

Nevertheless, the ZCS technique presents severe voltage rings across the active switches, and the boost diode has to sustain voltage twice the output voltage [10]. It should be noted that in the last years, a number of soft-commutation techniques were proposed to find an optimum soft-switching PWM technique. However, a desirable technique featuring soft commutation of the power semiconductor devices at ZC and ZV simultaneously, using the fewest number of auxiliary components and without additional drawbacks (voltage/current stresses and cost), was not achieved at this time.

It should be noticed that an experimental analysis for five different dc-to-dc boost topologies, including a new ZCS-PWM technique, was presented in [11]. In that paper, the converters were designed with the same input and output data, switching frequency, and operating at the same main switch. Those experimental results demonstrate that the new ZCS-PWM cell proposed presents less average total power dissipation in the devices in comparison with the tested techniques.

Therefore, in order to improve the efficiency and reduce heat sink size, this paper presents a new principle to achieve ZCS at constant frequency in a power factor correction rectifier with average current control, using IGBT's, based on the ZCS-PWM cell presented in [11] and [12].

II. THE NOVEL TOPOLOGY AND PRINCIPLE OF OPERATION

Fig. 1 shows the new single-phase ZCS-PWM HPF boost rectifier. The commutation cell of this new boost rectifier is formed by one switch S_p (main switch) and one S_a (auxiliary switch), two diodes D_1 and D_2 , two small resonant inductors L_{r1} and L_{r2} , and one resonant capacitor C_r [12].

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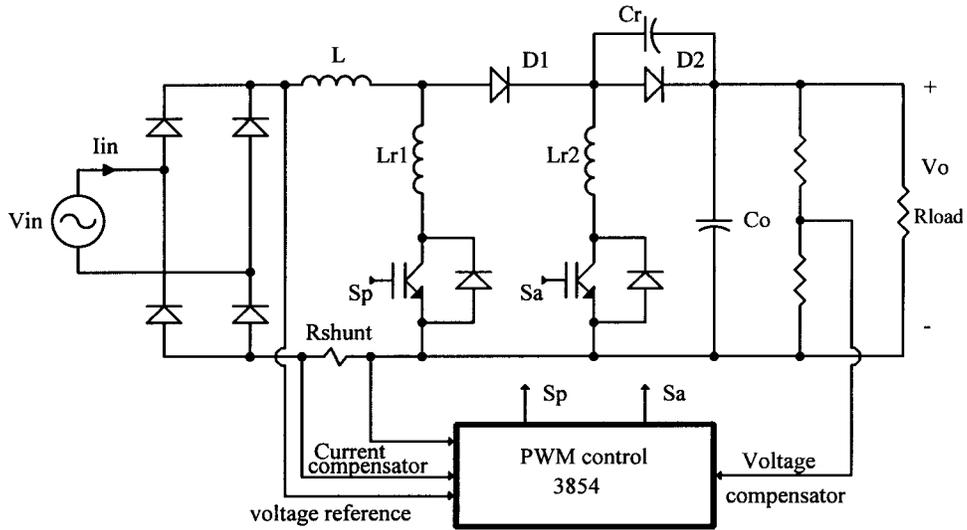


Fig. 1. The novel single-phase ZCS-PWM HPF boost rectifier.

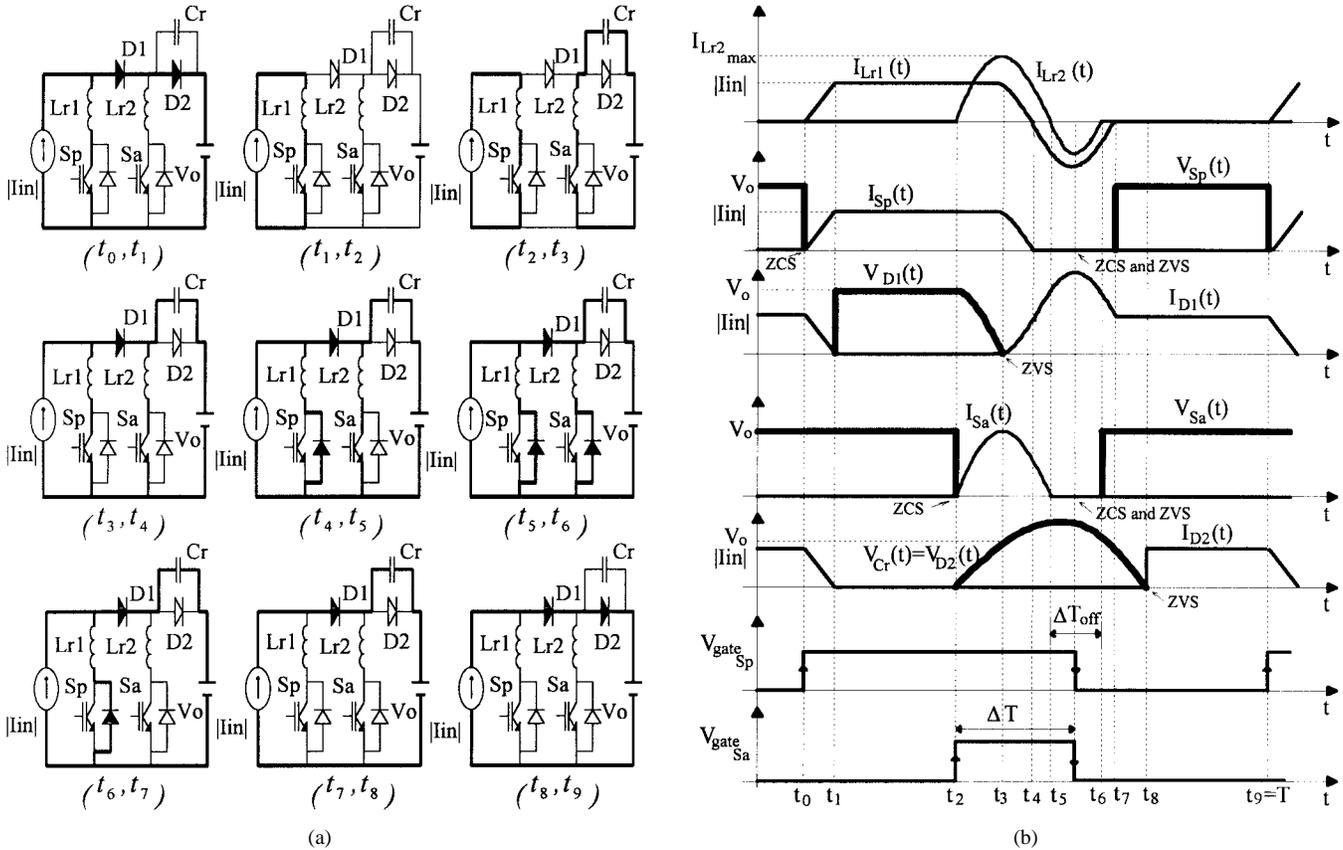


Fig. 2. (a) Topological stages. (b) Main ideal waveforms for the simplified ZCS-PWM HPF boost rectifier during a generic switching period.

In order to explain the operation of this new converter and quantify its behavior, the following conditions are assumed: 1) all components are ideal; 2) the converter is operating in steady state at a fixed switching frequency (f_s); 3) the input voltage (V_{in}) is a sine wave and the output voltage (V_o) is constant; and 4) the switching frequency is much higher than the ac line frequency (f_{line}) and the input filter (L) is large enough to be approximated by a current source ($|I_{in}|$) during a generic switching period (T), where

$$|I_{in}| = \text{Absolute value of the instantaneous input current.}$$

A. Stages of Operation for the Simplified ZCS-PWM HPF Boost Rectifier

Fig. 2(a) shows the nine topological stages of the commutation for the simplified ZCS-PWM HPF boost rectifier, and Fig. 2(b) shows the main ideal waveforms, during a generic switching period.

As can be seen in Fig. 2, the main switch S_p starts conducting at $t = t_0$ and the auxiliary switch S_a at $t = t_2$, both in ZCS. Both switches turn off simultaneously during the time interval $\Delta t_6 = t_6 - t_5$ in ZC and ZV switching. It should be

noticed that the diodes D1 and D2 are also softly commutated under ZVS, and from Fig. 2, it can be seen that only during the switching intervals do the ZCT's take place, and the ZCT time interval is a small fraction of the switching period. The time interval ΔT depends on the resonant parameters and it is independent of the output power.

STAGE 1: Fig. 2(a)—(t_0, t_1): Prior to the turn on of Sp, the current $|I_{in}|$ flows through D1, D2, and V_o . At the instant t_0 , Sp is gated on to start stage 1. In this stage, I_{Lr1} rises linearly from zero up to $|I_{in}|$, while I_{D1} and I_{D2} fall toward zero.

Thanks to the presence of L_{r1} , during the commutation from D1 and D2 to Sp, there are no switching losses.

STAGE 2: Fig. 2(a)—(t_1, t_2): In this stage, the current $|I_{in}|$ remains flowing through L_{r1} and Sp. The remaining semiconductors are in the off state.

STAGE 3: Fig. 2(a)—(t_2, t_3): At the instant t_2 , Sa is turned on. The current I_{Sa} evolves in a resonant way through V_o , C_r , L_{r2} , and Sa. Sp remains conducting the current $|I_{in}|$. Once again, due to the presence of L_{r2} , Sa is turned on with no switching losses. This stage ends when $V_{Cr}(t) = V_o$ at $t = t_3$.

STAGE 4: Fig. 2(a)—(t_3, t_4): At the instant t_3 , D1 also starts conducting. V_{Cr} , I_{Lr1} , and I_{Lr2} change in a resonant way. L_{r1} and L_{r2} are connected in parallel. Stage 4 ends when $I_{Lr1}(t) = 0$ at $t = t_4$.

STAGE 5: Fig. 2(a)—(t_4, t_5): During this stage, the current I_{Lr1} changes its direction and flows through the antiparallel diode of Sp. This stage ends when $I_{Lr2}(t) = 0$ at $t = t_5$.

STAGE 6: Fig. 2(a)—(t_5, t_6): During this stage, the current I_{Lr2} flows through the antiparallel diode of Sa. This stage finishes at the instant $t = t_6$, when I_{Lr2} reaches zero. During this time interval, Sp and Sa are turned off at ZC and ZV.

STAGE 7: Fig. 2(a)—(t_6, t_7): In stage 7, a resonant current flows through the antiparallel diode of Sp. This stage ends when $I_{Lr1}(t) = 0$ at $t = t_7$.

STAGE 8: Fig. 2(a)—(t_7, t_8): In this stage, the input current $|I_{in}|$ flows through D1 and C_r . Therefore, V_{Cr} decreases linearly toward zero, which is reached at instant $t = t_8$.

STAGE 9: Fig. 2(a)—(t_8, t_9): In this stage, the current $|I_{in}|$ flows through D1, D2, and load. This stage ends at $t = t_9$ when Sp is gated on to start the next operation period.

III. ANALYSIS OF COMMUTATION

In order to perform the analysis and derive equations independent of particular parameter values, the following parameters α and β are defined as follows:

$$\alpha = \frac{|I_{in}(t)|}{V_o} \sqrt{\frac{L_{r2}}{Cr}} \quad (1)$$

$$\beta = \frac{L_{r2}}{L_{r1}}. \quad (2)$$

In order to achieve soft commutation at ZCS for both active switches (Sp and Sa), for the described operation mode, the following inequalities should be satisfied:

$$\beta = \frac{L_{r2}}{L_{r1}} < 1 \quad (3)$$

and

$$\alpha_{\max} < \beta \quad (4)$$

where

$$\alpha_{\max} = \frac{I_{\text{imp}}}{V_o} \sqrt{\frac{L_{r2}}{Cr}} \quad (5)$$

$$I_{\text{imp}} = \frac{\sqrt{2}P_{\text{out}}}{\eta V_{\text{in(rms) min}}} \quad (6)$$

where

I_{imp}	peak input current value;
P_{out}	nominal output power;
η	minimum value of efficiency;
$V_{\text{in(rms) min}}$	minimum rms input voltage value.

The time interval Δt_{off} to turn off the switches Sp and Sa simultaneously is governed by (7). So, the time interval ΔT for the control of the auxiliary switch is defined by (8)

$$\Delta t_{\text{off}} = \Delta t_6 = \frac{1}{\omega_{01}} \left\{ \frac{2[\pi - a \cos(-\beta)]}{\sqrt{1+\beta}} \right\} \quad (7)$$

$$\Delta T = \frac{1}{\omega_{02}} \left[\frac{\pi\sqrt{1+\beta}}{2} + 2\pi - a \cos(-\beta) \right] - \frac{\Delta t_{\text{off}}}{2}. \quad (8)$$

Thus

$$\Delta T = \frac{1}{\omega_{01}} \left[\frac{\pi}{2} + \frac{\pi}{\sqrt{1+\beta}} \right] \quad (9)$$

where

$$\omega_{01} = \frac{1}{\sqrt{L_{r2}Cr}} \quad (10)$$

$$\omega_{02} = \omega_{01} \sqrt{1+\beta}. \quad (11)$$

At last, it should be noticed that the maximum value of duty cycle is limited by the resonant time interval $\Delta t = t_7 - t_4$. However, the resonant time interval is a small fraction of the switching period. Therefore, the input current cross-over distortion, and discontinuous-current mode (DCM) operation during this time can be practically eliminated through a correct design procedure.

IV. DESIGN PROCEDURE AND EXAMPLE

The design procedure and example of the new ZCS-PWM HPF boost rectifier is described as follows.

• *Step 1:* Input and output data specifications:

$V_{\text{in(rms)}}$	220 V (nominal rms input voltage);
$V_{\text{in(rms) min}}$	= 187 V, $V_o = 400$ V, and $P_{\text{out}} = 1600$ W;
η	0.95 (minimum value of efficiency);
f_s	20 kHz.

• *Step 2:* Peak input current (I_{imp}):

The peak input current value (I_{imp}) is given by (6). With the parameters shown in Step 1, we obtain

$$I_{\text{imp}} = 12.7 \text{ A.}$$

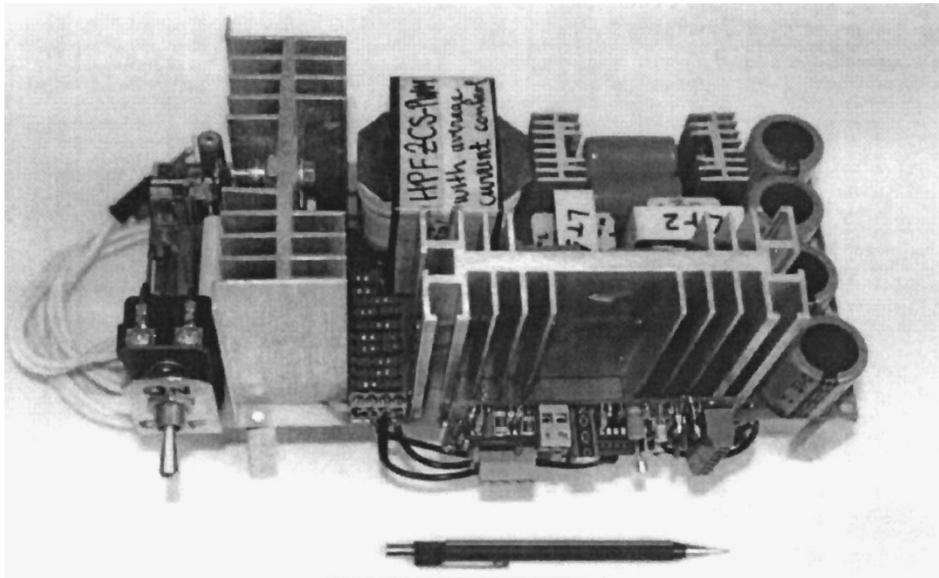


Fig. 4. Test unit of the new single-phase ZCS-PWM HPF boost rectifier.

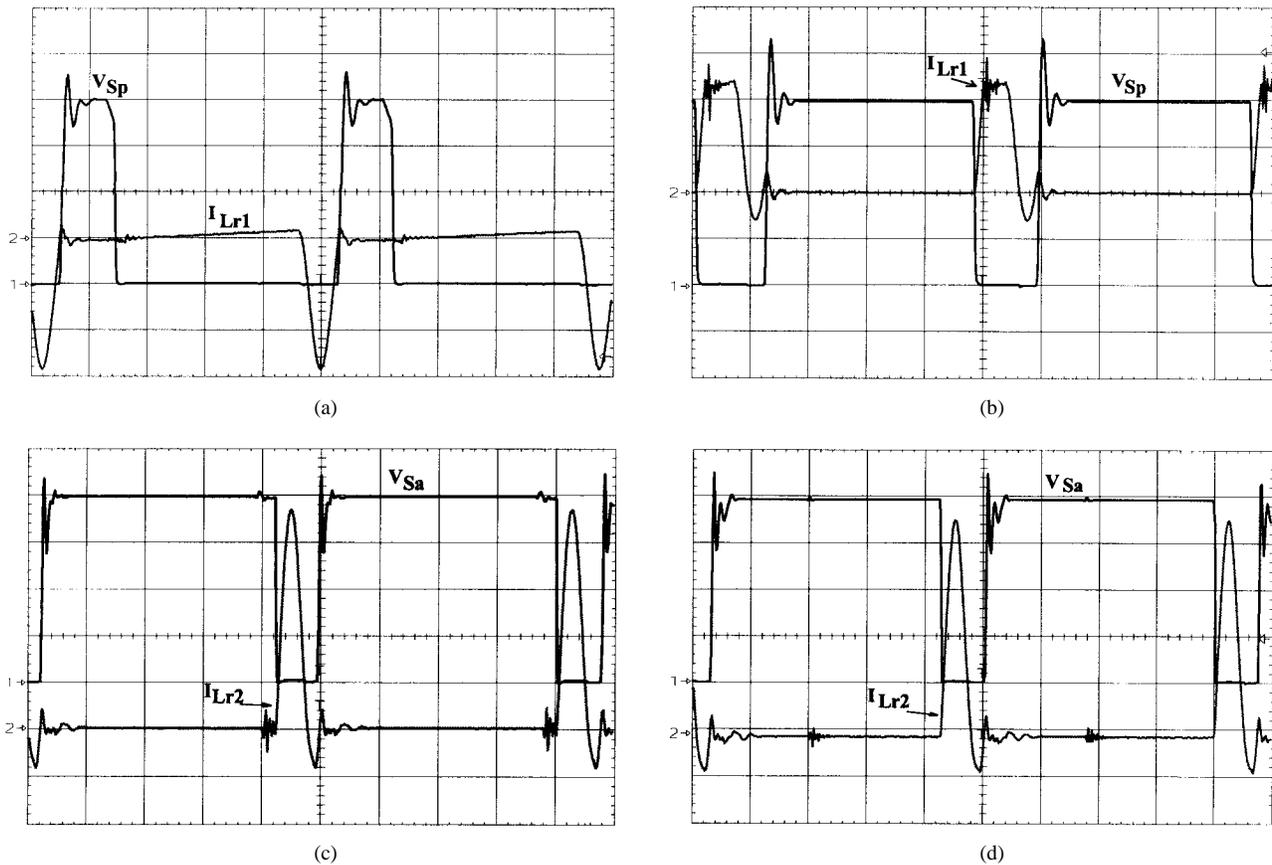


Fig. 5. Voltage across S_p and current through L_{r1} : (a) near $V_{in}(t) = 0$ and (b) near $V_{in}(t) = V_p$. Voltage across S_a and current through L_{r2} : (c) near $V_{in}(t) = 0$ and (d) near $V_{in}(t) = V_p$ at full load. Voltage: 100 V/div; current: 5 A/div; and time scale: 10 μ s/div.

uration voltage $V_{CE(on)}$, and with antiparallel ultrafast soft recovery diode) as power switches, the problems of the recovery currents (voltage stresses on S_p and S_a , which are seen in Fig. 5) due to external antiparallel diodes of S_p and S_a used in this paper, will be eliminated.

The blocking voltage stress on diode D1 is imposed by the interaction between the junction capacitance of diode (D1)

and its reverse recovery current, as shown in Fig. 6(a). This problem can be minimized using the new generation of 600-V ultrafast diodes with low-recovered stored charge (such as MURH860CT), improving EMI/RFI noise.

In the conventional ZCS technique, the boost diode has to sustain voltage twice the output voltage (in this case, >800 V). However, in this new ZCS operation proposed, the maximum

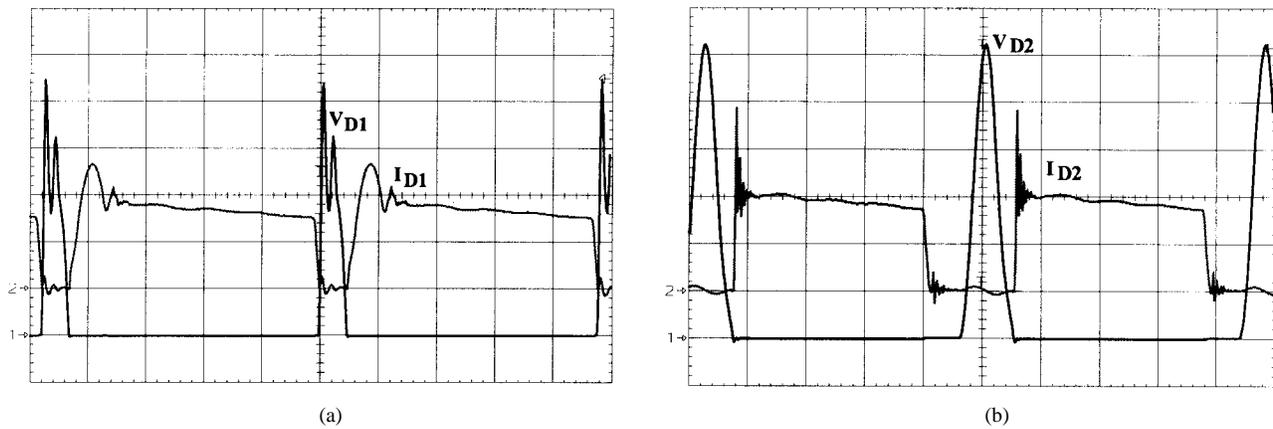


Fig. 6. (a) Voltage and current through D1. (b) Voltage and current through D2 at full load. Voltage: 100 V/div; current: 5 A/div; and time scale: 10 μ s/div.

TABLE I
EXPERIMENTAL LOSSES OF PWM AND ZCS-PWM HPF BOOST RECTIFIERS AT $V_{in(rms)} = 220$ V AND $P_{out} = 1600$ W

Components (losses)	PWM HPF boost		ZCS-PWM HPF boost	
	conduction	switching	conduction	switching
Sp	15.6W	49W	13.3W	~ 0
Sa	—	—	3.7W	~ 0
D1	7.4W	3.3W	9.0W	~ 0
D2	—	—	7.3W	~ 0
D3	—	—	1.1W	~ 0
D4	—	—	0.1W	~ 0
Others	28.7W		26.3W	
Total	104W		60.8W	
Efficiency	93.5%		96.2%	

value of the blocking voltage stress on diode D2 is determined by parameters α and β . In this design example, it is near 600 V, as shown in Fig. 6(b). On the other hand, the voltage stress increases indirectly the conduction losses in several high-voltage ultrafast diodes, which present high forward voltages. So, for better performance in practical applications, we suggested the device BYP100-Siemens (1000 V, low forward voltage $-v_{F(typ)} = 1.75$ V (100°C) and 55-ns ultrafast soft recovery) as diode D2.

The input voltage and input current for the prototype operating at 1600 W are presented in Fig. 7. This result demonstrates that the power factor is practically near unity (0.99) for full load, and the input current total harmonic distortion (THD) is equal to 3.94% for an input voltage with THD equal to 3.8%.

The measured experimental losses are summarized in Table I for the new ZCS-PWM HPF boost and the conventional hard-switching PWM HPF boost rectifiers, both operating at 220-V_{rms} nominal input voltage and 1.6-kW nominal output power. For the conventional PWM boost rectifier, it can be seen that the major power dissipation comes from the switching losses. It should be noted that for the new ZCS-PWM HPF boost rectifier, the additional power losses involved in the auxiliary components are only about 12 W, which is less than 0.8% of the nominal output power.

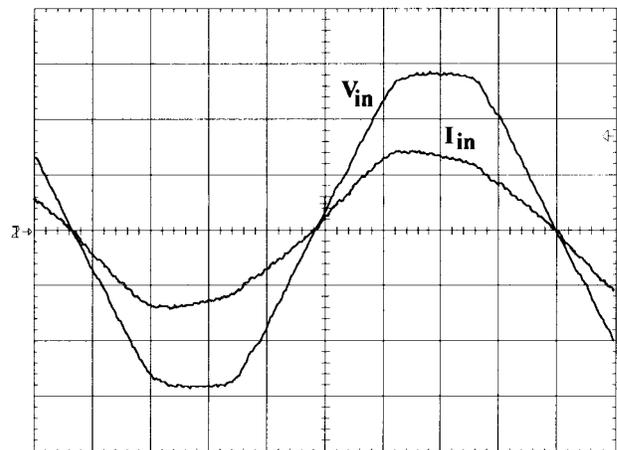


Fig. 7. Input voltage and current (voltage: 100 V/div; current: 10 A/div; and time scale: 2 ms/div).

Fig. 8 shows the measured efficiency of the new ZCS-PWM HPF boost rectifier proposed as a function of the output power in comparison with the conventional hard-switching PWM HPF boost rectifier's efficiency at the same data specifications.

The measured efficiency from the new ZCS-PWM HPF boost rectifier is equal to 96.2%, and from the conventional

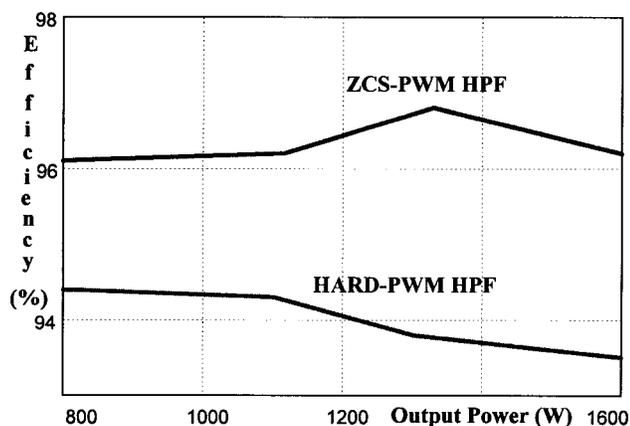


Fig. 8. Experimental efficiency comparison of the new ZCS-PWM HPF boost rectifier and the conventional hard-switching PWM HPF boost rectifier for nominal rms input voltage.

hard-switching PWM HPF boost rectifier it is equal to 93.5% at rated load.

Finally, the commutation energy for this ZCS-PWM cell proposed should be designed to attend the worst operation point (nominal load and low-rms input voltage), and it keeps constant in this converter since V_o (output voltage) is considered regulated. So, the efficiency for light load will not be high in this case. However, this drawback is present in almost all ZCS cells proposed in the literature, and the efficiency at heavy load is usually more a concern than at light load.

Therefore, the new ZCS-PWM technique significantly improves the circuit efficiency, providing a great reduction in the heat sinks size used.

VI. CONCLUSION

This paper has presented a novel single-phase ZCS-PWM HPF boost rectifier rated at 1600 W. Theoretical studies and experimental results for this new ZCS-PWM boost rectifier allow us to draw the following conclusions.

- HPF is achieved through average current control for a wide load and wide input voltage range. The total harmonic distortion of the input current is very low and it is in agreement with IEC-555-2.
- Soft commutation (ZCS) is achieved for the active switches from nonload up to full load.
- The passive switches (D1 and D2) were also softly commutated (ZVS).
- The converter is regulated by the conventional PWM technique at constant frequency.
- Latching of IGBT's due to turn off never occurs. This relieves its reverse bias safe operating area (RBSOA) stresses.
- Low-conduction losses are verified in the devices in spite of an additional diode in series with the load.
- The converter is able to provide efficiency above 96% for a wide load, thus providing a great reduction in the heat sinks size.

Therefore, this new ZCS-PWM HPF boost rectifier combines the advantages of the PWM and ZCS techniques, improving the converter performance and maintaining high efficiency.

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