

A New ZVS Semiresonant High Power Factor Rectifier with Reduced Conduction Losses

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Abstract—This paper presents a novel single-phase unity power factor rectifier, which features critical conduction mode and zero-voltage switching. The reduced conduction losses are achieved by the employment of a single converter, instead of the typical configuration composed of a front-end rectifier followed by a boost converter. Theoretical analysis, a design example, and experimental results of a 300-W converter with 127-V_{rms} input voltage and 400-V_{DC} output voltage are presented.

Index Terms—Power factor correction, rectifiers, soft commutation.

I. INTRODUCTION

THE converter usually employed for single-phase power factor correction consists of a front-end diode rectifier bridge followed by a boost converter. This converter, however, presents conduction and commutation losses, which will contribute to the reduction in the efficiency of the converter. The commutation losses occur due to the hard switching of power semiconductors, and the conduction losses are representative because there are always three semiconductors in the current flow path.

The reduction of the commutation losses can be achieved by different techniques, which can employ zero-voltage switching (ZVS) or zero-current switching (ZCS) [1]–[3]. With these converters, the efficiency is improved, but the conduction losses are significant.

The converter presented in [4] presents much lower conduction losses, due to the fact that there are always two semiconductors in the current flow path. However, the commutation losses problem is not solved.

In order to improve the efficiency even more, power factor correction rectifiers with soft commutation and reduced conduction losses were proposed in [5] and [6]. Due to complexity and cost, these converters are suitable for high-power single-phase applications, once they employ the continuous conduction mode to achieve high power factor.

For low-power single-phase applications, the boost converter with the discontinuous conduction mode using the voltage follower technique [7] can be employed. This technique, however, naturally presents hard commutation and input current distortion.

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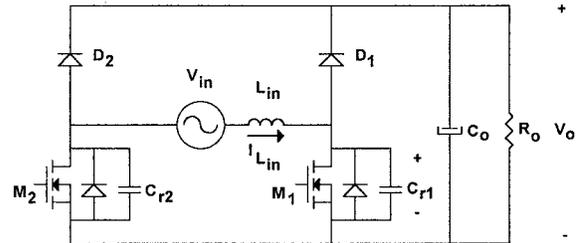


Fig. 1. Proposed converter.

Another solution for low-power single-phase applications is the boost converter in critical conduction mode, which features high power factor with simplicity and low cost [8]. However, this converter presents commutation losses and expressive conduction losses.

In order to obtain high power factor and high efficiency, a new converter employing a ZVS semiresonant boost converter with reduced conduction losses is proposed in this paper.

II. THE PROPOSED CONVERTER

The main topology is depicted in Fig. 1. This converter will operate as two boost converters, one for each half line cycle. When the input current is positive, the body diode of MOSFET M_2 or MOSFET M_2 itself, depending on the MOSFET's channel resistance, will conduct, while MOSFET M_1 and diode D_1 will perform the boost function with power factor correction in critical conduction mode. When the input current is in the reverse direction, MOSFET M_2 and diode D_2 will perform the boost function with power factor correction in critical conduction mode, while the body diode of MOSFET M_1 or MOSFET M_1 will conduct. The resonant capacitors C_{r1} and C_{r2} , along with the input inductor L_{in} , will be responsible for the ZVS of M_1 and M_2 employing the semiresonance.

The critical conduction mode will ensure near unity power factor with variable switching frequency.

III. PRINCIPLE OF OPERATION AND COMMUTATION ANALYSIS

In order to analyze the commutation process, it is considered that the minimum switching frequency is much higher than the ac mains frequency. Thus, the sinusoidal input voltage can be considered constant for each period of operation. The output voltage can be represented by a constant dc voltage source. The MOSFET's M_1 and M_2 will present a protection circuit [9], which will prevent them from conducting when their drain-to-source voltage is greater than zero and the gate signal is high.

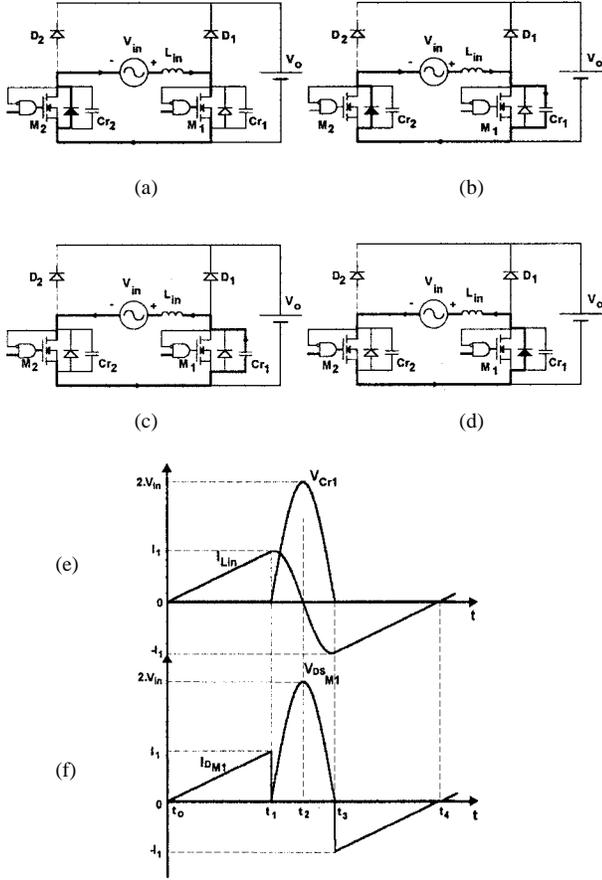


Fig. 2. Topological stages and main waveforms for the first mode of operation.

This protection circuit, based on the dual-thyristor principle, will ensure the ZVS commutation.

In this converter, there are two different operation modes. The first mode occurs when the voltage across C_{r1} or C_{r2} does not reach the output voltage V_o . The second mode occurs when the voltage across C_{r1} or C_{r2} reaches the output voltage V_o , conducting, therefore, the diodes D_1 or D_2 .

A. First Mode

The first operation mode, shown in Fig. 2, occurs when the instantaneous input voltage is near the zero crossing and it does not ensure sufficient magnetization of input inductor L_{in} in order to charge capacitors C_{r1} or C_{r2} up to the output voltage. Nevertheless, the ZVS is still ensured in this operation mode. This operation mode is later explained in detail.

1st Stage (t_o, t_1)—Linear Stage [Fig. 2(a)]: At the beginning of this stage (t_o), the current through L_{in} is null and the voltage across C_{r1} and C_{r2} is null. The MOSFET's M_1 and M_2 are turned on and the input current flows through them. The input current will flow through the body diode of MOSFET M_2 or through the MOSFET's channel, depending on its on resistance

$$V_{Cr1}(t) = 0 \quad (1)$$

$$I_{Lin}(t) = \frac{V_{in}}{L_{in}} \cdot t. \quad (2)$$

In order to obtain a high power factor, the on time (t_{on}) of the MOSFET's must be maintained constant during all the ac mains period. At the end of this stage, the inductor current is defined by (3)

$$I_{Lin}(t_1) = \frac{V_{in}}{L_{in}} \cdot t_{on} = I_1 \quad (3)$$

$$\Delta t_1 = t_{on} = \frac{I_1 \cdot L_{in}}{V_{in}} = \frac{\alpha}{\omega_o} \quad (4)$$

where

$$\alpha = \frac{Z_o \cdot I_1}{V_{in}} \quad (5)$$

$$\omega_o = \frac{1}{\sqrt{L_{in} \cdot C_{r1}}} \quad (6)$$

$$Z_o = \sqrt{\frac{L_{in}}{C_{r1}}}. \quad (7)$$

2nd Stage (t_1, t_2)—Resonant Stage [Fig. 2(b)]: At time t_1 , MOSFET M_1 and M_2 are turned off. The input current flows through C_{r1} and begins to charge it in a resonant way

$$V_{Cr1}(t) = V_{in} \cdot [1 - \cos(\omega_o \cdot t)] + Z_o \cdot I_1 \cdot \sin(\omega_o \cdot t) \quad (8)$$

$$I_{Lin}(t) = \frac{V_{in}}{Z_o} \cdot \sin(\omega_o \cdot t) + I_1 \cdot \cos(\omega_o t). \quad (9)$$

This stage finishes when $I_{Lin}(t) = 0$. The duration of this stage is, therefore, defined by

$$\Delta t_2 = \frac{1}{\omega_o} \cdot (\pi - \tan^{-1} \alpha). \quad (10)$$

At the end of this stage, the voltage across C_{r1} will not reach the value of the output voltage V_o . This voltage is defined by

$$V_{Cr1}(t_2) = V_{in} \cdot (1 + \sqrt{1 + \alpha^2}). \quad (11)$$

3rd Stage (t_2, t_3)—Resonant Stage [Fig. 2(c)]: At instant t_2 , the input inductor current becomes null. At this time, the control circuit will apply a gate signal to the drive circuits of both MOSFET's. However, only MOSFET M_2 begins to conduct immediately, because the dual-thyristor circuit prevents MOSFET M_1 from conducting while its drain-to-source voltage does not reach zero. The current I_{Lin} inverts its direction and a resonant stage makes the discharge of capacitor C_{r1}

$$V_{Cr1}(t) = V_{in} + V_{in} \cdot \sqrt{1 + \alpha^2} \cdot \cos(\omega_o t) \quad (12)$$

$$I_{Lin}(t) = -\frac{V_{in}}{Z_o} \cdot \sqrt{1 + \alpha^2} \cdot \sin(\omega_o t). \quad (13)$$

This stage finishes when the voltage across C_{r1} becomes null. The duration of this stage is defined by

$$\Delta t_3 = \frac{1}{\omega_o} \cdot (\pi - \tan^{-1} \alpha). \quad (14)$$

At the end of this stage, the inductor current will be defined by

$$I_{Lin}(t_3) = -I_1. \quad (15)$$

4th Stage (t_3, t_4)—Linear Stage [Fig. 2(d)]: When the voltage across C_{r1} becomes null at t_3 , the body diode of MOSFET M_1 begins to conduct the input inductor current. The current through L_{in} begins to increase linearly

$$I_{Lin}(t) = -I_1 + \frac{V_{in}}{L_{in}} \cdot t \quad (16)$$

$$V_{Cr1}(t) = 0. \quad (17)$$

This stage finishes when $I_{Lin} = 0$. The duration of this stage is defined by

$$\Delta t_4 = \frac{L_{in} \cdot I_1}{V_{in}} = \frac{\alpha}{\omega_o}. \quad (18)$$

During this stage, the MOSFET M_1 can be turned on. Thus, the MOSFET M_1 will commute under ZVS.

The input inductor current and the voltage across C_{r1} for one operation period in this mode are shown in Fig. 2(e). In Fig. 2(f) shows the voltage and current in MOSFET M_1 , where the ZVS characteristics can be noticed.

B. Second Mode

The second operation mode, shown in Fig. 3, occurs for the remaining time of the sinusoidal input voltage. In this mode, the voltage across C_{r1} or C_{r2} will reach the output voltage V_o , ensuring the conduction of diodes D_1 or D_2 , respectively. This operation mode is later explained in detail.

In the following analysis, the commutation process will be analyzed for the peak of the sinusoidal input voltage (V_{inp}).

1st Stage (t_o, t_1)—Linear Stage [Fig. 3(a)]: At the beginning of this stage (t_o), the current through L_{in} is null and the voltages across C_{r1} and C_{r2} are null. The MOSFET's M_1 and M_2 are turned on and the input current flows through them. The input current will flow through the body diode of MOSFET M_2 or through the MOSFET's channel, depending on its on resistance

$$V_{Cr1}(t) = 0 \quad (19)$$

$$I_{Lin}(t) = \frac{V_{inp}}{L_{in}} \cdot t. \quad (20)$$

In order to simplify the analysis, the voltage V_{Cr1} and the current I_{Lin} can be normalized

$$\bar{V}_{Cr1}(t) = 0 \quad (21)$$

$$\bar{I}_{Lin}(t) = \frac{\omega_o \cdot t}{\beta} \quad (22)$$

where

$$\beta = \frac{V_o}{V_{inp}} \quad (23)$$

$$\bar{V}_{Cr1}(t) = \frac{V_{Cr1}(t)}{V_o} \quad (24)$$

$$\bar{I}_{Lin}(t) = \sqrt{\frac{L_{in}}{C_{r1}}} \cdot \frac{I_{Lin}}{V_o}. \quad (25)$$

In order to obtain a high power factor, the on time (t_{on}) of MOSFET M_1 must be maintained constant during all the ac mains period. Thus, the peak of the current through L_{in} (I_p) will follow the sinusoidal shape of the input voltage.

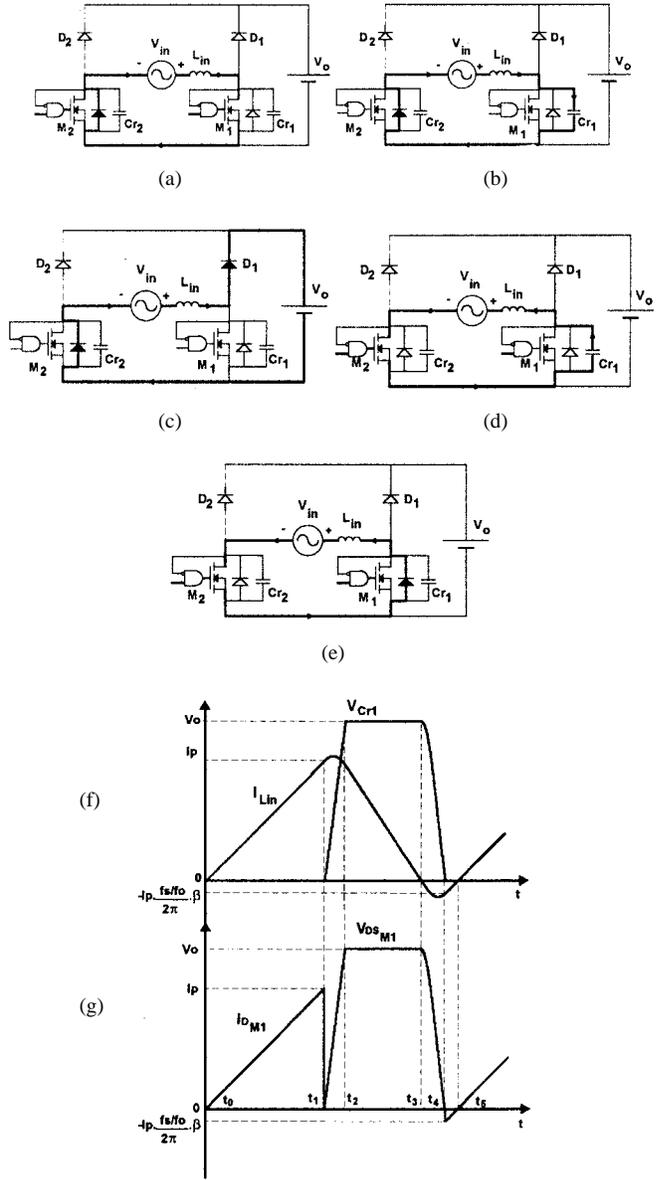


Fig. 3. Topological stages and main waveforms for the second mode of operation.

2nd Stage (t_1, t_2)—Resonant Stage [Fig. 3(b)]: At time t_1 , MOSFET's M_1 and M_2 are turned off. The input current flows through C_{r1} and begins to charge it in a resonant way

$$V_{Cr1}(t) = V_{inp} \cdot [1 - \cos(\omega_o \cdot t)] + Z_o \cdot I_p \cdot \sin(\omega_o t) \quad (26)$$

$$I_{Lin}(t) = \frac{V_{inp}}{Z_o} \cdot \sin(\omega_o t) + I_p \cdot \cos(\omega_o t). \quad (27)$$

Normalizing (26) and (27),

$$\bar{V}_{Cr1}(t) = \frac{1}{\beta} \cdot [1 - \cos(\omega_o \cdot t)] + \frac{2 \cdot \pi \cdot (\beta - 1)}{\beta^2 \cdot f_s / f_o} \cdot \sin(\omega_o \cdot t) \quad (28)$$

$$\bar{I}_{Lin}(t) = \frac{1}{\beta} \cdot \sin(\omega_o \cdot t) + \frac{2 \cdot \pi \cdot (\beta - 1)}{\beta^2 \cdot f_s / f_o} \cdot \cos(\omega_o \cdot t). \quad (29)$$

This stage finishes when $V_{Cr1}(t) = V_o$, or $\bar{V}_{Cr1}(t) = 1$.

3rd Stage (t_2, t_3)—Linear Stage [Fig. 3(c)]: At instant t_2 , the voltage $V_{Cr1}(t)$ is equal to V_o . The diode D_1 begins to conduct the input current. The input inductor begins to demagnetize linearly, and the current begins to fall at the same rate

$$V_{Cr1}(t) = V_o \quad (30)$$

$$I_{Lin}(t) = I_{Lin}(t_2) - \frac{(V_o - V_{in_p}) \cdot t}{L_{in}}. \quad (31)$$

Normalizing (30) and (31),

$$\bar{V}_{Cr1}(t) = 1 \quad (32)$$

$$\bar{I}_{Lin}(t) = \sqrt{\left(\frac{2 \cdot \pi \cdot (\beta - 1)}{\beta^2 \cdot f_s / f_o}\right)^2 - 1} + \frac{2}{\beta} - \frac{1}{\beta}(\beta - 1) \cdot \omega_o \cdot t. \quad (33)$$

This stage finishes when the input inductor current becomes null.

4th Stage (t_3, t_4)—Resonant Stage [Fig. 3(d)]: At instant t_3 , the input inductor current becomes null and diode D_1 turns off. At this time, the control circuit will apply a gate signal to the drive circuits of both MOSFET's. However, only MOSFET M_2 begins to conduct immediately, because the dual-thyristor circuit prevents MOSFET M_1 from conducting while its drain-to-source voltage does not reach zero. The current I_{Lin} inverts its direction and a resonant stage makes the discharge of capacitor C_{r1}

$$V_{Cr1}(t) = (V_o - V_{in_p}) \cdot \cos(\omega_o t) + V_{in_p} \quad (34)$$

$$I_{Lin}(t) = \frac{(V_{in_p} - V_o)}{Z_o} \cdot \sin(\omega_o t). \quad (35)$$

Normalizing,

$$\bar{V}_{Cr1}(t) = \frac{1}{\beta} [(\beta - 1) \cdot \cos(\omega_o \cdot t) + 1] \quad (36)$$

$$\bar{I}_{Lin}(t) = \frac{1}{\beta} (1 - \beta) \cdot \sin(\omega_o \cdot t). \quad (37)$$

This stage finishes when the voltage across C_{r1} becomes null.

The output voltage must be greater than double that of the input voltage in order to ensure the complete discharge of C_{r1} and guarantee the ZVS.

5th Stage (t_4, t_5)—Linear Stage [Fig. 3(e)]: When the voltage across C_{r1} becomes null at t_4 , the body diode of MOSFET M_1 begins to conduct the input inductor current. The current through L_{in} begins to increase linearly

$$I_{Lin}(t) = -\frac{V_{in_p}}{Z_o} \cdot \sqrt{\frac{V_o}{V_{in_p}} \cdot \left(\frac{V_o}{V_{in_p}} - 2\right)} + \frac{V_{in_p}}{L_r} \cdot t \quad (38)$$

$$V_{Cr1}(t) = 0. \quad (39)$$

Normalizing,

$$\bar{I}_{Lin}(t) = -\sqrt{\frac{\beta - 2}{\beta}} + \frac{1}{\beta} \cdot \omega_o \cdot t \quad (40)$$

$$\bar{V}_{Cr1}(t) = 0. \quad (41)$$

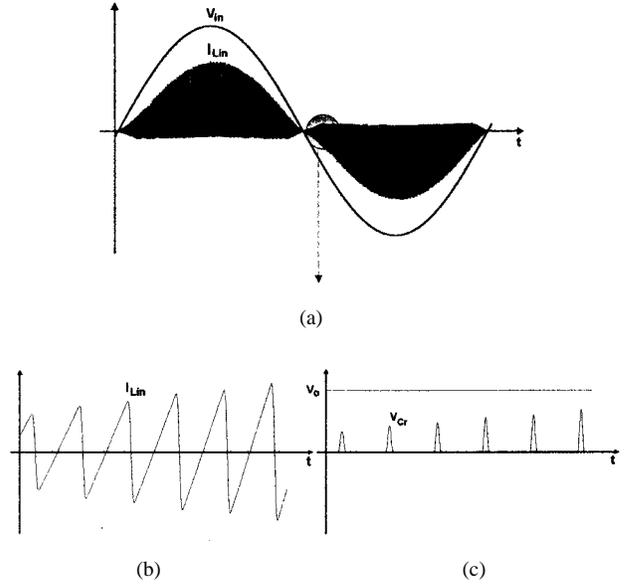


Fig. 4. (a) Input inductor current waveform in an ac mains period. (b) Input inductor current near zero crossing of input voltage. (c) Resonant capacitor voltage near zero crossing of input voltage.

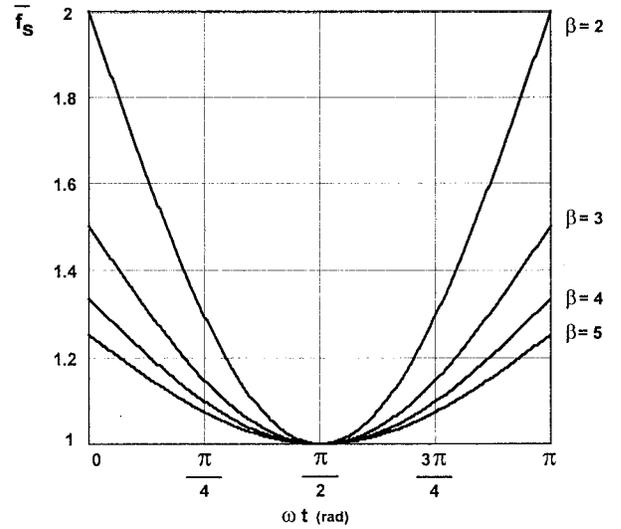


Fig. 5. Normalized switching frequency variation along half line cycle.

This stage finishes when $I_{Lin} = 0$. During this stage, the MOSFET M_1 can be turned on. Thus, the MOSFET M_1 will commutate under ZVS.

The input inductor current and the voltage across C_{r1} for one operation period are shown in Fig. 3(f). Fig. 3(g) shows the voltage and current in MOSFET M_1 . This figure is normalized by the peak of the input inductor current at the peak of the sinusoidal input voltage.

Symmetrical operation stages will occur when the input voltage has a reverse polarity.

IV. CONVERTER ANALYSIS IN AN AC MAINS PERIOD

The semiresonant boost converter operating in critical conduction mode can achieve a high power factor with constant on time of MOSFET's M_1 and M_2 . Thus, the peak current

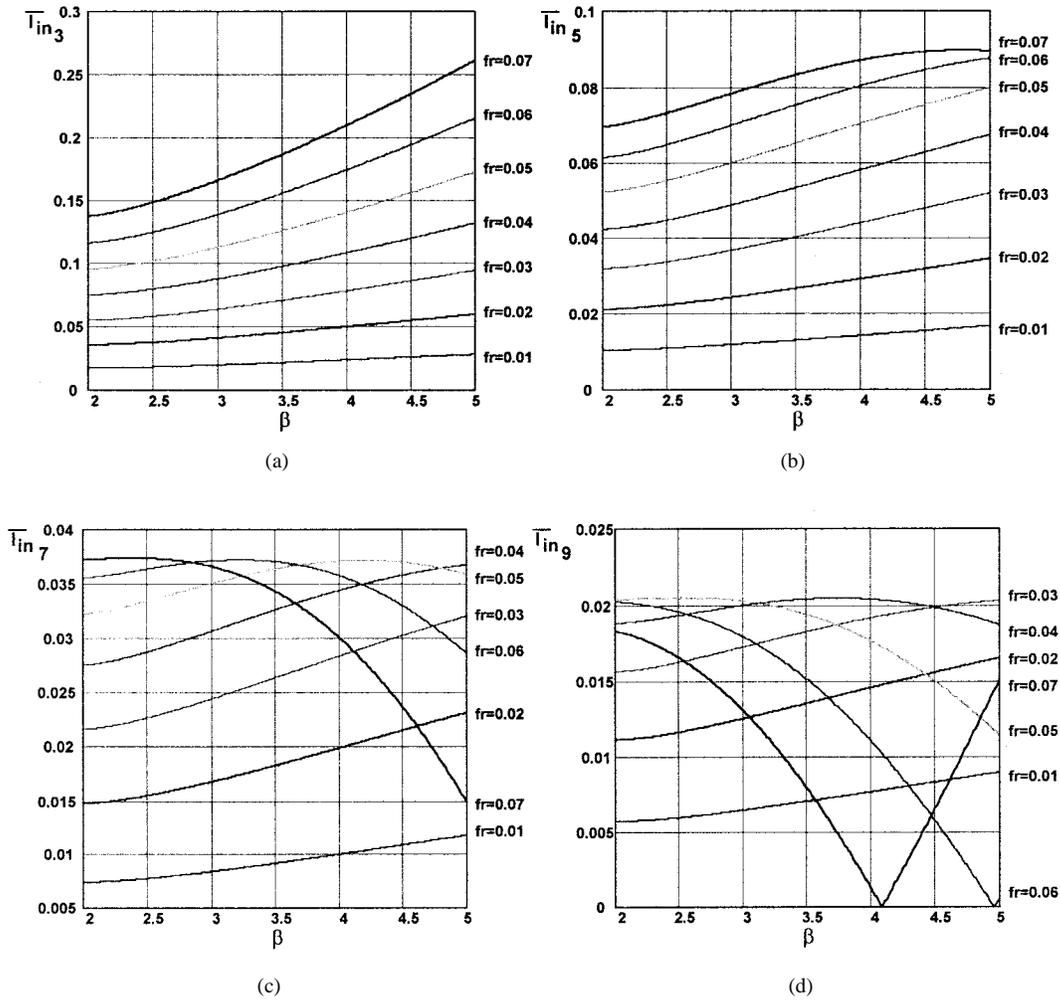


Fig. 6. Most relevant input harmonics. (a) Third harmonic. (b) Fifth harmonic. (c) Seventh harmonic. (d) Ninth harmonic.

through L_{in} will naturally follow the sinusoidal shape of the input voltage, as shown in Fig. 4(a).

However, during a small amount of time, near the zero crossing of the input voltage, the average value of the input inductor current will be null, as shown in Fig. 4(b). This occurs because the converter operates in the *First Mode*, as described in the previous section. During this mode, the voltage across the resonant capacitor C_{r1} or C_{r2} does not reach the output voltage [Fig. 4(c)] and the circuit will not transfer energy from the input to the output. Therefore, only reactive power will be present during this small interval, which will be responsible for a small power factor degradation. However, after this small time, when the instantaneous input voltage increases, the converter will operate in the *Second Mode*, which will ensure energy transfer from the input to the output.

As the converter will operate in critical conduction mode, the switching frequency will be variable along the cycle of the input voltage.

The critical conduction mode will also ensure that the voltage transfer ratio will be defined by

$$\beta = \frac{V_o}{V_{inp}} = \frac{\sin(\omega t)}{1 - D(\omega t)} \quad (42)$$

where $D(\omega t)$ is the equivalent duty cycle for each switching period.

Thus,

$$D(\omega t) = 1 - \frac{\sin(\omega t)}{\beta}. \quad (43)$$

The switching frequency can be defined as a function of the duty cycle and the conduction time of MOSFET M_1 or M_2

$$f_s(\omega t) = \frac{D(\omega t)}{t_{on}} \quad (44)$$

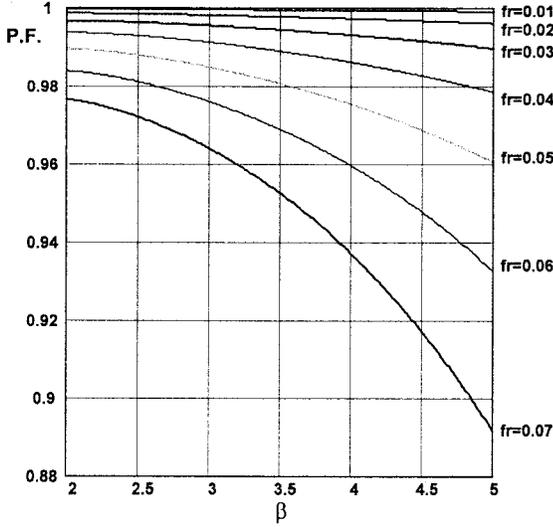
where

$$t_{on} = \frac{\left(1 - \frac{1}{\beta}\right)}{f_{s_{min}}}. \quad (45)$$

Thus, the switching frequency variation along the half cycle of the input voltage and normalized as a function of the minimum switching frequency is defined by (46) and depicted in Fig. 5

$$\bar{f}_s = \frac{f_s(\omega t)}{f_{s_{min}}} = \frac{\beta - \sin(\omega t)}{\beta - 1} \quad (46)$$

where $f_{s_{min}}$ is the minimum switching frequency.


 Fig. 7. Power factor variation as a function of β .

The normalized rms values of each individual harmonic of the filtered input current are defined by (47), shown at the bottom of the page, where

$$f_r = \frac{f_{s\min}}{2 \cdot \pi \cdot f_o} \quad (48)$$

$$\theta_1 = \sin^{-1} \left(\frac{\beta}{1 + \sqrt{1 + \omega_o^2 \cdot t_{\text{on}}^2}} \right) \quad (49)$$

$$\bar{I}_{\text{in}_n} = \frac{I_{\text{in}_n}}{I_{\text{in}_1}} \quad (50)$$

and I_{in_1} is the rms value of the fundamental input current.

The normalized rms value for the most relevant input current harmonics as a function of β and f_r are presented in Fig. 6.

The power factor obtained for this type of converter when the switching frequency harmonics are eliminated is defined by (51), shown at the bottom of the page.

The power factor as a function of the gain β for some relations of f_r is shown in Fig. 7. It can be noticed that the power factor is very high for all the situations.

The voltage ratio $\beta = V_o/V_{\text{in}_p}$ as a function of \bar{I}_o, t_{on} , and f_o can be obtained through the expression of the average

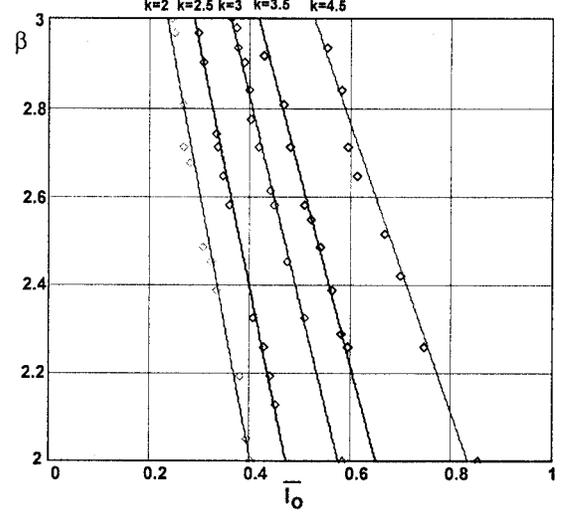


Fig. 8. Output characteristics.

output current for a switching period T , defined in

$$I_{\text{Oavg}} = \frac{1}{T} \cdot \int_0^{T-t_{\text{on}}} \left[I_p + \left(\frac{-I_p \cdot \beta \cdot \frac{f_s(t)}{f_o}}{\frac{2 \cdot \pi}{T-t_{\text{on}}}} \right) \cdot t \right] dt. \quad (52)$$

Thus,

$$I_{\text{Oavg}} = \frac{1}{4} \cdot I_p \cdot \frac{\left(\frac{2 \cdot \pi}{\beta} - \frac{f_s(t)}{f_o} \right)}{\pi}. \quad (53)$$

Replacing $f_s(t)$ and β in (53) by (46) and (42), respectively, integrating the expression for one ac mains period, and normalizing the output current, results in the output characteristic, defined by

$$\beta = \frac{2 \cdot \pi}{5} \cdot t_{\text{on}} \cdot f_o \cdot \left[\frac{4}{\pi} + \frac{2}{t_{\text{on}} \cdot f_o \cdot \pi^2} - \bar{I}_o \right] \quad (54)$$

where

$$\bar{I}_o = \frac{I_o}{I_{\text{Onorm}}} \quad (55)$$

I_{Onorm} is the output current for rated power.

$$\bar{I}_{\text{in}_n} = \frac{2}{\pi} \cdot \left[\int_{\theta_1}^{\pi-\theta_1} \frac{(f_r \cdot \beta \cdot \sin(\omega t) - f_r \cdot \beta^2 + \beta \cdot \sin(\omega t) - \sin(\omega t))}{\beta - 1} \cdot \sin(n \cdot \omega t) d\omega t \right] \quad (47)$$

$$\text{P.F.} = \frac{1}{\sqrt{\pi}} \cdot \frac{f_r \cdot \beta \cdot (\pi - 4 \cdot \beta) + \pi \cdot (\beta - 1)}{\sqrt{f_r \cdot (-8 \cdot \beta^3 + \pi \cdot \beta^2 \cdot f_r - 8 \cdot \beta^3 \cdot f_r + 2 \cdot \pi \cdot \beta^4 \cdot f_r + 2 \cdot \pi \cdot \beta^2 - 2 \cdot \pi \cdot \beta + 8 \cdot \beta^2) + \pi \cdot (\beta - 1)^2}} \quad (51)$$

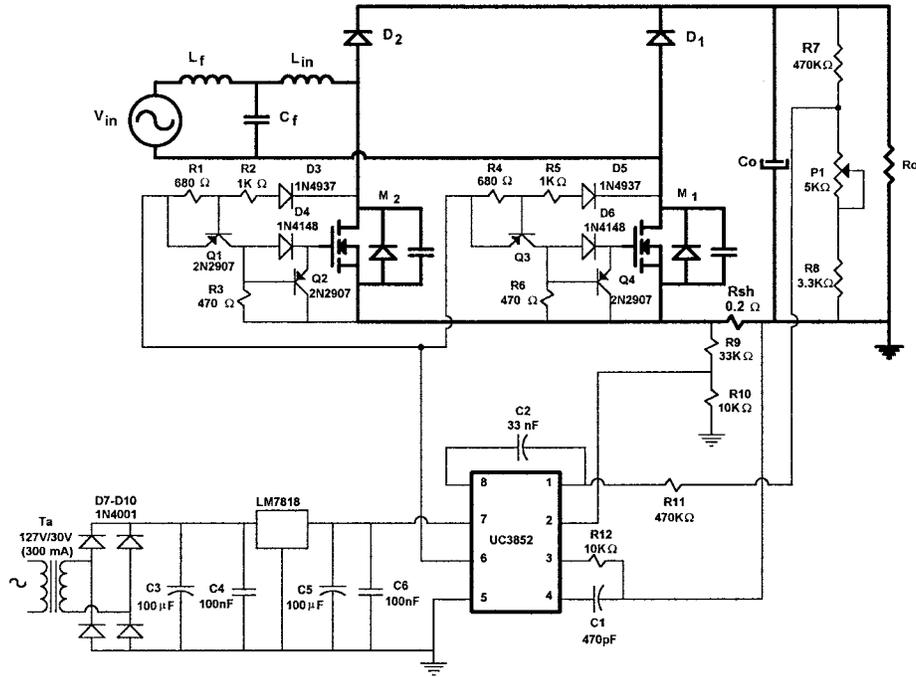


Fig. 9. Complete diagram of the implemented prototype.

The theoretical and experimental output characteristic of this converter are shown in Fig. 8 with $k = t_{on} \cdot f_o$. It can be observed that, in order to maintain a constant output voltage for all load situations, the on time must be varied.

V. DESIGN PROCEDURE AND EXAMPLE

The analysis previously performed in this paper shows that the converter is suitable for the 110–127-V ac input, with a high power factor for all load situations.

A simplified design procedure and example is described in this section as follows.

1) Input data:

$$V_o = 400 \text{ V}, \quad V_{in} = 127 \text{ Vrms}$$

$$P_o = 300 \text{ W}, \quad f_{s_{min}} = 55 \text{ kHz}, \quad f_o = 500 \text{ kHz}.$$

2) Determination of β and t_{on} :

$$\beta = \frac{V_o}{V_{in_p}} = \frac{400}{179.6} = 2.23.$$

Once $\beta \geq 2$, the ZVS commutation is ensured for all the ac mains period, even for near zero crossing of the input voltage

$$t_{on} = \frac{\beta - 1}{\beta \cdot f_{s_{min}}} = 11 \mu\text{s}.$$

3) Determination of the input inductance L_{in} :

$$L_{in} = \frac{V_o^2 \cdot (\beta - 1)}{4 \cdot \beta^3 \cdot P_o \cdot f_{s_{min}}} = \frac{400^2 \cdot (2 \cdot 227 - 1)}{4 \cdot 2 \cdot 227^3 \cdot 55 \cdot 10^3}$$

$$L_{in} = 295.7 \mu\text{H}.$$

4) Determination of the maximum switching frequency and f_r :

$$f_{s_{max}} = \frac{\beta \cdot f_{s_{min}}}{\beta - 1} = 108.9 \text{ kHz}$$

$$f_r = \frac{f_{s_{min}}}{2 \cdot \pi \cdot f_o} = \frac{55 \cdot 10^3}{2 \cdot \pi \cdot 500 \cdot 10^3} = 0.018.$$

5) Determination of the resonant capacitor:

$$f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{in} \cdot C_{r1}}}$$

$$C_{r1} = C_{r2} = \frac{1}{4 \cdot \pi^2 \cdot f_o^2 \cdot L_{in}} = 410 \text{ pF}.$$

6) Peak input inductor current and rms value of fundamental input current:

$$I_p = \frac{V_p}{L_{in}} \cdot t_{on} = \frac{179.6 \times 11 \times 10^{-6}}{295.7 \times 10^{-6}} = 6.68 \text{ A}$$

$$I_{1_{rms}} = \frac{P_o}{V_{in}} = \frac{300}{127} = 2.36 \text{ A}.$$

7) Expected harmonics:

Through Fig. 6, for $f_r \approx 0.02$, $\beta = 2.23$, and $I_{1_{rms}} = 2.23$, the most relevant harmonics can be determined:

$$I_{3_{rms}} = 0.081 \text{ A}, \quad I_{5_{rms}} = 0.048 \text{ A}$$

$$I_{7_{rms}} = 0.034 \text{ A}, \quad I_{9_{rms}} = 0.025 \text{ A}.$$

8) Expected power factor:

Examining Fig. 7, for $f_r \approx 0.02$, it can be noticed that the expected power factor will be better than 0.995. By

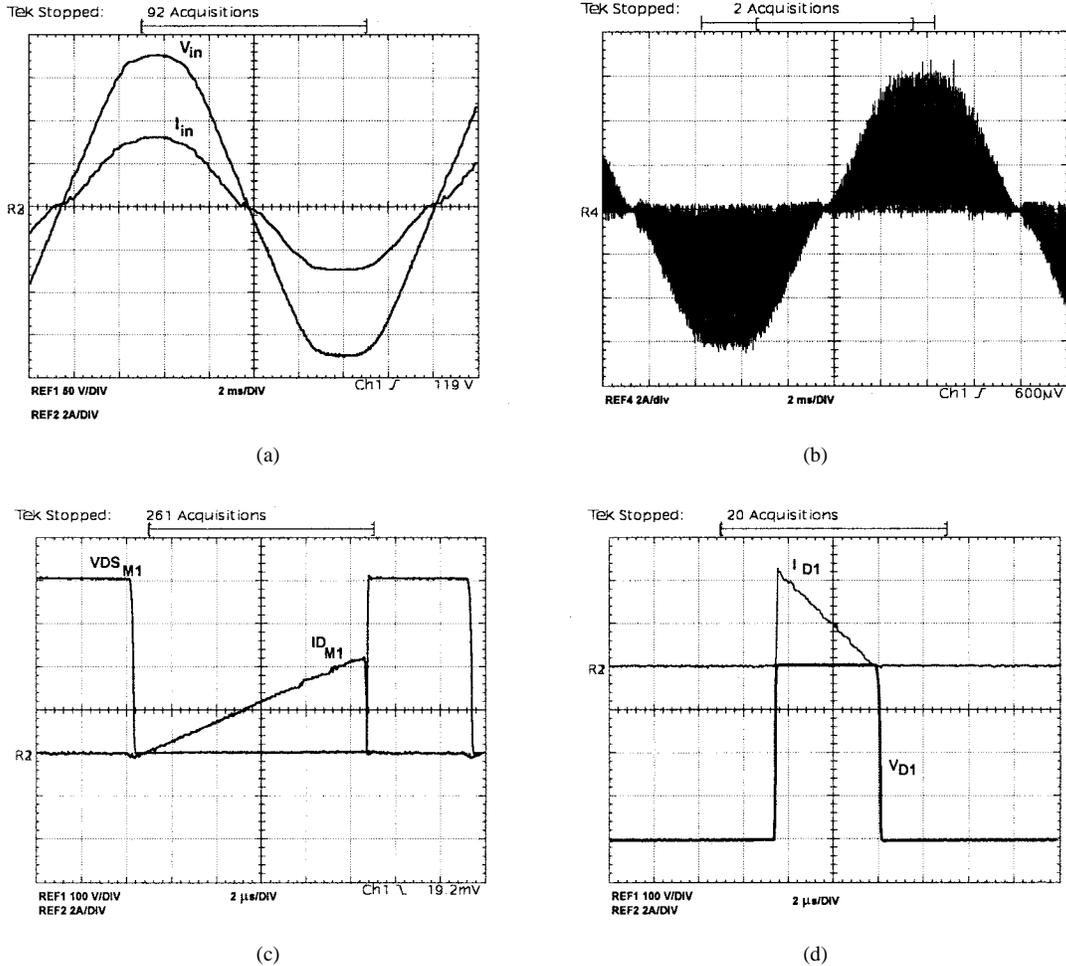


Fig. 10. Experimental results. (a) Input voltage (50 V/div) and input current (2 A/div). (b) Input inductor current (2 A/div). (c) Drain-to-source voltage (100 V/div) and drain current (2 A/div) of MOSFET M_1 . (d) Voltage (100 V/div) and current (2 A/div) of diode D_1 .

substituting the values of f_r and β in (51), the expected power factor will be 0.998.

VI. EXPERIMENTAL RESULTS

In order to experimentally verify the principle of operation and the theoretical analysis, a 300-W semiresonant ZVS high power factor converter has been implemented in the laboratory using Unitrode’s critical conduction mode IC, UC3852 [8]. The prototype was tested with an input voltage of 127 V_{rms} and an output voltage of 400 V_{DC}.

The complete diagram of the prototype is shown in Fig. 9. The dual-thyristor principle [9] is employed to ensure the ZVS of the MOSFET’s. The power components specification is as follows:

- M_1, M_2 —APT5025;
- D_1, D_2 —MUR 460;
- $L_{in} = 270 \mu\text{H}$ —46 turns (6×25 AWG) on EE-42/15 core (gap = 1.9 mm);
- $L_f = 1.5 \text{ mH}$ —99 turns (19 AWG) on EE-42/15 core (gap = 1.5 mm);
- $C_f = 1 \mu\text{F}/250 \text{ V}$ (polypropylene);
- $C_o = 680 \mu\text{F}/500 \text{ V}$.

Fig. 10(a) shows the input voltage and the filtered input current. The power factor obtained was 0.997 with a total harmonic distortion (THD) of 8.2% in the input current.

The input inductor current is shown in Fig. 10(b). It can be noticed that the input inductor peak current naturally follows the sinusoidal input voltage.

The commutation detail of the MOSFET M_1 is shown in Fig. 10(c). As can be noticed, the ZVS commutation is achieved.

The voltage and current of diode D_1 are shown in Fig. 10(d). It can be noticed that the current through the diode naturally extinguishes, therefore, the effect of the diode reverse recovery will be negligible.

The experimentally obtained current harmonic components are presented in Table I. It can be noticed that all the harmonics are in accordance with IEC harmonic regulations.

The obtained efficiency for full load was 96.7%, while the efficiency for the hard-switched converter at the same power level was 95.2%. The improvement of 1.5% in the efficiency represented a reduction from 15 to 10 W in the total losses. Therefore, the losses in the hard-switched converter are 50% higher than the losses for the semiresonant converter, leading to a reduction in the heat sink volume.

TABLE I
EXPERIMENTALLY OBTAINED HARMONIC COMPONENTS

Harmonic Order	Experimental Results (A rms)
3rd	0.1050
5th	0.1350
7th	0.0161
9th	0.0238
11th	0.0153
13th	0.0035
15th	0.0061
17th	0.0062

VII. CONCLUSION

In this paper, a technique to improve the efficiency of high power factor rectifiers by reducing the commutation losses and the conduction losses has been presented. The high efficiency is obtained by three important factors:

- soft-switching (ZVS);
- there are only two semiconductor voltage drops in the current flow path at any time;
- conduction losses in the MOSFET's are reduced if the gate-to-source voltage is high when the current is flowing from source to drain.

The topology also presents the following characteristics:

- absence of auxiliary switches to perform the soft-commutation;
- capability to draw a sinusoidal input current with constant on time of MOSFET M_1 and M_2 , using critical conduction mode with variable switching frequency;
- simplified gate circuit for the MOSFET's, once they have the same command.

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