A 3-kW Unity-Power-Factor Rectifier Based on a Two-Cell Boost Converter Using a New Parallel-Connection Technique

Henrique A. C. Braga, *Member, IEEE,* and Ivo Barbi, *Senior Member, IEEE*

***Abstract*— This paper applies a recently introduced parallel-connection technique to a unity power-factor preregulator based on a boost converter in continuous inductor-current mode. By means of a small extra inductance, two MOSFET pulsewidth modulation (PWM) cells are safely associated in parallel, which allows an increased output power being processed by two half-rated semiconductor devices. The new technique overcomes the existent alternatives, leading to a reliable switched converter along with simplified layout requirements. This paper also presents a theoretical analysis accompanied by digital simulation cases.**

Results from a 3-kW prototype, based on the Unitrode's UC3854 strategy, show that the present technique is very useful in revealing a natural balance among device currents. The laboratory circuit works at a 70-kHz switching frequency and also employs a soft-commutation network. This feature points to a high-efficiency converter and negligible device stresses, which have been verified in the laboratory.

***Index Terms*—Boost converter, power factor correction, rectifier, soft commutation.**

I. Introduction

POWER-FACTOR correction (PFC) strategies for switching power supplies have been the object of many scientific works during the past few years [1]–[4]. The most widely used procedure consists of employing a boost-based converter being controlled by the Unitrode's UC3854 [5] integrated circuit in an average current-control strategy. Telecommunications are included among the fields that take benefits from those studies. At medium power, the more common levels in this area are 1.5, 3, 6, and 12 kW. The first two levels are commonly implemented by using a single-phase utility while the last two ones require a three-phase system. For a single-phase off-line switching regulator, much effort has been made to reach the 3-kW mark with reliability, efficiency, and compactness [6], [7].

Perhaps the most straightforward alternatives to process a single-phase application at the 3-kW level lie on the use of a double-cell converter or even a single-cell one. A double-cell converter normally employs two devices connected in parallel by the conventional way. This alternative has the advantage of employing half-rated devices, generally cheaper than the normal-rated counterparts. However, it fails to provide a good dynamic equilibrium among device currents. So, the layout design must be carried out carefully in order to minimize the divergencies between device branches. In addition, it could be considered that switching parameters of devices are not the same, causing one of them to be continuously stressed (by supporting during sometime all the input current), which could reduce the converter reliability. Naturally, this problem becomes worse, as the number of paralleled devices increases.

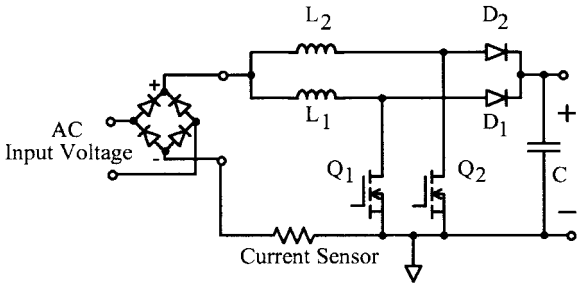

Fig. 1. Interleaved boost power-factor corrector.

The work reported in [6] employs a large-area MOSFET die and a fast-recovery epitaxial diode (FRED) to replace the parallel MOSFET devices normally used in high-current PFC circuits. The optimization process for a single pulsewidth modulation (PWM) cell converter depends on matching the MOSFET switching behavior to the dynamic characteristics of the companion fast-recovery diode. Also, in this case the physical layout of the power stage requires a careful design to minimize overvoltage transients and excessive electromagnetic interference (EMI).

A reasonable improvement relating to double-cell converters can be obtained using the interleaving technique, as explained in [8] and depicted in Fig. 1. In fact, this alternative can be understood as two boost converters in parallel. The individual cells have the same conversion frequency, but their internal switching instants are sequentially phased over equal fractions of a switching period. This mechanism provides a high overall frequency, useful to reduce filtering requirements, without increasing switching losses.

The interleaving strategy is a kind of cellular architecture for which a number of autonomous converters share the total power allowing the employment of single-die inexpensive devices [9], [10]. A converter employing this procedure can

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H. A. C. Braga is with the Universidade Federal de Juiz de Fora, 36.001-000, Juiz de Fora, MG, Brazil (e-mail: hbraga@engelet.ufjf.br).

I. Barbi is with the Universidade Federal de Santa Catarina, 88.040.970, Florianópolis, SC, Brazil (e-mail: ivo@inep.ufsc.br).

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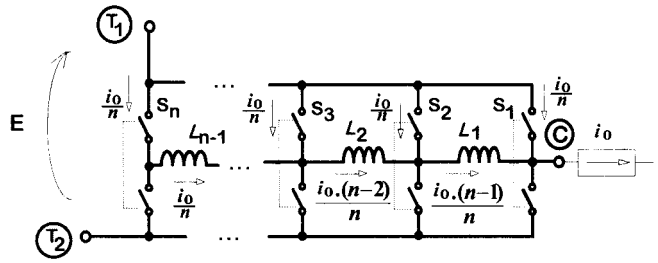

Fig. 2. Generalized cell for the new paralleling technique.

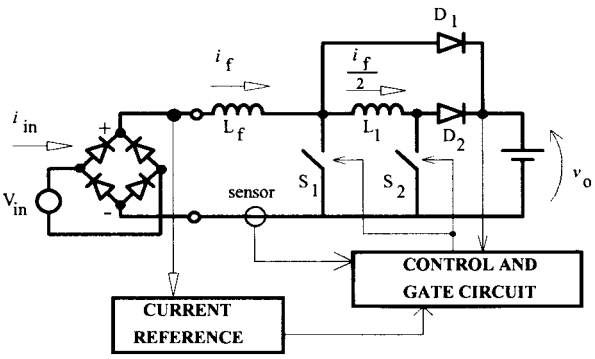

Fig. 3. Two-cell PFC boost converter.

feature a great power density without the penalty of reduced power-conversion efficiency. However, interleaving requires a complex circuitry, leading to a more expensive implementation and reduced reliability. Moreover, the unequal current sharing in continuous-inductor current and at average current control is a practical problem in this case. To guarantee a good current distribution, it would be necessary an additional current sensor for each MOSFET (in series with the source terminal) and some extra circuitry [7]. This requirement becomes more critical as the number of parallel cells increases.

This paper proposes the application of a recently introduced parallel-connection technique to a boost PFC converter, which offers a good alternative to the strategies mentioned above. The technique consists of a parallel association of PWM cells using small inductances to connect them, as shown in the general circuit of Fig. 2. Unlike the interleaving technique, all switches are gated by the same gate signal. The relationship among shown variables assumes a typical operation [11]. In a conventional nonisolated dc–dc converter, for example, current i_o is a dc current and bottom switches are diodes. The main advantages of the new technique include a natural static and dynamic current balance among devices, together with a simplified requirement for the power stage layout. This stems from a particular feature of the new technique for which, under certain limits, stray inductances and divergencies on device switching times do not interfere in the current distribution process [11]. Moreover, unlike the single-cell alternative, in the double-cell version the reverse recovery problem of the diode is shared between two devices. As will be shown, the proposed procedure also allows, at least, more than one point to insert the current sensor.

The operation principle of the circuit of Fig. 2 can be summarized as follows. Assuming continuous conduction current for all inductors, the current source at node $\mathbf{C}$ is determined mainly by "external" parameters. That is to say, it does not depend on the number of branches, value of inductors, and switch technology. In other words, current i_o is, basically, a function of external voltage sources and switching frequency. Since the conduction behavior of any two neighbor switches are much similar, balance inductors are continuously short circuited. In this simple parallel association, inductors charge according the well-known Norton's rule of circuit theory, obeying the levels indicated in Fig. 2 [11]. These statements will be verified by a more strict approach, detailed in Section II.

Fig. 3 shows the whole PFC system employing the technique of Fig. 2, including a block diagram of the control circuit. The current control strategy is fulfilled by the UC3854 integrated circuit, using the "average current control" method. Although there is not a specific value for L_f/L_1, the balance inductor should assume a small value in order to not interfere in the volume/weight of the equipment and to not introduce a poor dynamic response of the converter. Practical considerations regarding these two elements will be considered in Section III.

From Fig. 3, one can notice that both switches are gated by the same gate signal, which determines great simplicity and reliability to the proposed converter. Another benefit of the new technique consists of the fact that a switch does not support all the input current if, for any reason, it remains conducting alone for a short time (in the case of switching parameter divergences) [11]. It can be noticed that the interleaving technique, for example, also shares this property. However, those divergences consist of a potential problem for the conventional parallel-connection technique [12].

The current reference block of Fig. 3 builds a reference signal with the same shape of the rectifier output voltage, which is a "positive" sinusoidal quantity. The employed control strategy imposes a continuous conduction current (CCM) through the boost inductor L_f following the positive sinusoidal shape in order to attain a high-power-factor operation.

II. Theoretical Analysis of the Two-Cell Boost Converter

A. Line-to-Output Model

Fig. 4 shows a simplified equivalent circuit for the two-cell boost converter of Fig. 3 (so, assuming the rectifier bridge is a voltage source). This circuit is the line-to-output PWM switch model [13]. In that figure, all the switches have been represented by a "time-average" resistance r, which is based on the ON resistance of the active and passive switches. For the purpose of this analysis, some parameters have been neglected, such as the parasitic resistance of the reactive elements.

As stated before, no closed-loop strategy is employed to control the current sharing among switches. So, these currents must reach the dynamic and static current equilibrium by a natural operation way. The model in Fig. 4 can be used to check that statement. From Fig. 4, it is possible to find the

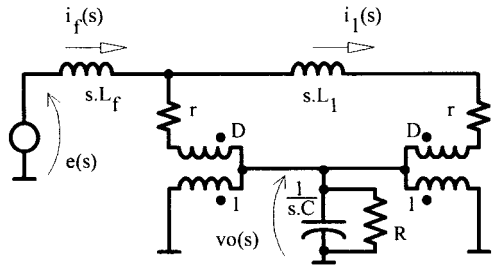

Fig. 4. Line-to-output model.

transfer functions of the main variables, such as v_o, i_f, and i_1

$$\frac{v_o(s)}{e(s)} = \frac{(1-D)(2r+L_1S)R}{H(s)} \tag{1}$$

$$\frac{i_f(s)}{e(s)} = \frac{(1+RCs)(2r+L_1s)R}{H(s)} \tag{2}$$

$$\frac{i_1(s)}{e(s)} = \frac{(1+RCs)r}{H(s)} \tag{3}$$

where $H(s)$ can be reduced to

$$H(s) = L_fL_1CRs^3 + L_f(L_1+2rRC)s^2 + [r^2RC + L_1R(1-D)^2 + 2L_fr]s + 2Rr(1-D)^2 \tag{4}$$

if one consider a practical situation in which $r \ll R$ and $L_1 \ll L_f$.

Figs. 5 and 6 show the performance of the basic two-cell boost converter using a step voltage of 200 V, a switch frequency of 70 kHz, $r = 0.2\ \Omega$, $D = 0.5$, $L_f = 700\ \mu$H, $L_1 = 10\ \mu$H, $C = 10\ \mu$F, and $R = 25\ \Omega$. Based on this set of parameters, a conventional (one-cell) boost converter would present an output voltage of 400 V and an input current of 32 A. The gate pulses to switch S_2 have been delayed 40 ns, a technique used to check the current clamping capability of the structure. The model equations (1)–(3) have been plotted in Fig. 5, revealing a very good description of the simulation case in such a way that their curves are almost the same of the simulated counterparts. It can be also observed that the steady-state quantities obey the conventional boost relationship, verifying the simplifier analysis of Section I.

Figs. 6 and 7 show that the two-cell boost converter has a good static and dynamic characteristic from the point of view of input voltage disturbances. In addition, Fig. 6 showed that the balance inductor current follows dynamically the half of the input inductor current. This is the reason for the good equilibrium among device currents. It can also be noticed that even in the presence of out-of-phase gate signals, negligible current spikes were observed. This behavior confirms the current clamping feature of the structure.

B. Control-to-Output Model

Another important point to be checked is related to the control-to-output behavior of the final PFC converter. To study this subject, the two-cell boost converter of Fig. 3 is going to

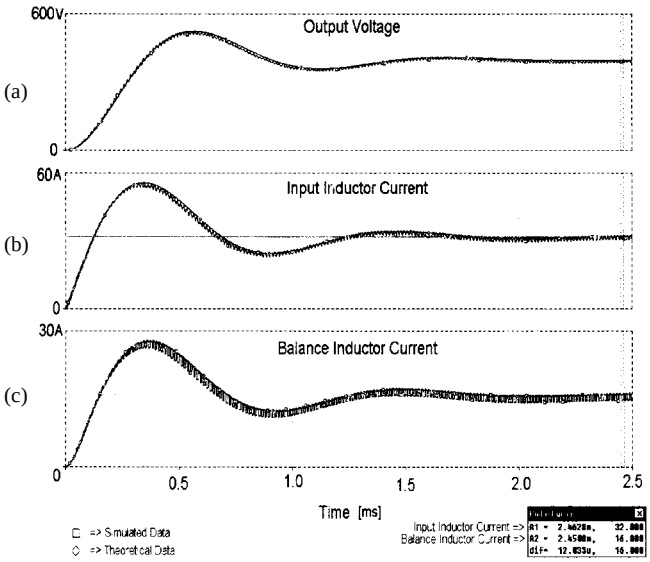

Fig. 5. Voltage-step response (digital simulation and model curves). (a) Output voltage, (b) input inductor current, and (c) balance inductor current.

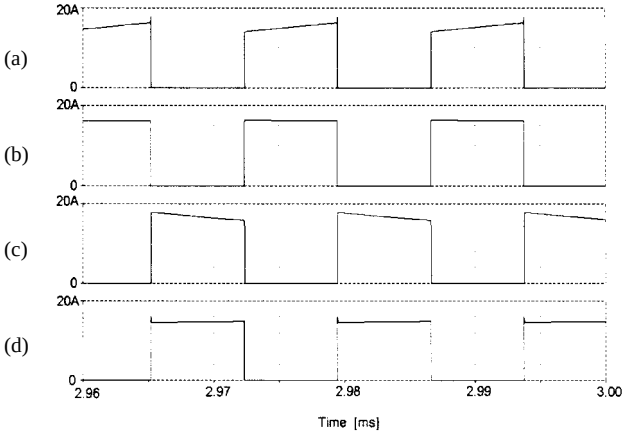

Fig. 6. Comparison of device currents at steady state. (a) S_1 current, (b) S_2 current, (c) D_1 current, and (d) D_2 current.

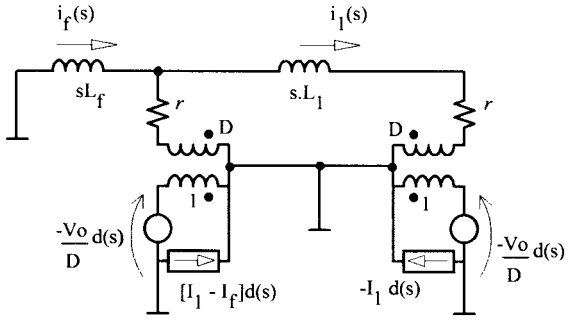

Fig. 7. Control-to-output model of the PFC boost converter.

be modeled by a procedure similar to that in previous section, as shown in Fig. 7. In that circuit, the output branch has been simplified to a constant output voltage source V_o being in rest in the equivalent model. The quantities I_f and I_1 represent the input and balance inductor currents at the operation point for a fixed duty cycle D, which is used to reference the dynamic analysis.

Equations (5) and (6) show the transfer functions of inductor currents, obtained by solving the circuit of Fig. 7

$$\frac{i_f(s)}{d(s)} = \frac{V_o(2r + sL_1)}{L_f L_1 s^2 + (L_f 2r + rL_1)s + r^2} \tag{5}$$

$$\frac{i_1(s)}{d(s)} = \frac{V_o r}{L_f L_1 s^2 + (L_f 2r + rL_1)s + r^2}. \tag{6}$$

It is not difficult to show that if $L_1 \ll L_f$ (a practical situation), (5) reduces to

$$\frac{i_f(s)}{d(s)} = \frac{V_o}{sL_f}. \tag{7}$$

Moreover, if $s \ll 2r/L_1$ (6) reduces to

$$\frac{i_1(s)}{d(s)} = \frac{V_o}{2sL_f}. \tag{8}$$

Thus, from the control viewpoint, the current through balance inductor L_1 is the half of the input current. The condition that gave rise to (8) determines, for the simulation case of the last section, changes in d at a frequency much smaller than 6.3 kHz. In practice, d changes at a frequency inferior to 120 Hz, which ensures that "$s \ll 2r/L_1$" is a very practical situation. This means that the new structure offers two points for insertion of the current sensor element. Moreover, (7) and (8) prove that the new structure obeys the same basic rules found in a conventional boost converter. In other words, it is possible to employ the same known strategies to control the input current aiming, for instance, to comply with high-power-factor behavior.

Fig. 8 shows the amplitude and phase angle of the input and balance inductor currents, according to (5) and (6), using the same parameters of those used in the last item.

As can be seen from Fig. 8, both functions have a low-frequency pole and another one near 7 kHz. However, the input inductor current has a zero at the same frequency of the second pole, determining a constant decay of 20 db/decade (and a phase angle not inferior to -90°). This feature is not present in the transfer function of the balance inductor current, which is reflected in the 40-dB/decade slope above 7 kHz. The frequency response of the balance inductor current reveals it to be very close to that relative to the input inductor current (despite the double rate between their gains) for changes in d below 1 kHz approximately. This mark seems to be enough to prove the similarity involving the two variables, as was discussed in the previous paragraph. Of course, the design of the current control system must take into account the switching frequency f_{SW}. Special care is required for high values of this parameter, since the open-loop gain could assume at the cutoff frequency an insufficient phase-margin value, causing the system to get into an unstable condition.

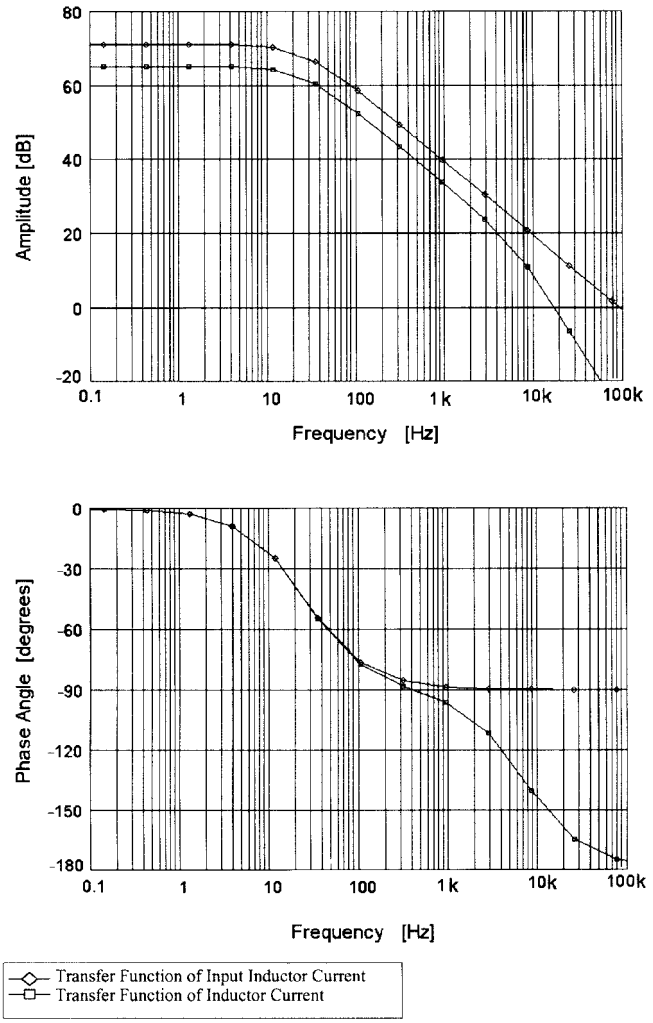

Fig. 8. Bode plots of (5) and (6).

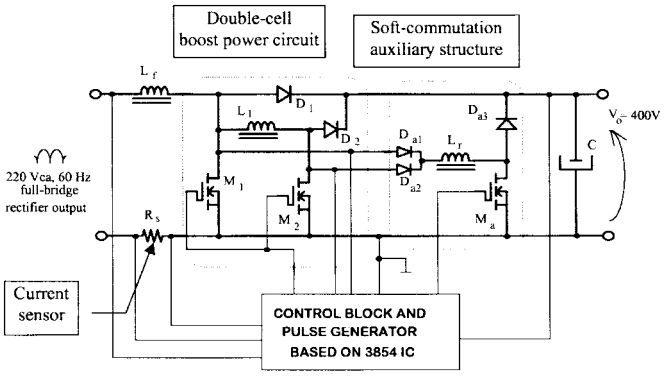

Fig. 9. Preregulator circuit tests in laboratory (simplified diagram).

III. Design Considerations and Digital Simulation

As stated in the previous section, the new structure does not alter the main features of a conventional boost converter. So, the design procedures follow similar rules. This section gathers some important aspects concerning the design of a unity power-factor rectifier delivering an output power of 3.2 kW, employing the new structure and including a soft-commutation strategy. The basic structure is shown in Fig. 9 and will be designed to operate at a 70-kHz switching frequency.

The zero-voltage transition (ZVT) circuit has the purpose of reducing heatsink requirements since the switching losses of main switches are negligible. Although the extra components cannot be of smaller die sizes, the ZVT network responds

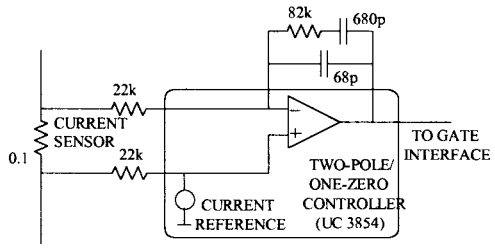

Fig. 10. Current controller details.

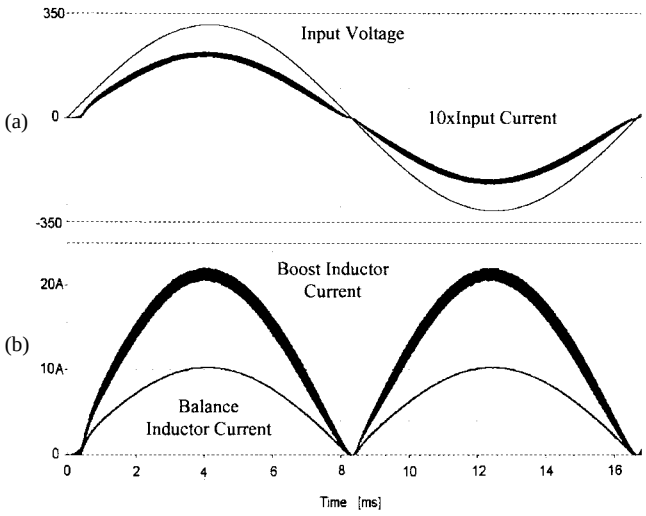

Fig. 11. Waveforms from computer simulation. (a) Utility voltage and current (nonfiltered). (b) Boost and balance inductor currents.

for only a fraction of the total power losses. It can be proved that at 70 kHz, the soft-commutation network allows a reduction of power losses around 11 W (15% of total losses with soft commutation), and, as a consequence, a reduction in the volume-weight of the final equipment. If a 200-kHz switching frequency had been adopted, the correspondent economy would be more than 90 W (or more than 100% of total losses).

From Fig. 9 one can notice that, except for the use of an extra diode, the auxiliary soft-commutation circuit (ZVT) employs the same arrangement (same number of elements) used in a conventional boost converter [14]. This simplification is possible because in the current strategy both switches are gated by the same gate signal. using the interleaving technique, for example, at high frequencies (more than 100 kHz) each parallel branch would require an extra auxiliary soft-commutation circuit due to the out-of-phase gate strategy employed. On the other hand, the interleaving technique allows doubling the effective switching frequency, as compared to the current technique, resulting in higher power density in the case of hard commutation. Moreover, input and output filter design for the interleaving technique leads to smaller elements considering the same input voltage, same output power, same output voltage, same output-voltage ripple, and same line-current ripple.

In the following, some simplified considerations concerning the choice of L_f, L_1, and the main switches will be discussed. The controller design, which is associated with the UC3854 integrated circuit, will also be discussed in briefly. The design of the ZVT structure is not considered here because it is discussed in the original papers [14]. The main design steps are as follows.

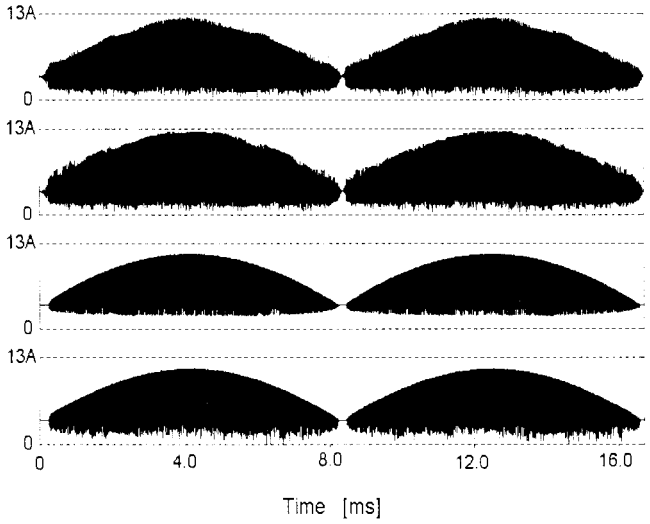

Fig. 12. Comparison of device currents (from top to bottom: S_1, S_2, D_1, and D_2 currents).

1) First of all, it is important to calculate some parameters which will be used to design further elements of the circuit. Assuming an ideal efficiency converter, the maximum (peak) input current will be 20.6 A (neglecting the ripple). So, for an ideal current distribution, each device will conduct a peak current of 10.3 A (again, neglecting ripple) during the ON state.
2) Input inductor L_f has the main purpose of reducing the ripple over input current. If this ripple is high, it is expected some imbalance involving the peak values of device currents. The cell formed by M_1–D_1 has the greatest values of peak current since it is closer to the input current source [11]. The design of the input inductor depends on the switching frequency, input voltage, and allowed ripple [4], [5]. Considering an output power of 3 kW, a switching frequency of 70 kHz, an input voltage of 220 V, and a current ripple between 10% and 15% of input current, it is possible to find out a value between 370–700 μH for the input inductance.
3) The balance inductor L_1 is used to connect the PWM cells in parallel and to protect them from current stresses due to switching differences between active devices or branches with different stray inductances [11]. Practical studies have shown that protecting devices against differences on device switching parameters is a procedure that also minimizes the bad effects of stray inductance imbalances. If one MOSFET begins or remains conducting alone for some period of time, the output voltage will be across L_1 during that time. This is reflected as current spikes through device currents. Assuming 30 ns as the maximum time, a device conducts alone and allowing 10% of maximum current spike (related to the maximum device current), the value of L_1 will be 11.6 μH. A

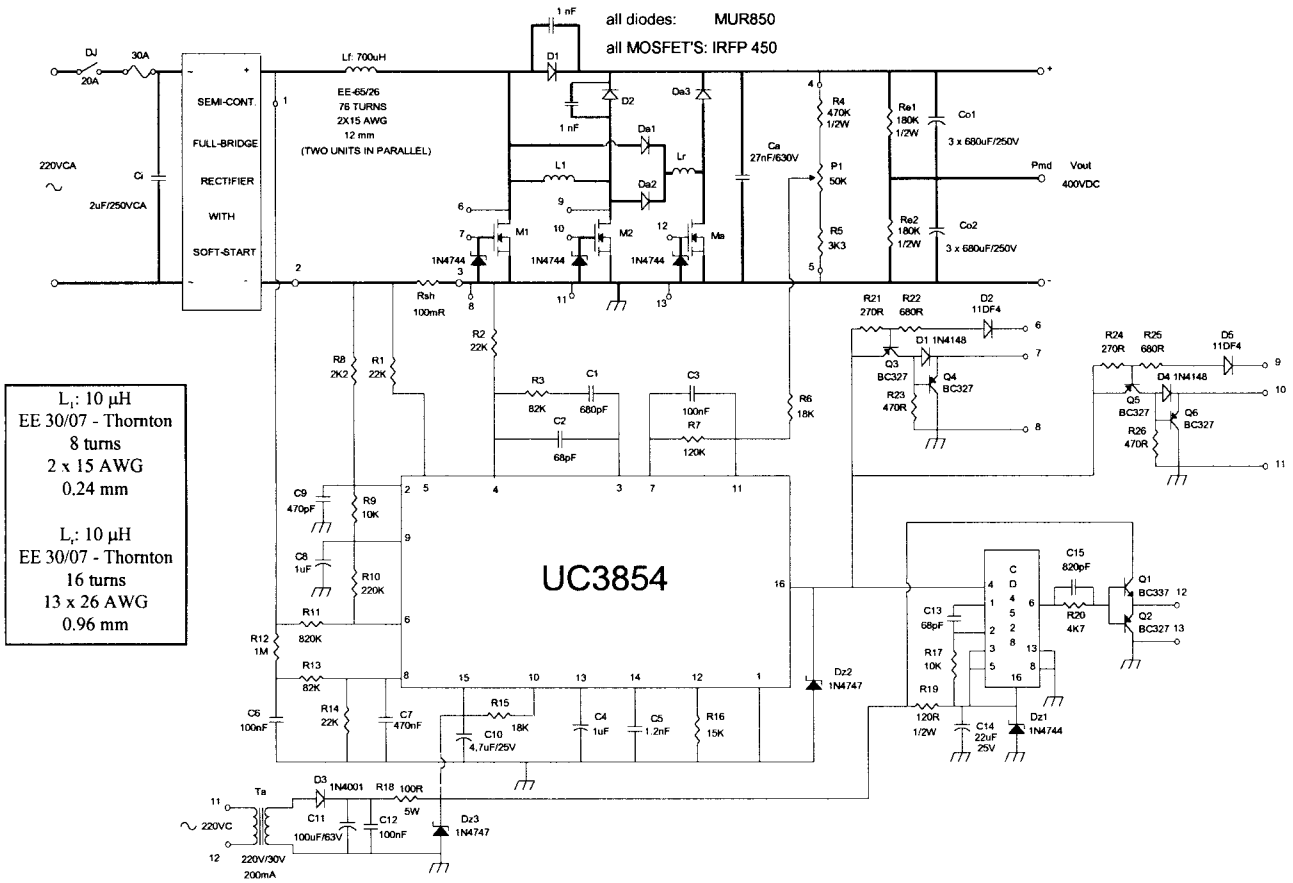

Fig. 13. Complete circuitry of laboratory prototype.

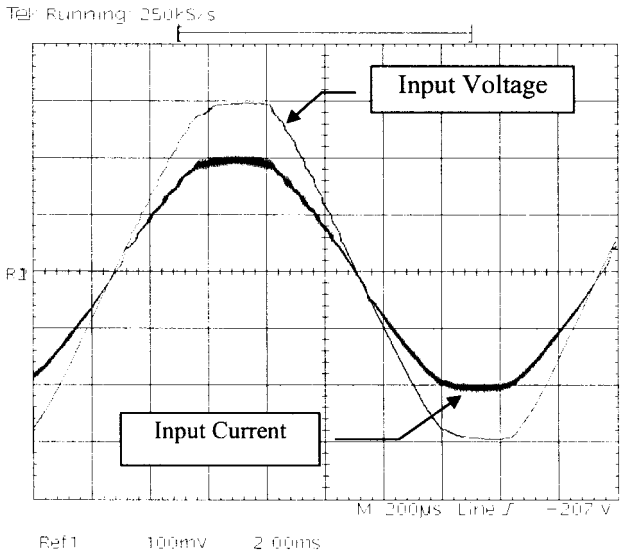

Fig. 14. Input voltage and current at full load (100 V/div; 10 A/div).

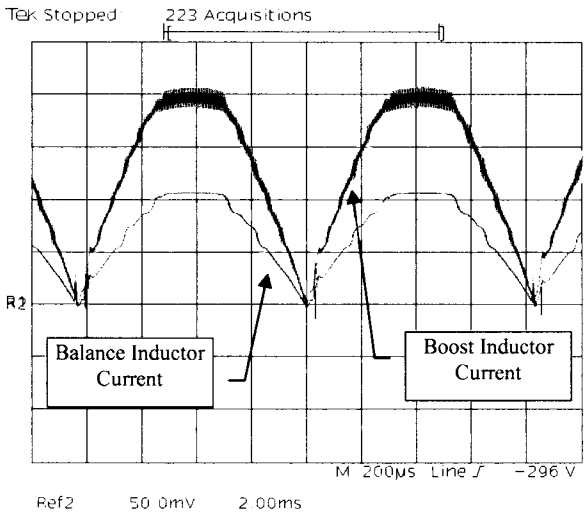

Fig. 15. Input and balance inductor currents (5 A/div).

practical value of 10 μH can be used with almost the same performance. This calculation assumed a constant voltage across L_1, which is not a strict consideration. However, it stands for a reasonable approximation.

4) Active and passive switches can be chosen considering, first, that the ZVT module eliminates voltage stresses of devices. In addition, the parallel-connection structure guarantees a huge reduction of current stresses. Thus, the choice of the switches can be done assuming an ideal circuit operation. For the desired parameters, the semiconductor elements must support a repetitive voltage of 400 V and carry a peak current of 12 A (considering the current ripple). Moreover, active and passive switches

must be chosen to sustain the following current values (deduced similarly as in [15]):

$$i_{S\text{rms}} = \frac{1}{2}\sqrt{I_{\text{rms}}^2 - \frac{3}{8}\left(\frac{V_p I_p}{V_o}\right)^2} \quad (9)$$

$$i_{D\text{avg}} = \frac{1}{2}\left(\frac{1}{\pi}\int_0^{\pi}\frac{I_p V_p}{V_O}\sin^2(\omega t)\mathrm{d}(\omega t)\right) = \frac{I_p V_p}{4V_O} \quad (10)$$

where I_{rms}, I_p, V_p, and V_o are the values of the rms of input current, peak input current, peak input voltage, and output voltage, respectively. Assuming the conditions of 1), (9) and (10) yield 5.4 and 4.0 A, respectively. Of course, the right choice of components should take into account the nature of the switches [insulated gate bipolar transistor (IGBT), MOSFET, etc.], input voltage tolerance, current ripple, and available heatsinks. Sometimes the reduction of size and volume is the primary goal. For this case, the designer could adopt a stronger switch (more expensive, but with a lower ON resistance) to reduce the heatsink requirement. Thus, the multicell arrangement could lead to up to 50% less conduction losses, as compared to a single-cell alternative employing the same devices.

5) Device power dissipation is determined mainly by conduction losses since negligible switching losses are expected due to the ZVT circuit. All the power semiconductor elements can be placed on the same heatsink, including the soft-commutation devices, which respond to a low-power dissipation.
6) The voltage control loop associated with the UC3854 integrated circuit can be designed as suggested in [5]. The current control loop, which is also associated with the UC3854, is represented in Fig. 10. The elements external to the integrated circuit have been designed according to the Bode plots of Fig. 8 in order to provide a stable condition. The current sensor has been allocated in the input inductor loop.

The circuit of Fig. 3 has been simulated using $V_{in} = 220$ Vrms, $f_{in} = 60$ Hz, and $L_f = 700$ μH and $L_1 = 10$ μH, $V_o = 400$ V (filtered by a 680-μF capacitor), $P_o = 3.2$ kW, and $f_{SW} = 70$ kHz. The voltage control loop was not considered so as to speed up the simulation time. It has also been employed as a soft-commutation technique, as indicated in Fig. 9. Pspice actual semiconductor models have been used to simulate the switches: IRFP450 as active devices and MUR850 ad diodes.

Figs. 11 and 12 show the simulation results using the above-mentioned set of parameters. Fig. 11 shows that a high-power-factor situation has been attained. Fig. 12 reveals that an excellent current distribution among switches has been reached.

IV. Experimental Results

Fig. 13 shows the complete circuit diagram useful to anyone who wants to reproduce the results that follow. The basic power circuit is constituted of a couple of PWM cells (two sets of a PWM switch formed by a diode and a MOSFET) connected by means of a 10-μH inductor. This stage is fed by a full-bridge rectifier, boosted by a 700-μH inductor.

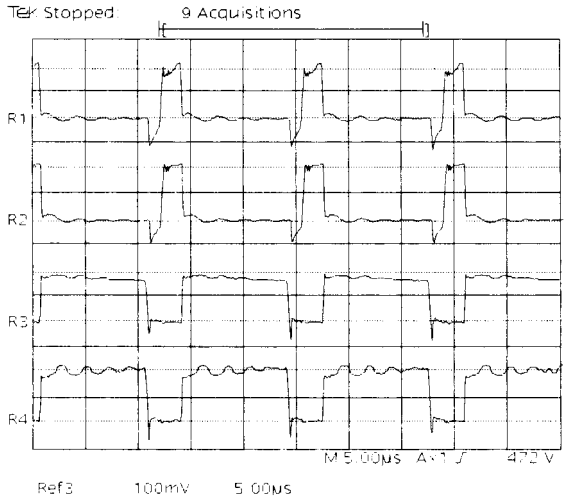

Fig. 16. Device current comparison at peak condition (from top to bottom: M_1, M_2, D_1, and D_2; 5 A/div).

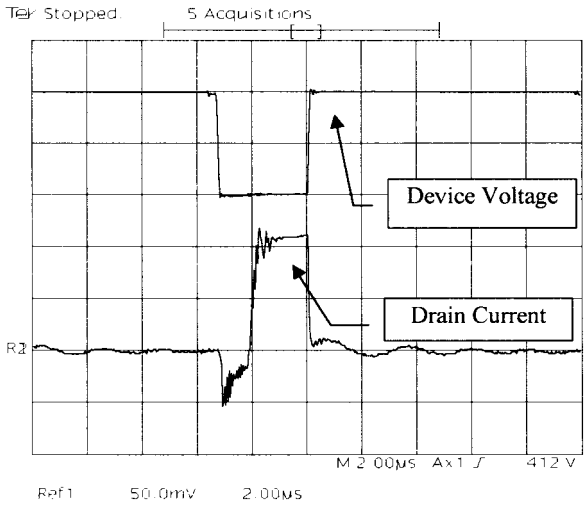

Fig. 17. Soft-commutation detail (100 V/div, 5 A/div, 2 μs/div).

On the other hand, ZVT [14] arrangement is set to provide the soft-commutation feature. This auxiliary circuit employs three diodes, another MOSFET, and a 10-μH inductor. As explained in the last section, those components are expected to work with only a small fraction of the total processed energy.

All the active devices are gated and controlled by a control unity based on the Unitrode's UC3854 [15]. This stage is designed to gate the MOSFET's at a 70-kHz frequency. The measured output power reached a value of 3.04 kW, leading to an efficiency of 97.5%.

Fig. 14 shows the laboratory waveforms of the input voltage and current at full load. A small distortion is inherent to the input voltage, but a high power factor can be observed.

Fig. 15 shows the waveforms of the boost and balance inductor currents. As predicted, the balance inductor current

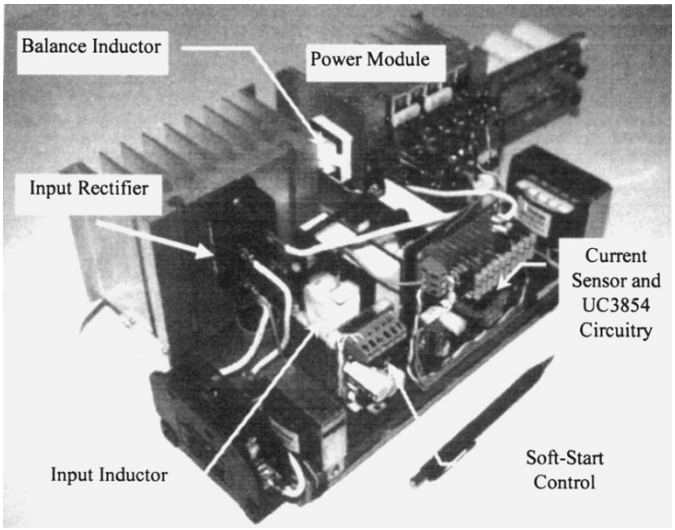

Fig. 18. Prototype photograph.

is the half of the value measured for the boost inductor current. This is a fundamental condition for a good current balance among the main semiconductor devices. This situation is definitely proved in Fig. 16. At the peak condition, one can observe a very good current distribution. Fig. 16 also shows that the diode reverse recovery problem [6] is minimized since it has been shared between two diodes. So, it is expected a reduced overvoltage across diodes and, as a consequence, lower EMI levels.

Fig. 17 shows a detail of the soft-commutation process. It can be noticed that the MOSFET drain current flows by its antiparallel diode only after the drain voltage falls to zero. So, the positive current conduction is assured to start at zero-voltage condition. At turn off, the MOSFET drain-to-source capacitance needs to be charged, which explains the energy exchange observed during this transition.

Fig. 18 shows a prototype picture. From this figure, it is possible to observe the negligible volume required by the balance inductor element, as compared to the input inductor volume. It must be pointed out that the setup size could be significantly reduced because it has employed a heatsink greater than necessary (since, momentarily, the optimum shapes were not available in the laboratory). Moreover, it has not been considered as a design orientation (at least in this stage of the work) to find out the minimum size of the final product. However, the PFC preregulator equipment (including the ac–dc rectifier unit and heatsink) presented a power density of about 12 W/in^3. This can be considered a good mark comparing to a interleaving setup reported, using near the same ratings, but employing a switching frequency of 100 kHz (or a 200-kHz effective frequency) [7] without soft commutation.

V. Conclusions

This work has shown an application of a recently introduced parallel-connection technique to a rectifier system operating with unity power factor. The system is based on a two-cell boost converter and offers an excellent static and dynamic current sharing among devices. Due to its cellular concept, the system can be adapted to process a high-output power. In this case, any number of PWM cells can be paralleled.

The new structure has, under certain limits, a natural tolerance to branch imbalances caused by stray inductances. For this motive, it requires a very simplified layout design. The resulting commutation cell is compatible with the existing dedicated integrated circuits for driving and control of a PFC converter. Moreover, it can be easily adapted to existing soft-commutation techniques, requiring minimal circuitry whatever the number of parallel branches.

Those features ensure that the new structure is suitable to be employed in industrial and commercial applications working above the 1-kW level of power.

The above features have been verified by a laboratory prototype from which 3.04 kW have been drawn. The system has been designed to work at a 70-kHz switching frequency, supplying an output voltage of 400 V. The practical circuit employed a soft-commutation technique and presented an overall efficiency of 97.5% at full rate and a power density of 12 W/in^3.

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Henrique A. C. Braga (M'83) was born in Aimorés, MG, Brazil, in 1959. He received the B.S. degree in electrical engineering from the Universidade Federal de Juiz de Fora, Brazil, in 1982, the M.S. degree in electrical engineering from COPPE–Universidade Federal do Rio de Janeiro, Brazil, in 1988, and the Ph.D. degree from the Universidade Federal de Santa Catarina, Florianópolis, Brazil, in 1997.

Since 1985, he has been a Lecturer on Basic and Power Electronics at the Universidade Federal de Juiz de Fora, where he is currently Head of the electrical engineering course. In addition, he helped establish the M.S. program of electrical engineering at the same University. In 1991, he encouraged his students to found the IEEE Student Branch at the Universidade Federal de Juiz de Fora, where he was the Branch Counselor.

Ivo Barbi (M'78–SM'90), for a photograph and biography, see this issue, p. 97.