A New High-Power-Factor Three-Phase AC–DC Converter: Analysis, Design, and Experimentation

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Abstract—This paper proposes a new high-power-factor three-phase ac–dc converter, which is composed of a line interphase transformer (LIT) and two three-phase diode rectifiers, followed by a pulsewidth modulation (PWM) dc–dc boost converter.

The active switch of the boost converter is gated at a constant frequency such that the ac input current is discontinuous. This procedure provides an input current shaping without the third, fifth, and seventh harmonics. The currents that flow through the LIT and boost inductors have such a high-switching frequency that ferrite cores with a small size can be utilized.

In addition, the output voltage is regulated by PWM to compensate for line voltage variations and load change.

Theoretical analysis, design procedure and example, along with experimental results taken from a 6-kW laboratory prototype are given.

Index Terms— AC–DC converter, harmonics, line interphase transformer, power factor correction.

I. INTRODUCTION

ONE OF THE most important research topics in power electronics at the present time is the power factor (PF) correction of three-phase diode rectifiers with capacitive output filters. This kind of rectifier is mostly utilized in industrial and commercial applications for economic reasons. The technique proposed in [1] and shown in Fig. 1 (six-pulse rectifier) is very simple because it uses only one active switch, with no active control of the current. It is one of the most popular techniques discussed in the literature due to its simplicity. Thanks to the discontinuous inductor current mode, a sinusoidal input current shaping is achieved in this circuit.

Two main drawbacks of the converter mentioned above have been identified, namely, excessive output voltage and the presence of fifth harmonics in the line current.

A less known but not less important power-factor-correction technique, suitable for high-power application, was proposed in [2] and is represented in Fig. 2 (12-pulse rectifier). This technique is simple, offers high reliability, and, most important, has been used successfully in many industrial applications.

Three problems exist with this converter: the output voltage is not controlled, it is too low for most applications, and the

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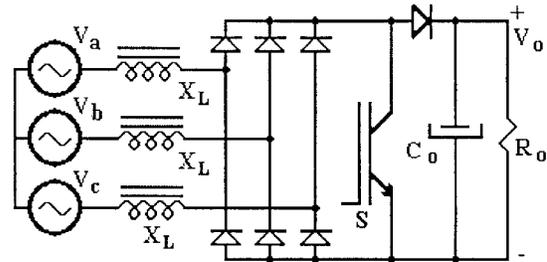
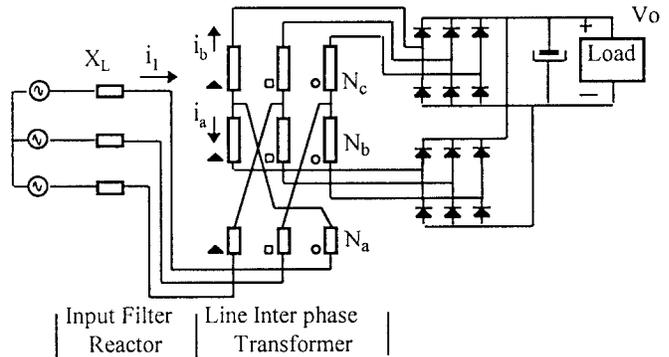Fig. 1. High-power-factor three-phase diode rectifier proposed in [1].

Fig. 2. High-power-factor three-phase diode rectifier using the LIT proposed in [2].

line interphase transformers are relatively large because they operate at the line frequency.

In this paper, we propose a technique that benefits from the best features of the two mentioned circuits. Details of the theoretical analysis, together with experimental results, are provided in the following sections.

II. THE PROPOSED CIRCUIT

The proposed circuit [3] is shown in Fig. 3. It is formed by three boost inductors (L), three line interphase transformers (LIT's) [2], two three-phase diode rectifiers (R_a and R_b), and a pulsewidth modulation (PWM) dc–dc boost converter. A three-phase high-frequency input filter is placed between the power main supply and boost inductors.

The LIT, with the turns ratio given by (1a) and (1b), generates two three-phase current systems with a displacement of 30° in the rectifiers R_a and R_b. The two three-phase currents form a line input 12-pulse current
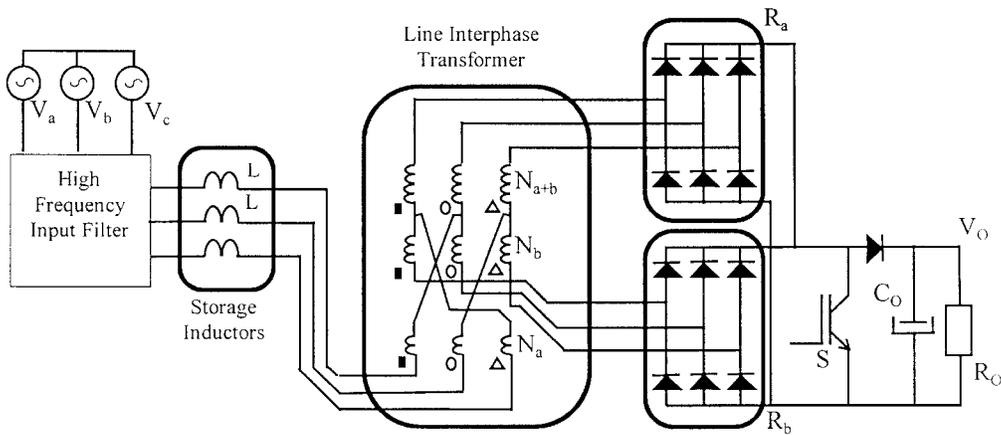
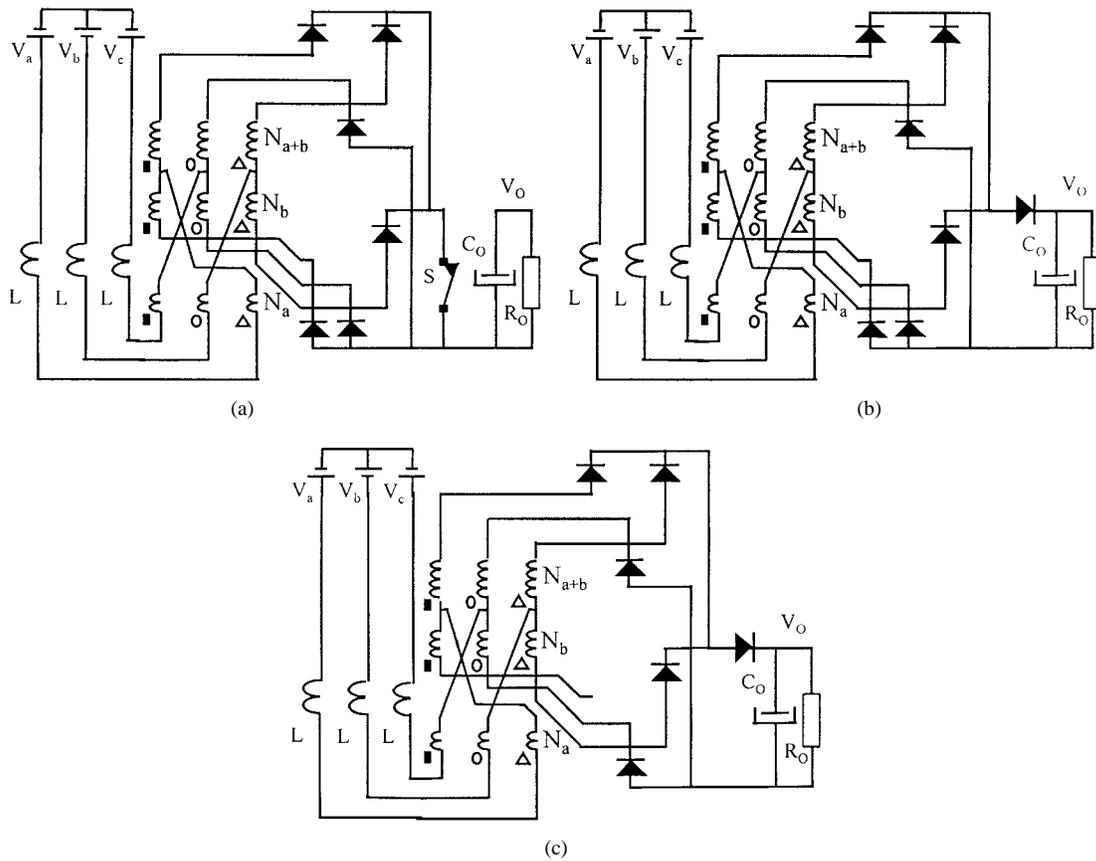$$\frac{N_a}{N_b} = 0.366 \tag{1a}$$

Fig. 3. The proposed circuit.

(a)

(b)

(c)

Fig. 4. Topological stages for $0° \leq \theta \leq 15°$ when: (a) switch S is closed, (b) switch S is opened, first power transfer stage, and (c) switch S is opened, second power transfer stage.

$$N_{a+b} = N_a + N_b. \tag{1b}$$

The order of the harmonics of the line current that is generated by a line-commutated converter can be calculated by

$$n = k \cdot p \pm 1 \tag{2}$$

where

n order of harmonics;
p number of pulses;
k $1, 2, 3, \cdots$.

In a 12-pulse rectifier system, the lowest order input current harmonics are the eleventh and thirteenth, with a balanced input voltage source. Obviously, the input current harmonics fifth and seventh are theoretically eliminated.

The boost converter operates at constant and high frequency, such that the currents through L are discontinuous. These discontinuous currents also circulate through the LIT. Therefore, the bulky low-frequency LIT used in the classic 12-pulse rectifier system can be replaced with a ferrite core LIT, with a significant size reduction.

Nonideal operating conditions, such as input voltage unbalance, input voltage distortion, inequality among the transform-

ers that form the high-frequency LIT, and the LIT magnetizing current component, prevent the complete elimination of the harmonics fifth and seventh. However, as it will be experimentally demonstrated in Section VI of this paper, they are very small.

III. PRINCIPLE OF OPERATION

In order to simplify the analysis, the following is assumed.
- The switching frequency is much higher than the line frequency.
- The semiconductors are ideal.
- The transformers have negligible magnetizing currents.
- The high-frequency input filter is removed.
- The output circuit has a large capacitor.
- The phase sequence is positive (abc).

The phase voltages are given by

$$v_a = V_{pk} \sin(wt) \tag{3a}$$
$$v_b = V_{pk} \sin(wt - 120°) \tag{3b}$$
$$v_c = V_{pk} \sin(wt + 120°). \tag{3c}$$

The operation of the converter is cyclically repeated every 30°. Therefore, its operation can be completely characterized once the interval from 0° to 30° is described.

In the interval from 0° to 15°, the polarities of the input voltages remain unchanged, as shown in Fig. 4.

The topological stages along a switching period inside this interval are described as follows.

1) First Stage—Energy Storage, Fig. 4(a): During this stage the switch S is kept closed. The LIT secondary windings are short circuited by the rectifiers R_a and R_b and the boost inductor currents rise linearly. The equivalent circuit is shown in Fig. 5(a).

2) Second Stage—First Power Transfer Stage, Fig. 4(b): During this second stage, the switch S is kept off. Due to the presence of the LIT, the current i_{L_a} continues rising linearly while the currents i_{L_b} and i_{L_c} start decreasing linearly. This stage ends at the instant that the current through the winding N_b reaches zero. The equivalent circuit is shown in Fig. 5(b).

3) Third Stage—Second Power Transfer Stage, Fig. 4(c): During this stage, the currents through the boost inductors decrease linearly and reach zero simultaneously. The equivalent circuit is shown in Fig. 5(c).

4) Fourth Stage—Zero Inductor Currents, Fig. 5(d): After the currents become null in the boost inductors, all rectifiers are blocked and the load is supplied only by the output capacitor.

Fig. 5 shows the equivalent circuits for each ideal case. Fig. 7 shows the typical instantaneous currents for the boost inductors from 0° to 15°. For $15° \leq \theta \leq 30°$, a similar operation will occur with basically the same equivalent circuits. The only equivalent circuit difference occurs in the first power transfer stage, which is presented in Fig. 6. All currents start decreasing linearly.

The final currents at the end of the first stage can be expressed by (4), where V_{IN} and I_{pk} are the instantaneous input phase voltage and peak boost inductor current at the
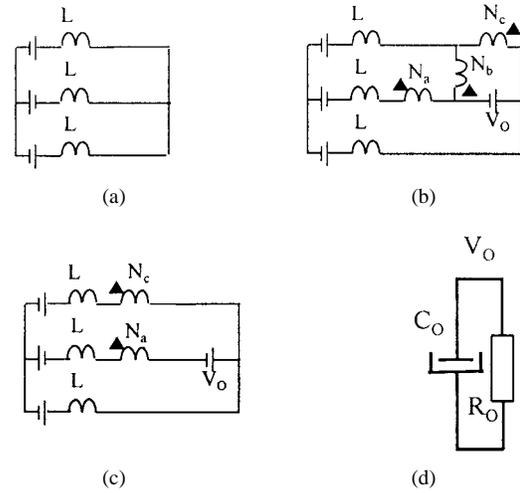

Fig. 5. Equivalent circuit for $0° \leq \theta \leq 15°$ when: (a) switch S is closed, (b) switch S is opened, first power transfer stage, (c) switch S is opened, second power transfer stage, and (d) zero inductor currents.

switching frequency, respectively,

$$I_{pk} = \frac{V_{pk}}{L} T_{\text{ON}}. \tag{4}$$

The equivalent circuit of the first stage is the same for all the topological combinations, while the corresponding instantaneous phase voltage may differ. Therefore, the final current of this stage has a sinusoidal envelop as shown in Fig. 8.

With a small high-frequency input filter, the input current becomes a practically sinusoidal waveform with only small eleventh and thirteenth harmonic current components.

IV. RELEVANT ANALYSIS RESULTS

An analysis was made using an equivalent single-phase circuit for the critical situation and $\theta = 15°$, which is shown in Fig. 9, where

$$V_O^1 = \frac{(2+\sqrt{3})}{6} V_O \tag{5a}$$
$$V_b = \frac{(\sqrt{6}+\sqrt{2})}{4} V_{pk}. \tag{5b}$$

The voltage ratio is defined as

$$\beta = \frac{V_O}{V_{LL}}. \tag{6}$$

The output current is given by

$$I_O = \frac{2+\sqrt{3}}{8} \frac{V_{PK}}{fs \cdot L} D^2 \frac{1}{0.789\beta - 1} \tag{7}$$

where

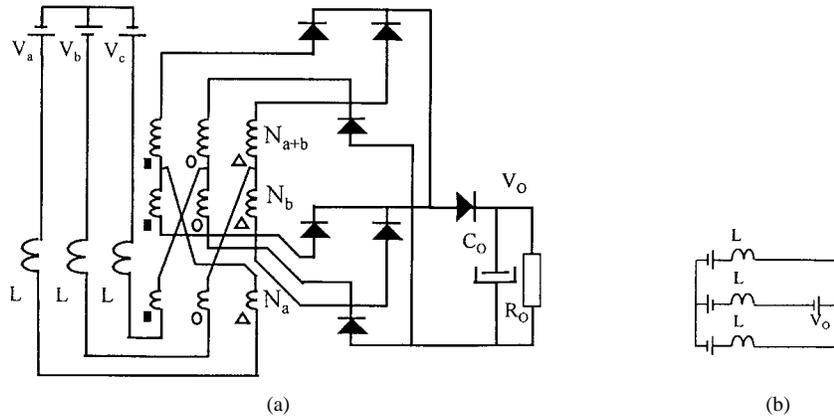|	
V_{LL}	rms value of the line-to-line voltage;
V_O	output voltage;
V_{PK}	peak phase input voltage;
L	line boost inductor;
fs	switching frequency;
D	duty cycle

Fig. 6.   (a) Topological circuit at the first power transfer stage for $15° \leq \theta \leq 30°$ and (b) equivalent circuit.
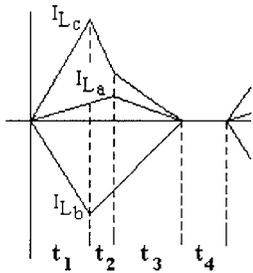

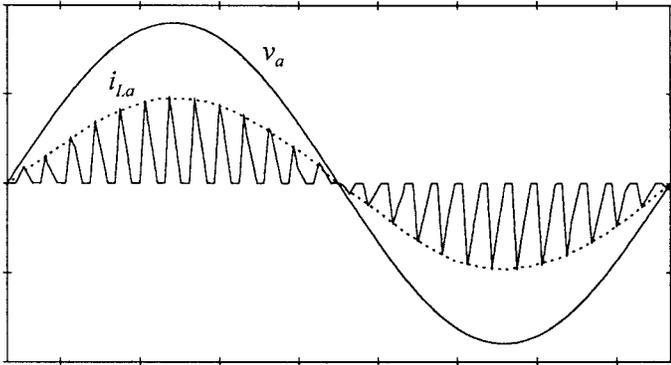Fig. 7.   Inductors current for $0° \leq \theta \leq 15°$.

Fig. 8.   Boost inductor current at the line frequency.

and normalizing one obtains

$$\overline{I}_O = D^2 \frac{1}{0.789\beta - 1} \tag{8a}$$

$$\beta = \frac{\overline{I}_O + D^2}{0.789 \cdot \overline{I}_O}. \tag{8b}$$

By analytical and numerical approaches, the most relevant curves representing the behavior of the output characteristics are shown in Fig. 10. They represent the output voltage versus the output current, taking the duty cycle as a parameter.

To ensure the discontinuous current mode (DCM) operation, the storage inductor L must be lower than L_{DCM}, given by

$$L_{\text{DCM}} = 0.38 \cdot \frac{V_O^2 \cdot \eta}{\beta \cdot Po \cdot fs} \cdot \overline{I}_O. \tag{9}$$
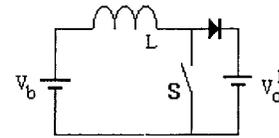

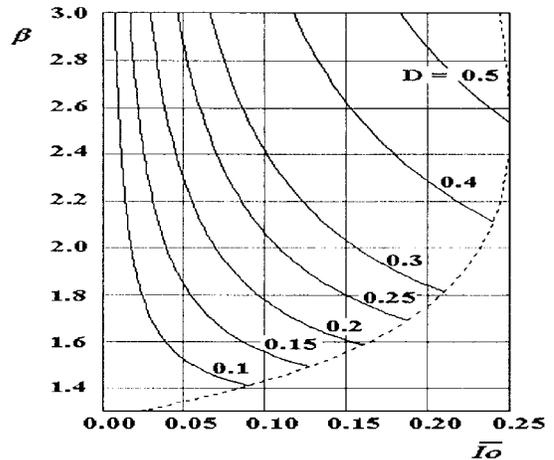Fig. 9.   Equivalent single-phase circuit for critical situation.

Fig. 10.   Output characteristics.

The boost inductor peak current, or the switch peak current, can be obtained by

$$I_{pk} = 0.816 \cdot \frac{V_{LL}}{L \cdot fs} \cdot D \max. \tag{10}$$

To help the design, the normalized current stresses are indicated in Figs. 11–13, respectively.

The other current stresses can be obtained using the following expressions.

• Average diode current in each diode of the bridge rectifiers

$$I_{Dpm} = 0.166 \cdot (I_O + I_{Sm}). \tag{11}$$

• The rms boost inductor current

$$I_{Lef} = 0.732 \cdot I_{Tef}. \tag{12}$$

• The peak voltage across the switch

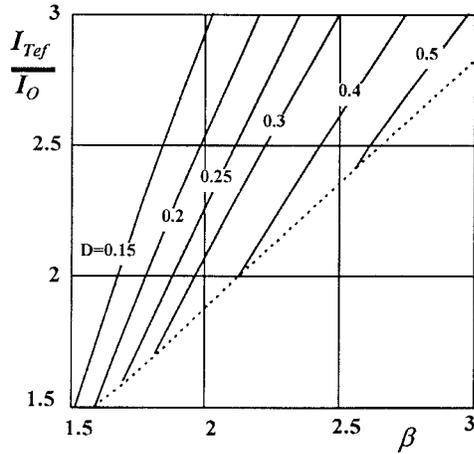$$V_{\text{RRM}} = V_O. \tag{13}$$

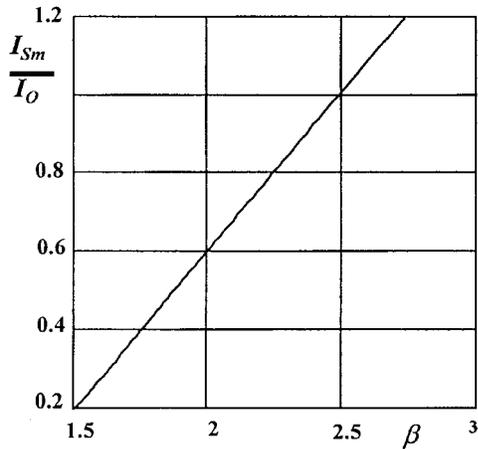Fig. 11.   Total normalized rms output current before the principal switch.
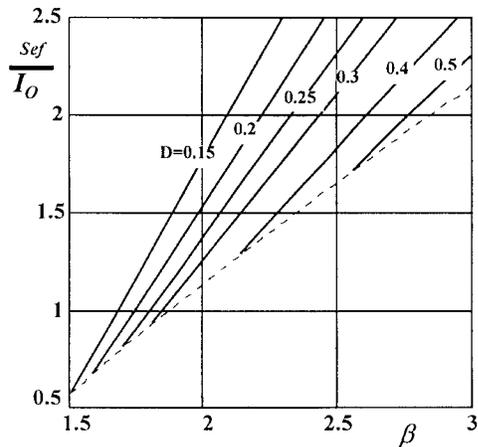

Fig. 12.   Normalized average switch current.

Fig. 13.   Normalized rms switch current.

The LIT number of turns can by obtained as follows.

1) Total secondary number of turns

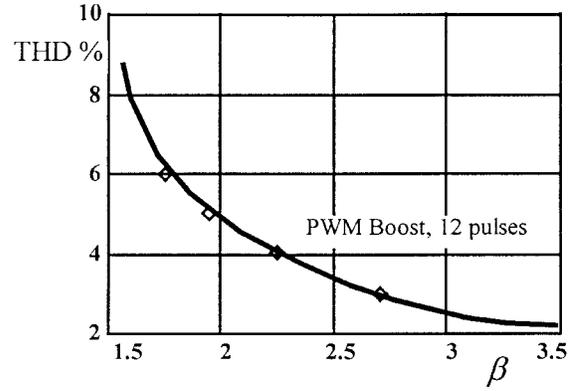$$N_T = \frac{(1 - D \max) \cdot V_O \cdot 10^4}{\beta \cdot fs \cdot Bm \cdot Ae} \qquad (14)$$

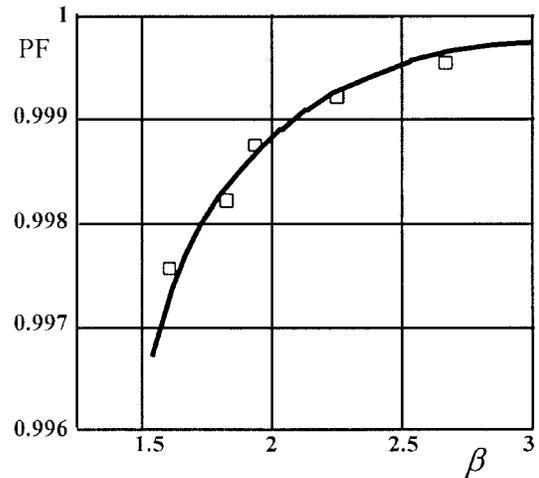Fig. 14.   Total harmonic distortion obtained by numerical analysis.

Fig. 15.   Power factor obtained by numerical analysis.

where

$$Bm = \text{maximum magnetic flux density}$$
$$Ae = \text{core area.}$$

2) Primary number of turns

$$N_a = 0.155 \cdot N_T. \qquad (15)$$

3) First secondary number of turns

$$N_b = 0.423 \cdot N_T. \qquad (16)$$

Other relevant analysis results concern the PF and the total harmonic distortion (THD). For a sinusoidal input voltage, the PF, before the input filter, is expressed by

$$PF = \frac{\cos \phi_{(1)}}{\sqrt{1 + THD^2}} \qquad (17a)$$

$$THD = \frac{\sqrt{\sum_{2}^{\infty} I_n^2}}{I_1}. \qquad (17b)$$

For passive rectifiers the $\cos \phi$ is unity. The THD is obtained by a numerical approach, as shown in Fig. 14. Those characteristics (Figs. 14 and 15) show that the PF is higher than 0.996 for $\beta > 1.5$ and the THD is very low.
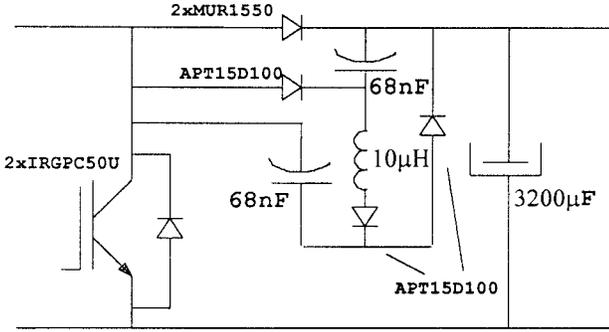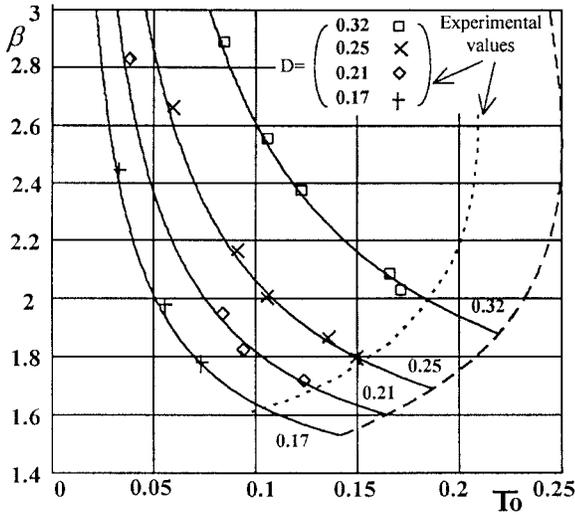
Fig. 16. Regenerative snubber.

Fig. 17. Normalized output characteristic.

Fig. 18. Total harmonic distortion.

Fig. 19. Power factor.

V. DESIGN PROCEDURE

A simple design procedure is presented for the proposed topology. An example is given for the following specifications:

$$V_{LL} = 220 \text{ V (60 Hz)} \quad V_O = 400 \text{ V}$$
$$P_O = 6000 \text{ W} \quad \eta = 0.9 \quad fs = 26 \text{ kHz}.$$

1) With β given in (6) (in Fig. 10), the normalized output current and the maximum duty cycle (D max), are obtained. Therefore

$$\beta = 1.81 \quad \overline{I}_O = 0.20 \quad D\max = 0.3.$$

2) With the output power, normalized output current and efficiency given, the maximum inductor (L) that ensures DCM operation can be obtained by using (9). Therefore

$$L = 37.6 \,\mu\text{H} \quad I_O = 15 \text{ A}.$$

3) With the established inductor value, the peak switch current is given by (10). Therefore

$$I_{pk} = 54.5 \text{ A}.$$

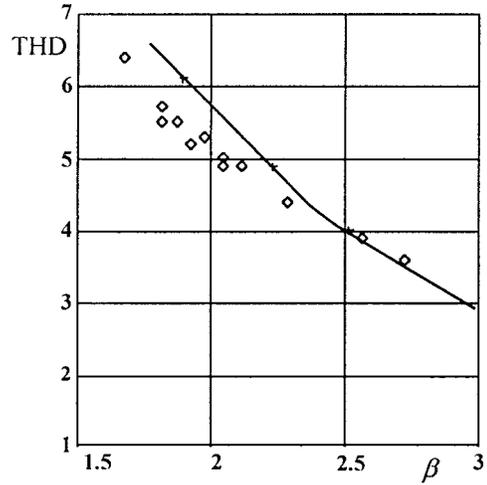4) With D max and the output current established, the current stresses can be obtained from (11) to (13) and
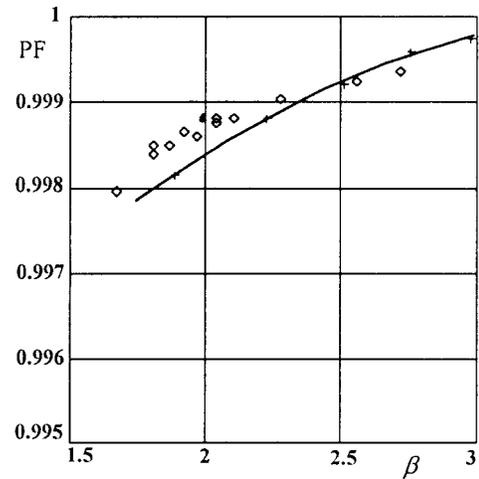
Figs. 11–13. Therefore

$$\overline{I}_{Tef} = 1.7 \qquad \overline{I}_{Sef} = 0.9 \qquad \overline{I}_{Sm} = 0.45$$
$$I_{Tef} = 25.5 \text{ A} \qquad I_{Sef} = 13.5 \text{ A} \qquad I_{Sm} = 6.75 \text{ A}$$
$$I_{Lef} = 18.6 \text{ A} \qquad I_{Dpm} = 3.61 \text{ A}.$$

5) The maximum blocking voltage of the semiconductors, is given by (14)

$$V_{\text{RRM}} = 400 \text{ V}.$$

6) By selecting a THORNTON'S E65/36 IP6 core, and by using (14)–(16), the number of turns are calculated. The obtained number of turns are

$$N_T = 45 \quad N_b = 19 \quad N_a = 7.$$

The LIT is formed by 12 E65/36 ferrite cores with a total weight of 10 kg, while the LIT weight for low-frequency operation was 32 kg.

VI. EXPERIMENTAL RESULT

A laboratory prototype has been set up with the parameters and specifications obtained in Section V. The value used for
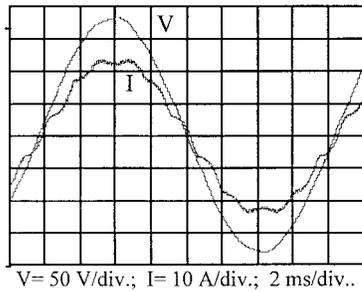
V= 50 V/div.; I= 10 A/div.; 2 ms/div..

Fig. 20.   Experimental line current and phase voltage.
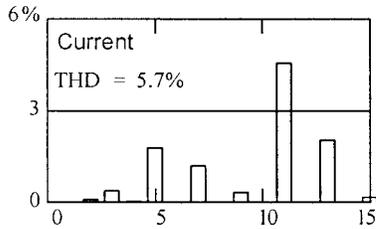
Fig. 21.   Line current harmonic component.
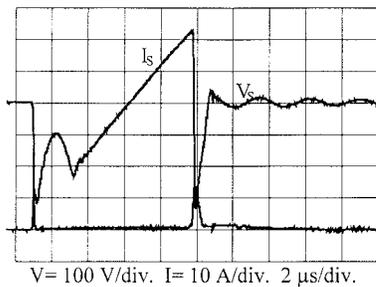

V= 100 V/div. I= 10 A/div. 2 µs/div.

Fig. 22.   Switch voltage and current.

the boost inductor is $L = 24$ μH, taking into account the transformer's leakage inductance and the necessary demagnetizing time. The output capacitor is $C_o = 3200$ μF.

The selected semiconductors are

diode bridge rectifier $\rightarrow$ MUR1550

output diode $\rightarrow$ $2 \times$ MUR1550

main switch $\rightarrow$ $2 \times$ IRGPC50U (IGBT).

Due to the turn-off losses of insulated gate bipolar transistors (IGBT's), it is necessary to apply soft switching to obtain the expected power. Fig. 16. presents a passive circuit to attenuate the turn-off losses. It is a regenerative snubber for the principal switch. A complete study of this snubber can be found in [4]. This circuit is very robust as it does not have any auxiliary active switch. Experimental results from a 6-kW 400-V prototype are shown in Figs. 17–23. From the laboratory prototype, the estimated limit on the magnetizing current to achieve DCM operation is shown in Fig. 17.

Figs. 18 and 19 show the graphical comparison between analytical and experimental values. In these figures, all the continuous lines are analytical values. These results verify the analytical approach.

Figs. 20 and 21 verify the predicted behavior and indicate that a PF of 0.998 and a THD of 6% have been obtained for
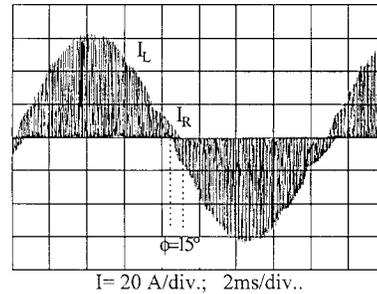

I= 20 A/div.;   2ms/div..

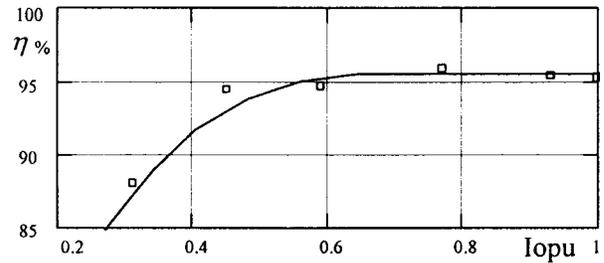Fig. 23.   Experimental input and output current in the LIT.

Fig. 24.   Experimental efficiency.

an output power of 6 kW. It is noticed that the third, fifth, and seventh harmonics in the input current are reduced. The eleventh harmonic amount is equal to 5% of harmonic distortion. The little low-frequency distortion (<11th harmonic) which can be seen is caused by the preexistent voltage line distortion.

Fig. 22 shows that the snubber circuit operation provides soft commutation for the IGBT.

Fig. 23 shows the displacement between input (I_L) and output (I_R) LIT current, and Fig. 24 shows the efficiency for a large load range.

VII. CONCLUSIONS

From the theoretical and experimental studies presented in this paper, we draw the following conclusions.

- The theoretical analysis and the design methodology have both been experimentally verified.
- The proposed technique is suitable for many commercial and industrial applications, such as conventional and uninterruptible power supplies.
- The design guidelines provide a simple procedure for the selection of components.

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