A Flying-Capacitor ZVS PWM 1.5 kW DC-to-DC Converter with Half of the Input Voltage Across the Switches

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***Abstract*—This paper introduces an isolated flying-capacitor dc-to-dc converter which features half of the input voltage across the switches, zero-voltage-switching, operation at constant frequency, regulation by pulse-width-modulation, and low rms current stress upon power switches. The complete operating principle, theoretical analysis, relevant equations and design example are provided in this paper. The experimental results of a 1.5 kW converter with 60 V, 25 A output, 600 V input, operating at 50 kHz switching frequency are also presented and discussed in the paper. The proposed converter is an alternative to the full-bridge ZVS-PWM dc-to-dc converter in high-input voltage applications.**

***Index Terms*—DC–DC converters, multilevel converters, power supply, soft switching.**

I. Introduction

In THE design of high frequency switching mode power supplies for high power applications, the conventional full-bridge zero-voltage-switching pulse-width-modulation (FB-ZVS-PWM) converter [1]–[3] is considered one of the best alternatives. This converter possesses the most desirable characteristics of both the hard switching PWM and the soft switching converters, while avoiding their major drawbacks, such as commutation losses in the first group, and variable switching frequency and high conduction losses in the second group. However, the conventional FB-ZVS-PWM converter is not suitable for high input voltage applications because the total input voltage is applied across its blocking switches.

Efforts have been made to find alternatives for the conventional FB- ZVS-PWM converter with the purpose of reducing the voltage across the switches allowing the use of popular and low cost semiconductor devices with low blocking voltage capability.

Among the studied alternatives are the multilevel topologies [4]–[8] that consist of a commutation cell using series-connected semiconductors with clamping circuits ensuring the voltage sharing across the blocking switches. The multilevel technique solves the problems of static and dynamic sharing of the voltage and limits the dV/dt to standard levels [4].

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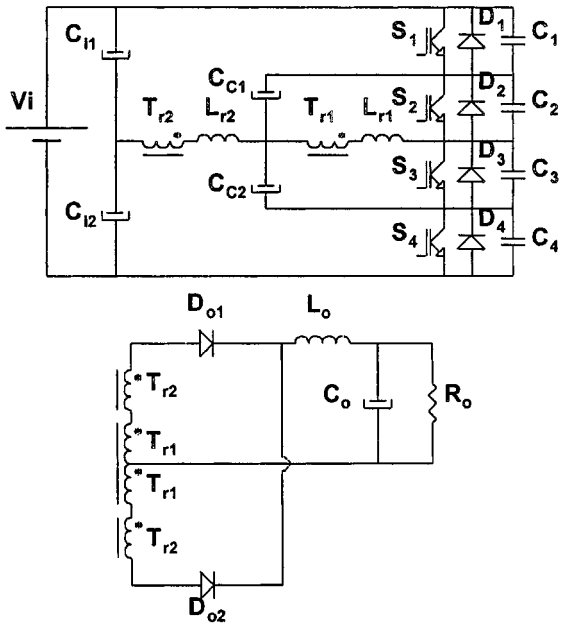

Fig. 1. Proposed ZVS PWM dc-to-dc converter.

This paper presents the analysis, design procedure and experimental results of an isolated dc-to-dc converter based on the flying-capacitor multilevel cell shown in Fig. 1. This converter is controlled by pulse-width-modulation featuring ZVS commutation and half of the input voltage is the maximum voltage applied across the switches.

II. The Circuit and Principle of Operation

A. Circuit Description

The converter which is presented in Fig. 1 can be described as a cascade connection of the primary side of two half-bridge converters with complementary duty-ratio control [9]. One of the converters is formed by capacitors C_{i1} and C_{i2}, switches S_1 and S_4 and transformer T_{r2}. The other one is formed by capacitors C_{C1} and C_{C2}, switches S_2 and S_3 and transformer T_{r1}.

The inductances L_{r1} and L_{r2} along with snubber capacitors C_1–C_4 provide a resonant transition permitting zero-voltage turn-on that eliminates turn-on switching power losses. Capacitors C_1–C_4 also provide capacitive turn-off snubbing reducing the commutation losses.

The output stage of the converter is formed by the series connection of the secondary center-tapped windings of the

transformers T_{r1} and T_{r2}, associated with rectifiers D_{o1} and D_{o2} and an output filter composed of L_o and C_o.

B. Principle of Operation

The following assumptions are made to simplify the analysis: all components are considered ideal; the output filter is large enough to be considered as a current source with a value equal to the load current I_o; the transformers turns ratio is equal to one; and the inductances L_{r1} and L_{r2} are referred to the secondary.

Fig. 2 shows the topological stages of the converter for a half-period of operation and Fig. 3 shows the key waveforms for one switching period.

First Stage (t_0, t_1): During this stage the load current flows through S_3, D_1, C_{C1} and C_{C2}. The voltage $v_{Tr1}+v_{Tr2}$ is zero, and the output rectifiers D_{o1} and D_{o2} are conducting, short-circuiting the output stage ($v_{Io} = 0$). At this stage switch S_1 is gated on at zero-voltage and zero-current [Fig. 2(a)].

Second Stage (t_1, t_2): This stage begins at time t_1, when S_3 is gated off and turns off in a soft switching manner. Voltage v_{C3} increases from zero to $Vi/2$, while v_{C2} decreases from $Vi/2$ to zero. This stage ends at t_2, when D_2 is directly polarized and starts conducting. The load current flows through output rectifiers D_{o1} and D_{o2} [Fig. 2(b)].

Third Stage (t_2, t_3): During this stage, the current $i_{Tr1} = i_{Tr2} = i_{Lrs1} - i_{Lrs2}$ flows through diodes D_1 and D_2, and decreases linearly. During the conduction of D_2, switch S_2 is gated on at zero-voltage and zero-current [Fig. 2(c)].

Fourth Stage (t_3, t_4): When i_{Tr1} reaches zero, D_1 and D_2 turn off, and S_1 and S_2 start conducting. Current i_{Tr1} increases linearly in the reverse direction. Output rectifiers D_{o1} and D_{o2} are conducting the load current and the output stage remains short-circuited ($v_{Io} = 0$) [Fig. 2(d)].

Fifth Stage (t_4, t_5): This stage begins when i_{Tr1} reaches load current I_o. Output rectifier D_{o2} turns off naturally, and only through D_{o1} the load current does flow. The output voltage v_{Io} is equal to $v_{Tr1}+v_{Tr2}$, and power is transferred from the input to the load [Fig. 2(e)].

Sixth Stage (t_4, t_5): This stage begins when S_2 is turned off. Voltage v_{C2} increases form zero to $Vi/2$, while v_{C3} decreases from $Vi/2$ to zero, with a constant current. This stage ends at instant $T_s/2$, when D_3 is directly polarized and starts conducting. The load current flows through D_{o1} [Fig. 2(f)].

The second half period is identical to the first one with switches S_1 and S_4 replacing S_2 and S_3 at the commutation stages. The corresponding waveforms are presented in Fig. 3.

III. Relevant Analysis Results

A. Output Characteristics

The linear variation of the current through the resonant inductors causes a reduction in the effective duty-cycle on the load, as shows Fig. 3. This fact is given by (1).

$$V_o = Vi \cdot \left(D - \frac{2 \cdot f_s \cdot L_{rs} \cdot I_o}{Vi} \right) \tag{1}$$

where

f_s is the switching frequency;

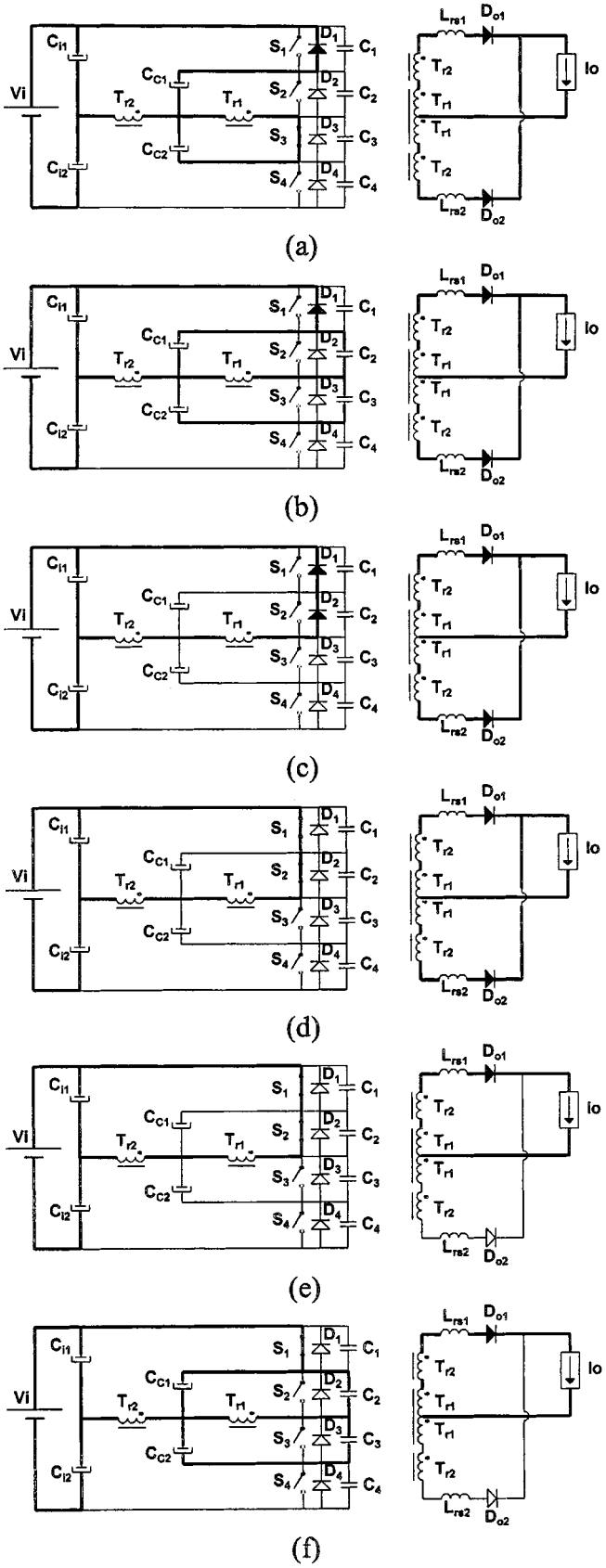

Fig. 2. Stages of operation.

D is the duty-cycle;

L_{rs} is given by (2).

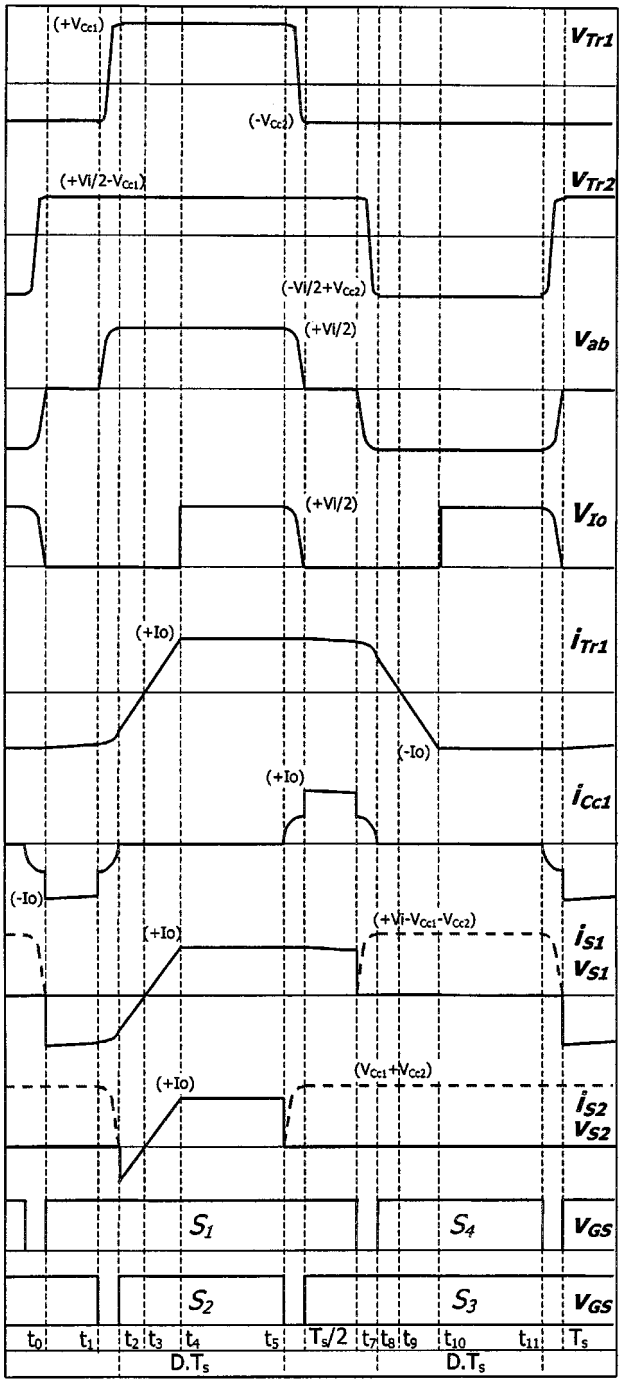

Fig. 3. Key waveforms.

$$L_{rs} = L_{rs1} = L_{rs2} = 2 \cdot (L_{r1} + L_{r2}). \tag{2}$$

According to (1), which represents the dc voltage conversion ratio of the converter, it can be noticed that the larger L_{rs} is, the larger the reduction of the output voltage caused by the reactive voltage drop will be.

B. Commutation Analysis

This converter presents two different commutations in its switches.

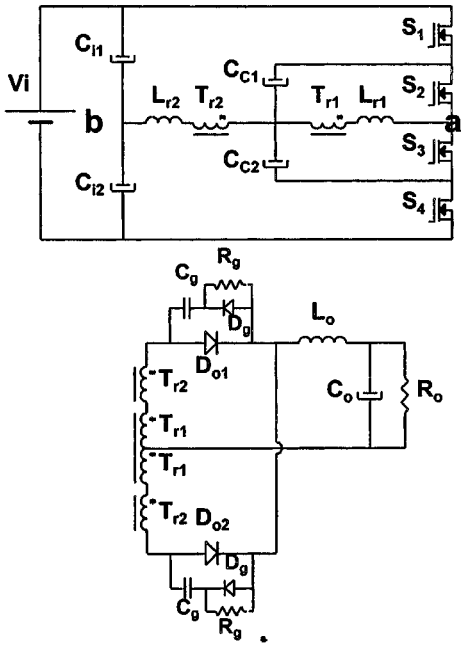

Fig. 4. Complete power stage diagram.

In stage 6, the charge/discharge of the capacitors in parallel to the switches occurs with constant current I_o.

The most critical commutation takes place during the second stage where the charge and discharge of the capacitors in parallel with the switches occurs at the resonance stage between the inductor L_{rs} and the capacitors C_2 and C_3.

The following condition, defined in (3), must be respected to ensure soft commutation:

$$I_o \geq \sqrt{\frac{4 \cdot C}{L_{rs}}} \cdot \frac{Vi}{2}. \tag{3}$$

The wider the load range with ZVS is, the higher the reactive voltage drop across the inductance L_{rs}. A good design involves sacrificing the soft commutation at light load, where the conduction losses are low, in order to obtain high efficiency at full load.

C. Voltage Sharing

The maximum voltage across the pair of switches S_1–S_4 and S_2–S_3 (Fig. 3) is defined by (4) and (5).

$$V_{S14\,\max} = Vi - (V_{Cc1} + V_{Cc2}) \tag{4}$$

$$V_{S23\,\max} = (V_{Cc1} + V_{Cc2}). \tag{5}$$

The voltage across the clamping capacitors is defined by (6) and (7).

$$V_{Cc1} = \frac{Vi}{2} \cdot (1 - D) \tag{6}$$

$$V_{Cc2} = \frac{Vi}{2} \cdot D. \tag{7}$$

Therefore

$$V_{Cc1} + V_{Cc2} = \frac{Vi}{2}. \tag{8}$$

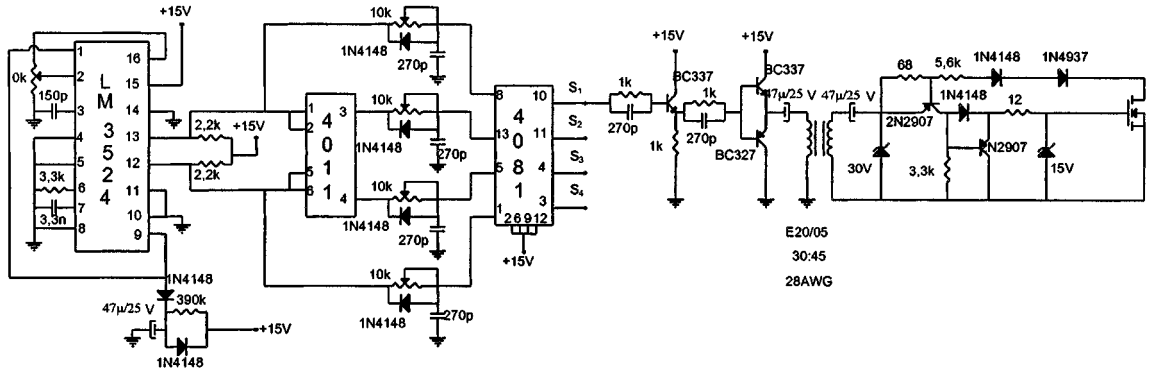

Fig. 5. Control signal generation and MOSFET's gate drive circuitry.

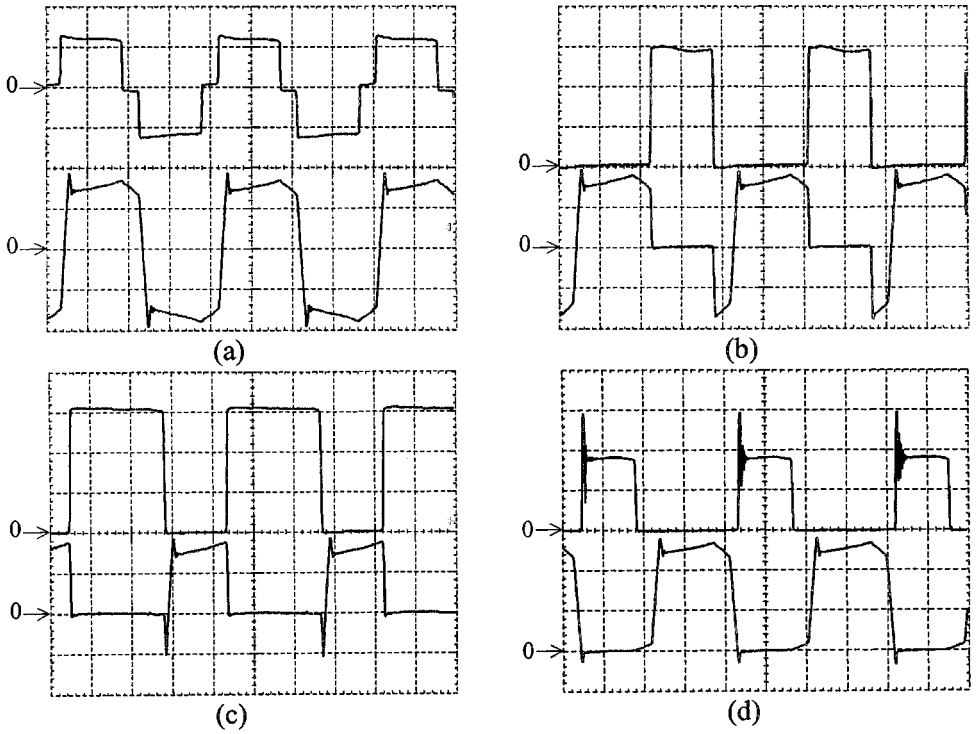

Fig. 6. Experimental waveforms: (a) top trace: voltage v_{ab} (250 V/div) and bottom trace: current i_{Lr2} (5 A/div), (b) top trace: drain-to-source voltage v_{DS1} (100 V/div), bottom trace: drain current i_{D1} (5 A/div), (c) top trace: drain-to-source voltage v_{DS2} (100 V/div), bottom trace: drain current i_{D2} (5 A/div), and (d) top trace: catode-to-anode voltage v_{Do1} (100 V/div), bottom trace: anode current i_{Do1} (10 A/div), time scale: 5 μs/div.

Consequently, based on (8) one can say that the maximum voltage across any blocking switch is half of the input voltage Vi.

IV. Design Procedure and Example

The design procedure of the converter presented in this paper is similar to that of the FB-ZVS-PWM converter [2], and of the ZVS-PWM dc-to-dc converter based on the NPC cell [5], and also on the flying capacitor cell [6], [7]. A simplified approach is presented in this section.

A. Input Data

Rated output power	$P_O = 1.5$ kW;
Input voltage	$Vi = 600$ V;
Output voltage	$V_O = 60$ V;
Switching frequency	$f_S = 50$ kHz;
Output current ripple	$\Delta I_O = 2.5$ A;
Output voltage ripple	$\Delta V_O = 0.06$ V;
Clamping voltage ripple	$\Delta V_{Cc} = 3$ V;
Minimum efficiency	$\eta = 90\%$;
Maximum duty-cycle	$D_{\max} = 0.4$;
Maximum duty-cycle reduction	15%;
ZVS load range	30–100%.

B. Transformers Turns Ratio

The reduction of the duty-cycle can be calculated by (9), and the transformers turns-ratio by (10).

$$\Delta D = 0.15\, D\max = 0.06 \tag{9}$$

$$n = \frac{Vi}{V_o} \cdot (D\max - \Delta D) = 3.4. \quad (10)$$

C. Resonant Inductances

The resonance inductance, taking into consideration the duty-cycle reduction, is calculated by (11).

$$L_{rtot} = \frac{\Delta D \cdot Vi \cdot n}{4 \cdot I_o \cdot f_s} = 24.5\ \mu\text{H}. \quad (11)$$

Subtracting the total leakage inductance of the transformers (8.4 μH), one obtains L_{r1} and L_{r2} equal to 8 μH.

D. Clamping Capacitances

The clamping capacitances to achieve the clamping voltage specification is given by (12).

$$C_{C1} = C_{C2} = \frac{I_o}{n \cdot f_s \cdot \Delta V_{Cc}} \left(\frac{1}{2} - D\max\right) = 4.9\ \mu\text{F}. \quad (12)$$

E. Active Switches Stress

The MOSFET's selection to perform ZVS at high frequency must be done considering the rated rms drain current, peak current and maximum drain-to-source voltage, which can be calculated using (13)–(15):

$$I_{D\text{rms}} = \frac{I_o}{n \cdot \eta}\sqrt{\frac{1}{2} - \frac{5}{6}\Delta D} \therefore I_{D\text{rms}} = 5.48\ \text{A} \quad (13)$$

$$I_{Dpk} = \frac{I_o}{n \cdot \eta} \therefore I_{Dpk} = 8.17\ \text{A} \quad (14)$$

$$V_{DS\ \max} = \frac{Vi}{2} \therefore V_{DS\ \max} = 300\ \text{V}. \quad (15)$$

The IRFP460 MOSFET was chosen as it features the above mentioned requirements.

F. Output Rectifier Diodes Stress

The diodes must be selected taking into consideration the rated average current, peak current and maximum reverse voltage that can be calculated using (16)–(18):

$$I_{Doavg} = \frac{I_o}{2} \therefore ID_{oavg} = 12.5\ \text{A} \quad (16)$$

$$I_{Dopk} = I_o + \frac{\Delta I_o}{2} \therefore I_{Dopk} = 26.25\ \text{A} \quad (17)$$

$$V_{DRM} = \frac{Vi}{n} \therefore V_{DRM} = 176.47\ \text{V}. \quad (18)$$

The MUR1560 diode was chosen as it features the above mentioned requirements.

G. Output Rectifier Diodes Clamping Circuits

In order to limit the voltage overshoot and ringing across the output rectifiers diodes, caused by the leakage inductances of the transformers, a voltage clamp circuit is selected using the methodology proposed in [3].

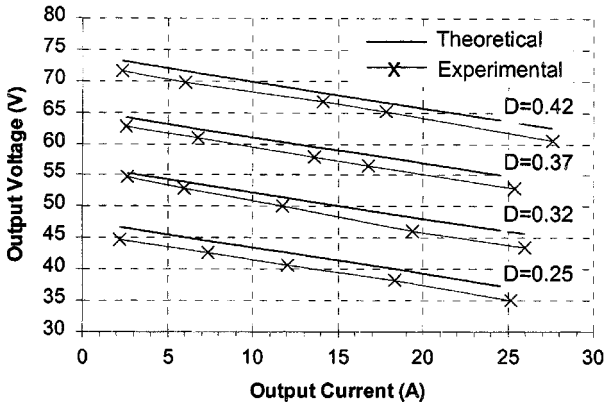

Fig. 7. Output voltage as a function of output current.

H. ZVS Load Range

The minimum output current that guarantees zero-voltage-switching can be determined by (19):

$$I_{O\ \min} = n \cdot \frac{Vi}{2} \cdot \sqrt{\frac{C_{ds}}{L_r}} = 5.8\ \text{A} \quad (19)$$

This guarantees a ZVS load range of about 23.2–100% which meets the soft commutation requirements.

V. Experimental Results

Based on the design given in Section IV, a prototype has been implemented. The power stage of the converter is shown in Fig. 4, using the following components:

S_{1-4}	IRFP 460–500 V, 20 A (Harris);
D_{o1-2}	MUR 1560–600 V, 15 A (Motorola);
T_{r1-2}	Ferrite core E65/39–IP 12 (Thornton)–Primary: 17 turns–Secondary: $5+5$ turns–22 AWG;
L_{r1-2}	8 μH–ferrite core E30/7–IP12 (Thornton);
L_o	89 μH–ferrite core E55/28/21–IP12 (Thornton);
C_o	470 μF/100 V–electrolytic (Icotron);
C_{C1-2}	5×1 μF/250 V–polypropylene (Icotron);
C_{i1-2}	2 μF/400 V–polypropylene (Icotron);
D_g	MUR140–400 V, 1A (Motorola);
C_g	10 nF/400 V–polypropylene (Icotron);
R_g	24 kΩ/5 W.

The MOSFET's body diodes were used for D_1–D_4 and MOSFET's intrinsic capacitances for C_1–C_4 of Fig. 1. The implemented control signal generation and MOSFET's drive circuit is shown in Fig. 5.

Experimentally obtained waveforms for P_o equal to 1.5 kW, I_o of 25 A, Vi equal to 600 V, f_s of 50 kHz and D equal to 0.42 are shown in Fig. 6.

The theoretical and experimental output characteristics of the converter for different values of D are presented in Fig. 7, which confirms (1) with the output voltage decreasing with an increase of the output current due to the reduction of the effective duty-cycle.

The experimentally measured efficiency as a function of the load current is shown in Fig. 8. The efficiency at full load (25 A) is equal to 92%. The main sources of losses are diode and MOSFET conduction losses, and magnetic and snubber losses.

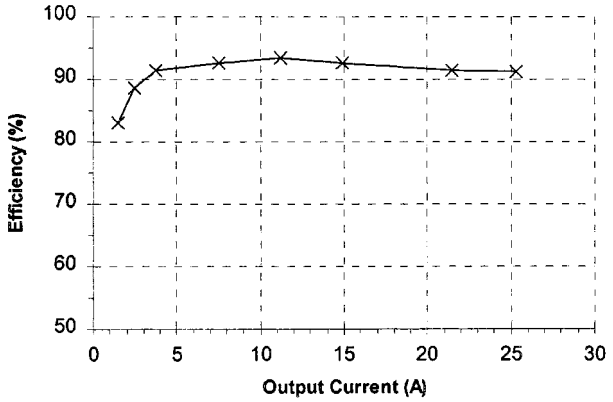

Fig. 8. Efficiency as a function of output current.

The switching losses at full load are practically null, as it can be observed in Fig. 6(b) and (c), due to the zero-voltage switching.

The magnetic losses in this converter are higher than the magnetic losses in other three-level dc-to-dc converters due to the need of two power transformers [9].

From Fig. 8 it can be observed that the efficiency clearly decreases for load currents lower than 5 A when the ZVS commutation is lost and the converter starts to operate with hard-switching as predicted in (19).

VI. Conclusions

The Flying-Capacitor ZVS PWM 1.5 kW dc-to-dc Converter was introduced in this paper.

From the theoretical and experimental studies conducted by the authors and reported in the paper, we can drawn the conclusions as follows.

1) The proposed converter presents identical output and soft switching characteristics to the FB-ZVS-PWM converter [1].
2) The voltage across the switches is equal to the half of the input voltage, like the conventional Three-Level ZVS-PWM Converter [5].
3) The processed power is naturally shared between two high frequency transformers. This is a desirable feature in high power applications.
4) The number of components, the size, the volume and the efficiency (92%) of a laboratory prototype rated and 1.5 kW and 50 kHz is similar to the others three-level dc-dc Converters. However, any study has been performed in order to optimize the size and efficiency.

It is the authors opinion that at this stage of the development of the design of Three-Level ZVS PWM based power supply, none of the known circuits can be considered better or worse. The experience and the time will indicate which one in the best for specific application in this context. This new circuit is one additional option to the designers.

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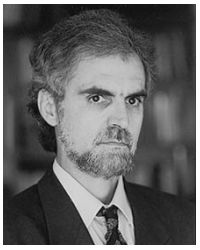

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