Abstract—This paper proposes a zero-voltage-switching scheme for the three-level capacitor clamping inverter. The proposed small-rating auxiliary circuit ensures not only zero-voltage switching of the main switches and zero-current switching of the auxiliary switches, but the clamping capacitor voltage of the inverter is also stabilized. The scheme prevents any voltage or current spikes from happening over the main or auxiliary switches and no modulation constraints are incurred. Operation, analysis, designing, and testing aspects of the scheme are detailed.

Index Terms—Multilevel inverter, soft switching.

I. INTRODUCTION


In the recent decade, the neutral-point-clamped (NPC) [1] inverter has been increasingly used in such high-power applications as traction, industrial drives, and flexible-ac-transmission-systems (FACTS) [2], [3]. With the available switching devices, the NPC inverter increases the per-unit capacity while it reduces the output voltage harmonics. However, the NPC inverter has the following drawbacks.

1) While the two outer switches are directly clamped by the clamping diodes, the two inner switches are not directly clamped. As can be observed from field tests [4], [5], the inner switches will see higher blocking voltage depending on the stray inductance of the neutral rail [6].

2) The redundancy in switching state giving different zero-sequence conditions (1, 1, 0 ↔ 0, 0, –1, for example) at the inverter output must be attributed to neutral potential control [7], and the dc-link voltage utilization [8] cannot be optimized consequently.

3) Unless two legs are used [9], a single NPC leg cannot work as a multilevel chopper, and the range of application is limited.

As opposed to the NPC inverter, the three-level capacitor clamping inverter [10], [11] offers an alternative for high power conversion and has the following features.

1) Assuming stable clamping capacitor voltage, all four switches will be directly clamped. As ac current at the switching frequency flows through the clamping capacitor, the capacitance will be small [12], although the challenge arises in selecting the type of the capacitor [13].

2) The redundancy in switching state giving different zero-sequence conditions can now be attributed to dc-link voltage utilization, while the controlling of the clamping capacitor voltage where necessary can be left to the additional redundancy in switch combination for the “0” state of each leg [14].

3) Besides inverter mode operation [15], the capacitor clamping inverter can also work as a multilevel chopper [16], [17].

As such, the three-level capacitor clamping inverter represents an interesting alternative to the NPC inverter for high power conversion.


To the end of high-frequency operation in a high-power converter, the use of soft switching has been deemed a highly promising solution [12], [21]. Soft switching of a multilevel inverter can always be obtained by extending the resonant pole techniques [22] appropriately to each two-level switching cell in the multilevel inverter.

The ARCPI circuit [18], as given in Fig. 1, has always been referred to as the most suited structure for a high-power converter. However, no field application has been reported in the literature. The difficulty of the technique consists in the center-tap structure of the dc-link capacitor. On the one hand, this structure limits the voltage source for the commutation resonance to half dc-link voltage, which warrants for the “boost” stage to be introduced as discussed in [18]. On the other hand, possible fluctuation of the center-tap potential renders the circuit unreliable [23], especially when asymmetrical working conditions leading to dc drift of the potential are taken into account [24].

The true-PWM-pole soft-switching scheme [19], as shown in Fig. 2, utilizes a half-bridge structure in the auxiliary circuit, avoiding the center-tap configuration in the ARCPI scheme, while an autotransformer is used for synthesizing the voltage source for the commutation resonance. The voltage source so synthesized can then be valued at more than half dc-link voltage by setting properly the autotransformer ratio \( k_T = N_2/N_1 < \).
Fig. 1. ARCPI [18].

Fig. 2. True-PWM-pole zero-voltage-switching pole inverter proposed in [19], where $k_{T1} = N_2/N_1 < 1/2$, which enables simultaneous turn-off of the main switch with turn-on of the corresponding auxiliary switch. The need for a "boost" stage for the commutation as needed in the ARCPI scheme is removed.

In particular, in comparison with the ARCPI scheme, the auxiliary switch current in the true-PWM-pole circuit is nearly halved $(1 - k_{T1})$ times, $k_{T1} = N_2/N_1 < 1/2$, as the resonant inductor current is shared between the auxiliary switch and the autotransformer primary winding.

Nevertheless, it is found that magnetization of the autotransformer in the true-PWM-pole structure is not able to be reset following each commutation, due to the freewheeling paths existing between the auxiliary devices and the main devices through windings of the autotransformer, which renders the scheme not practically applicable.

The transformer-assisted PWM zero-voltage switching scheme recently proposed [20] $(k_{T2} = N_2/N_1 < 1/2)$, as shown in Fig. 3, solves the autotransformer resetting problem by means of a transformer replacing the autotransformer in the auxiliary circuit, while the bridge configuration of the auxiliary devices is kept. The scheme allows for reliable operation with no extra control. Unfortunately, the feature of current sharing with the true-PWM-pole scheme is lost. The auxiliary switch carries almost the same current as that in the ARCPI scheme as a result.

Reference [12] has reported several ideas for achieving soft switching for the capacitor clamping inverter. In particular, an auxiliary resonant commutated pole three-level capacitor clamping converter was discussed in [26], where commutations of both the two-level switching cells are assisted by a single resonant pole [27], [28]. The auxiliary switch will see twice the main switch blocking voltage. Moreover, commutations of one switching cell will interfere with the commutations of the other cell, as the two cells are independent from each other.

C. Objective of This Paper

This paper proposes a zero-voltage-switching three-level capacitor clamping inverter. The circuit employs the transformer-assisted PWM zero-voltage-switching scheme in the inner switching cell and the true-PWM-pole zero-voltage-switching scheme in the outer switching cell. The true-PWM-pole in the outer switching cell no longer suffers from the autotransformer magnetization resetting problem existing in the normal two-level true-PWM-pole inverter, because of the clamping capacitor involved in the resonant paths. Most significantly, however, due to the charging and discharging paths established by the true-PWM-pole auxiliary circuit, the clamping capacitor voltage as well as the dc-link neutral potential is forced to be stable, and no specific feedback control is needed as a consequence. Operation, analysis, designing, and testing of the circuit will be reported in the paper.

II. PROPOSED CIRCUIT AND ITS OPERATION

A. Proposed Circuit and Its Soft Switching

Fig. 4 shows the circuit scheme of the proposed zero-voltage-switching three-level capacitor clamping inverter. In the main circuit, $S_2/S_3$ is a switching pair forming the outer switching cell, whereas $S_2/S_3$ is another switching pair forming the inner switching cell. Given a constant clamping capacitor ($C_m$) voltage, the two cells are actually independent from each other. Each cell can be controlled by the normal subharmonic PWM pattern, with the two carriers for the two...
switching cells being phase shifted by \( \pi \), offering an optimal output spectrum [15].

Evidently, the commutation of the inner switching cell \( S_2/S_3 \) is assisted by the auxiliary branch \( S_{a2}/S_{a3} \) exactly in the same way as in the two-level case [20].

Given further a stable dc-link neutral potential at \( O \), i.e., \( V_{Cl} = V_{C2} = V_{dc}/2 \), the outer switching cell \( S_1/S_4 \) will actually see a similar commutation procedure as the inner switching cell. For \( D_4 \) to \( S_1 \) commutation, referring to Figs. 5 and 6, the procedure is described as follows.

**Step 1)** \((t_0 - t_1):\) Circuit steady state. \( D_4 \) and \( D_3 \) carry the load current. Inverter output is at the minus level. The clamping capacitor \( C_m \) is at the floating state.

**Step 2)** \((t_1 - t_2):\) When \( S_4 \) is turned off at \( t_1 \), \( S_{a4} \) is turned on simultaneously, leading to conduction of \( D_{a4} \) and a reflected voltage of \( [k'(1 + k')]V_{dc}/2 \) on the secondary winding \( N_2 (k' = N_2/N_1' < 1) \). Capacitor \( C_2 \) voltage \( (V_{dc}/2) \) then joins the \( N_2' \) voltage establishing a voltage source of \( [1/(1 + k')]V_{dc}/2 \) forcing the current decreasing in \( D_4 \). The clamping capacitor is charged. Auxiliary switch \( S_{a4} \) works with inductive turn-on. Step 3) \((t_2 - t_3):\) \( D_4 \) blocks at \( t_2 \), initiating a resonance among \( L_{a14}, C_{a1} \) and \( C_{a1} \), forced by the established voltage source of \( [1/(1 + k')]V_{dc}/2 \). \( C_{a1} \) is charged while \( C_{a2} \) is discharged. Main switch \( S_4 \) works with capacitive turn-off.

**Step 4)** \((t_3 - t_4):\) Upon full discharging of \( C_{a1} \) at \( t_3 \), \( D_1 \) starts conduction and \( S_1 \) gating signal is released by the zero-voltage detecting circuit installed across it. The resonant inductor current continues to decrease.

**Step 5)** \((t_4 - t_5):\) \( S_1 \) starts carrying current as the resonant inductor current falls below the load current at \( t_4 \). The resonant inductor current continues to decrease. Main switch \( S_1 \) works with zero-voltage turn-on.

**Step 6)** \((t_5 - t_6):\) Upon extinction of the resonant inductor current at \( t_5 \), \( S_1 \) takes the full-load current charging the clamping capacitor \( C_m \). Gating signal for \( S_{a1} \) can be withdrawn at \( t_6 \) considering a margin from \( t_5 \). Auxiliary switch gating signal width is predetermined to be a constant covering the maximum commutation duration at the peak load current [20], and remains the same for all auxiliary switches. Auxiliary switch \( S_{a4} \) works with zero-current turn-off. During \( t_6 - t_7 \), inverter output is at the zero level.

**Step 7)** \((t_7 - t_8):\) When \( S_1 \) is turned off at \( t_7 \), \( S_{a1} \) is turned on simultaneously, leading to conduction of \( D_{a1} \) and a reflected voltage of \( [k'(1 + k')]V_{dc}/2 \) on \( N_2 \). Capacitor \( C_1 \) voltage \( (V_{dc}/2) \) then joins the \( N_2' \) voltage establishing a voltage source of \( [1/(1 + k')]V_{dc}/2 \) forcing the resonance among \( C_{a1}, C_{a4} \) and \( L_{a14} \). \( C_{a1} \) is charged while \( C_{a4} \) is discharged. Main switch \( S_1 \) works with capacitive turn-off while auxiliary switch \( S_{a1} \) works with inductive turn-on.

**Step 8)** \((t_8 - t_9):\) Upon full discharging of \( C_{a1} \) at \( t_8 \), \( D_4 \) starts conduction carrying the sum of the load current and the resonant inductor current. Gating signal for \( S_4 \) is released by the zero-voltage detecting circuit installed across it. Clamping capacitor \( C_m \) is discharged by the auxiliary switch current. The resonant inductor current continues to decrease.

**Step 9)** \((t_9 - t_{10}):\) When the resonant inductor current extincts at \( t_9 \), \( D_1 \) starts carrying the full load current. Gating signal for \( S_{a1} \) can be withdrawn at \( t_{10} \) considering a margin from \( t_9 \). Auxiliary switch \( S_{a1} \) works with zero-current turn-off. After \( t_{10} \), inverter output returns to the minus level, and the clamping capacitor returns to the floating state.

Considering that the resonant capacitor \( C_{a2} \) is small compared to the clamping capacitor \( C_m \), charging and/or discharging current through \( C_{a2} \) is also small and has been neglected in the analysis.

Consequently, in the proposed circuit, with no extra control for the auxiliary circuit, all the main switches work at zero-voltage turn-on and capacitive turn-off, while all the auxiliary switches work at zero-current turn-off and inductive turn-on.
resulting in truly lossless commutations and, therefore, ample space for switching-frequency increase.

Stability of the clamping capacitor voltage, stability of the dc-link neutral potential (O), as well as the resetting of the magnetization of the autotransformer in the outer switching cell will be treated, respectively, in the following.

B. Clamping Capacitor Voltage Stabilization and DC-Link Neutral Potential Stabilization

Thanks to the specific configuration of the proposed circuit, the clamping capacitor voltage is prevented from being higher or lower than either of the dc-link capacitor voltages. This mechanism guarantees the stabilization of the clamping capacitor voltage as well as the stabilization of the dc-link neutral potential, as explained in the following.

When $S_1$ is gated, if the clamping capacitor voltage is lower than the up-capacitor $C_1$ voltage, then it will be charged by the up capacitor through $S_1$, $D_{sh4}$, $N_2'$ and $L_{T14}$, as shown in Fig. 7(a), whereas the down capacitor $C_2$ is also charged. In the other instance, when $S_4$ is gated, if the clamping capacitor voltage is lower than the down-capacitor $C_2$ voltage, then it will be charged by the down capacitor $C_2$ through $S_4$, $D_{sd4}$, $N_2'$, and
Fig. 7. Charging (discharging) paths for the clamping capacitor through the main circuit and the auxiliary circuit. (a) Charging path by up dc-link capacitor $C_1$ when $S_1$ is gated. (b) Charging path by down dc-link capacitor $C_2$ when $S_4$ is gated. (c) Discharging path to up dc-link capacitor $C_1$ when $S_{ad}$ is gated. (d) Discharging path to down dc-link capacitor $C_2$ when $S_{ad}$ is gated.

For $L_{T14}$, as shown in Fig. 7(b), while the up capacitor $C_1$ is also charged. As $S_1$ and $S_4$ conduct alternatively all the time except for the deadtime interval, the clamping capacitor voltage cannot be lower than either of the dc-link capacitor voltages.

Also, the clamping capacitor voltage cannot be higher than either of the dc-link capacitor voltages. Without regard to the initial value of the clamping capacitor voltage, the clamping capacitor will be discharged to the up capacitor $C_1$ through $D_1$, $L_{T14}$, $N_2$, and $S_{ad}$ during $S_4$-$S_4$ commutation when $S_{ad}$ is gated, as shown in Fig. 7(c), while the down capacitor $C_2$ is also discharged. In the other instance, it will be discharged to the down capacitor $C_2$ through $S_{ad}$, $N_2$, $L_{T14}$, and $D_4$ during $S_1$-$S_4$ commutation when $S_{ad}$ is gated, as shown in Fig. 7(d), while the up capacitor $C_1$ is also discharged. In either case, if the clamping capacitor voltage becomes lower than the corresponding up- or down-capacitor voltage when the commutation ends, it will be charged subsequently by $S_1$ or $S_4$ until reaching the corresponding up- or down-capacitor voltage. On the other hand, the commutation will not end as long as the clamping capacitor voltage is higher than the corresponding up- or down-capacitor voltage. It will end when the clamping capacitor voltage gets equal to the corresponding dc-link up- or down-capacitor voltage. Note that the auxiliary switch gating signal width has been assumed sufficient to cover the commutation duration when clamping capacitor voltage fluctuation is taken into consideration.

In summary, the clamping capacitor voltage cannot be lower than either of the dc-link capacitor voltages due to the charging paths established by the main switch $S_1$/ $S_4$. In the meantime, it cannot be higher than either of the dc-link capacitor voltages due to the discharging paths established by the auxiliary switch $S_{ad}$/ $S_{ad}$. As a result, the clamping capacitor voltage must be equal to either of the dc-link capacitor voltages, and the dc-link neutral potential must also be stable. Due to the complexity of clamping capacitor voltage control involving monitoring of the load current and the clamping capacitor voltage, the stability of the clamping capacitor voltage as well as the dc-link neutral potential is deemed an interesting property of the proposed circuit, which greatly enhances the attractiveness of the circuit.

C. True-PWM-Pole in the Outer Switching Cell

The autotransformer resetting problem arising from the true-PWM-pole zero-voltage-switching pole inverter [19] originates essentially from the commutation residual current flowing from the active auxiliary switch to the incoming main switch through the autotransformer secondary winding and the resonant inductor [25], during the interval after the autotransformer primary winding current arrives at zero and before...
the turning off of the auxiliary switch. For instance, in Fig. 2, a residual current flowing from \( S_2 \) through \( L_r \) and \( N_2 \) to \( S_{a1} \) after \( N_2 \) current reaching zero and before turning off of \( S_{a1} \) during \( D_1 \) to \( S_2 \) commutation will cause the magnetization of the autotransformer not being able to be reset when auxiliary switch \( S_{a1} \) is turned off.

For the outer switching cell of the proposed circuit, however, such residual current loop always involves the clamping capacitor and the corresponding dc-link up and down capacitors. For \( S_4 \) to \( S_5 \) commutation, for example, the loop involves \( L_{r4}, N_2 \), \( S_{a4}/D_{a4} \), \( C_m \), \( S_4/D_4 \), and \( C_2/C_1 \). For \( S_2 \) to \( S_3 \) commutation, on the other hand, the loop involves \( L_{r2}, N_2 \), \( S_{a2}/D_{a2} \), \( C_m \), \( S_4/D_4 \), and \( C_2/C_1 \). In either case, no residual current will likely to flow in the loop continuously, since at steady state the clamping capacitor voltage must be equal to the corresponding dc-link capacitor voltage and the current flowing in the loop must be zero. This is deemed reasonable taking into account the small time constant of the charging/discharging loop (resonant inductance and thermal resistance) as well as the margin considered in the auxiliary switch gating signal width design.

Without residual current, magnetization of the autotransformer will be reset appropriately. Hence, the true-PWM-pole zero-voltage-switching pole scheme becomes applicable to the outer switching cell of the proposed circuit without suffering from the autotransformer magnetization resetting problem.

As mentioned before, the true-PWM-pole zero-voltage-switching pole scheme reduces the current rating of the auxiliary switch to nearly half \[ \times \] as compared to the ARCPI circuit [18] or the transformer assisted PWM zero-voltage-switching pole circuit [20], in which cases the auxiliary switch carries the full resonant inductor current.

Note that, as shown in Fig. 4, the autotransformer winding connection has been modified in comparison with that shown in Fig. 2. The modified connection [29], [30] allows the autotransformer secondary winding to carry the auxiliary switch current, instead of the resonant inductor current, without affecting the autotransformer secondary voltage for synthesizing the auxiliary voltage source for forcing the commutation resonance. The autotransformer size is nearly halved as a result.

III. ANALYSIS AND DESIGN

Characteristic curves for the transformer-assisted PWM zero-voltage-switching pole inverter, including the commutation duration, the peak resonant inductor current, as well as the rms resonant inductor current related to the instantaneous load current, the transformer ratio, and the switching cycle, in cases of both diode to switch commutation and switch to diode commutation, have been comprehensively addressed in [20].

For design of the auxiliary circuit for the inner switching cell, the transformer ratio should be set first to less than 1/2 depending on the actual resonant loop resistance, to ensure the pole voltage to swing to the rail level during the commutation resonance. The resonant capacitance can be designed as per the device turn-off loss and the thermal conditions associated [31]. Resonant inductance can then be decided according to the acceptable resonant inductor rms current stress given in Fig. 8, taking into account the expected operating frequency of the circuit. Rating of the auxiliary device can be evaluated according to the resonant inductor peak current stress given in Fig. 9, as well as the rms current stress given in Fig. 8.

Gating signal width for the auxiliary switch can be decided referring to the commutation duration relation given in Fig. 10. Gating signal width dimensioning must also consider the necessary margin dealing with charging and discharging interaction of the clamping capacitor with the corresponding dc-link capacitor, in order to guarantee that the clamping capacitor voltage becomes equal to the corresponding dc-link capacitor voltage within the auxiliary switch conduction interval. In the meantime, the minimum pulsewidth in the inverter PWM pattern should not be less than this duration. The next commutation should not start before the conclusion of the previous commutation.

 Auxiliary transformer design can be based on the commutation (magnetization) duration information given in Fig. 10, and the resonant inductor rms current stress information given in Fig. 8. The resonant inductor can be designed based on the resonant inductor peak current information given in Fig. 9, and the resonant inductor rms current information given in Fig. 8.
Characteristic curves for the transformer-assisted PWM zero-voltage-switching pole circuit utilized in the inner switch cell can be conveniently extended to the true-PWM-pole circuit utilized in the outer switching cell. Based on these curves, the true-PWM-pole circuit can be analogously designed.

Note that throughout Figs. 8–10, $V_{\text{base}} = V_{\text{dc}}/2$, $Z_{\text{base}} = \sqrt{L_r/2C_r}$, $i_{\text{base}} = V_{\text{base}}/Z_{\text{base}}$, $\omega_0 = 1/\sqrt{2C_rL_r}$, and $t_{\text{base}} = \omega_0 t$.

IV. EXPERIMENTAL VERIFICATION

A half-bridge three-level capacitor clamping inverter prototype has been built in the laboratory. The main circuit of the prototype has been modulated by subharmonic PWM pattern, as detailed in [15]. Specifications of the prototype are given in Table I. The parameters of the half-bridge laboratory prototype are: $L_{r1} = L_{r2} = 15 \mu$H, $C_{r1} = C_{r2} = C_{r3} = C_{r4} = 0.1 \mu$F, and $N_2/N_1 = 0.4$ and $N_2'/N_1' = 0.67$. $S_1$–$S_4$ and $S_{a1}$–$S_{a4}$ used are SKM50GB123D (1200 V/50 A), $D_{a1}$–$D_{a4}$, and $D_{a2}$–$D_{a3}$ used are HFA30T60C (600 V/30 A).

In addition, dc capacitors used are $C_1 = C_2 = 3300 \mu$F, each with a nominal voltage of 350 V. The clamping capacitor in use is 2750 μF with a nominal voltage of 500 V (two 5500-μF/250-V capacitors in series). The half-bridge inverter output is installed with a second-order LC filter with $L_f = 1.45$ mH and $C_f = 12 \mu$F. Gating signal width of the auxiliary switch is set at 14.4 μs. Minimum pulsewidth is set at 28.8 μs and maximum pulse width is set at 124.8 μs. Deadtime of 2.4 μs is inserted for each switching cell. Besides, four zero-voltage detecting circuits are employed to interface the four SEMIKRON SKHI10 drivers to the four main insulated gate bipolar transistors (IGBT’s), respectively [32].

Fig. 11 shows the prototype half-bridge inverter output voltage waveform. The stable three-level output verifies well the stability of the clamping capacitor voltage as well as the

TABLE I

| Specifications of the 3-kW Half-Bridge Three-Level Capacitor Clamping Inverter Prototype |
|---------------------------------|-------|--------|---------|---------|---------|
| DC input voltage | $V_{\text{dc}}$ | $V_{\text{out}}$ | $V_{\text{base}}$ | $V_{\text{mod}}$ | $M$ |
| 600V | 120V | 0.62 |
| output power | $P_o$ | load current | $I_{\text{rms}}$ | switching frequency |
| 3kW | =25A |  |
| gate frequency | $f_m$ | 6.5kHz |

Fig. 9. Variations of the resonant inductor peak currents with load current and transformer ratio. (a) Diode to switch commutation. (b) Switch to diode commutation.

Fig. 10. Variations of commutation durations $t_{\text{on}}$ and $t_{\text{off}}$ with load current and transformer ratio. (a) Diode to switch commutation. (b) Switch to diode commutation.

Fig. 11. The prototype half-bridge inverter output voltage waveform.
Fig. 11. Experimental three-level output voltage of the 3-kW half-bridge three-level capacitor clamping inverter prototype.

Fig. 12. Experimental voltage and current waveforms of the main switch $S_1$ during $D_4$ to $S_1$ commutation and $S_1$ to $D_4$ commutation. As expected, the main switch works with zero-voltage turn-on and capacitive turn-off, and neither voltage nor current spike arises. Fig. 13 shows the experimental result of the auxiliary switch $S_{A4}$ voltage in relation to the resonant inductor ($L_{r1A}$) current and the load current during $D_4$ to $S_1$ commutation process. As can be observed, the auxiliary switch works with inductive turn-on and zero-current turn-off, without the magnetization resetting problem.

V. CONCLUSIONS

1) The proposed soft-switched three-level capacitor clamping inverter guarantees zero-voltage switching of the main switches, zero-current switching of the auxiliary switches, without incurring any voltage or current spike over the main or auxiliary switches, and without being subjected to any modulation limits. Due to simultaneous turn-off of the main switch and turn-on of the corresponding auxiliary switch, no additional monitoring or controlling for the auxiliary switch is required.

2) Due to the charging and discharging paths established by the auxiliary circuit in the outer switching cell, the clamping capacitor voltage as well as the dc-link neutral potential is forced to be stable during the operation, regardless of whether an active control of the clamping capacitor voltage has been taken.

3) Due to the clamping capacitor involved in the resonant paths, the true-PWM-pole zero voltage-switching circuit can be utilized in the outer switching cell, without suffering from the magnetization resetting problem of the autotransformer occurring in the normal two-level true-PWM-pole inverter. The current stress of the auxiliary switch is, therefore, almost halved ($1/(1 + k_f^2)$) times, $k_f = N_{2r}/N_{1r} < 1$ due to current sharing of the autotransformer windings.

4) The proposal can be used to advantage for advanced applications in high-speed drive or active power filtering areas, etc., where high-switching-frequency high-power operation is demanded.

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