Fundamentals of a New Diode Clamping Multilevel Inverter

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***Abstract*—The conventional diode clamping inverter suffers from such problems as dc link unbalance, indirect clamping of the inner devices, turn-on snubbing of the inner dc rails as well as series association of the clamping diodes etc. It is due largely to these problems that the application of the conventional diode clamping inverter in practice has been deterred, in spite of the growing discussion in the literature. The paper proposes a new diode clamping inverter, which works without the series association of the clamping diodes. An auxiliary resistive clamping network solving the indirect clamping problem of the inner devices is also discussed for both the new and conventional diode clamping inverter. Operation principle, clamping mechanism, auxiliary clamping as well as experimentation are presented.**

***Index Terms*—Multilevel inverter.**

I. Introduction

In response to the growing demand for high power inverter units, multilevel inverters have been attracting growing attention from academia as well as industry in the recent decade. Among the best known topologies are the H-bridge cascade inverter, the capacitor clamping inverter (imbricated cells), and the diode clamping inverter [1]–[3].

As reported in the literature, the H-bridge cascade inverter has been used in several practical instances for broadcasting amplifier [4], plasma [5], industrial drive [6] as well as STATCOM [7] applications etc. The main limitation of the H-bridge cascade inverter consists in the provision of an isolated power supply for each individual H-bridge cell when real power transfer is demanded. For STATCOM application, where the isolated supplies are not required, the power pulsation at twice output frequency occurring with the dc link of each H-bridge cell necessitates over-sizing of the dc link capacitors.

The capacitor clamping inverter, though the three-level scheme of which was published in the early 1980's [8], had been rarely discussed until the introduction of the "imbricated cells" [9]. The individual clamping capacitor needs only to smooth the switching frequency ripple voltage and the required capacity for each clamping capacitor is therefore small. However, as the number of level increases, such problems as thermal designing, low-inductance designing, as well as insulation designing of the system will become critical. Medium voltage drives using four-level capacitor clamping inverter has recently been available on the market [10].

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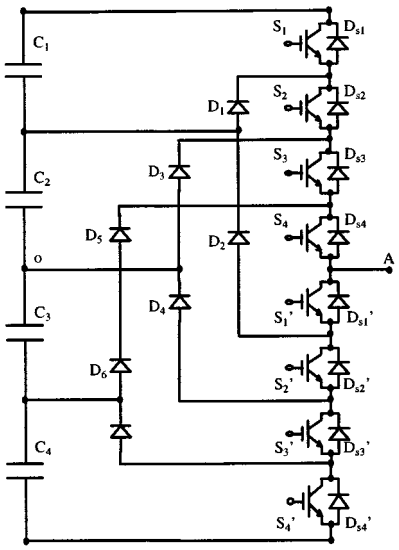


Fig. 1. Structure of the original diode clamping inverter (five level).

The diode clamping inverter, as shown in Fig. 1, published by different researchers [11]–[13] in the early 90's can be deemed as the extension of the neutral-point-clamped (NPC) inverter introduced in the early 80's [14]. Unlike the NPC inverter which has been extensively used today in industrial drives [15], tractions [16] as well as FACTS systems [17], the diode clamping inverter is right under investigation.

In addition to the dc link unbalance problem identified in the literature [18], [19], other problems with the diode clamping inverter are briefed in the following [20]:

a) Indirect clamping of the Inner devices: In a normal two-level inverter leg, each switch is directly clamped to the dc link capacitor by the opposite freewheeling diode. And no static over-voltage will possibly appear across the switch, though transient voltage spike resulted from energy release of the stray inductance at the moment of commutation can happen across the switch. Switches in the diode clamping inverter, however, are actually not directly clamped to the dc link capacitors, except for the lateral two (S_1 and S_4' in Fig. 1). Depending on the stray inductances of the structure, any indirectly clamped switch may see more than the nominal blocking voltage, which is $V_{\rm dc}/(M-1)$ for a M-level inverter, during its OFF state.

b) Turn-on snubbing for the inner dc rails: Among the M DC-rails of a M-level diode clamping inverter, each of the inner $(M-2)$ rails has to carry bidirectionally controlled current. As in the case of matrix converter, a bidirectionally current controlled rail prevents the use of polarized turn-on snubber. Non-polarized snubber is known to be especially inefficient [21].

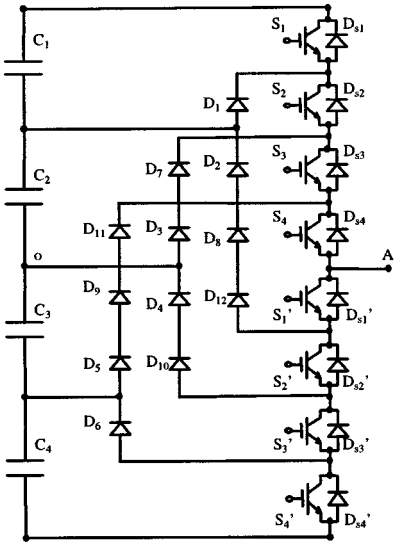


Fig. 2. Structure of the conventional diode clamping inverter with series clamping diodes (five level).

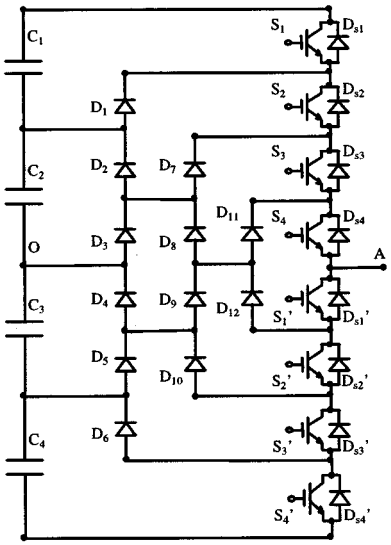


Fig. 3. Structure of the proposed new diode clamping inverter (five level).

c) Multiple blocking voltage of the clamping diodes: Even though each main switch is supposed to block the nominal blocking voltage, the blocking voltage of each clamping diode in the diode clamping inverter is dependent on its position in the structure. For a M-level leg, one can find two diodes each sees blocking voltage of

$$V_{\text{diode}} = \frac{M-1-k}{M-1} V_{\text{dc}} \tag{1}$$

where M is the number of levels, k goes from 1 to $M-2$ and V_{dc} is the total dc link voltage.

The indirect clamping problem comes inherently with the diode clamping structure of the circuit. Unless an active switch be put in parallel with each clamping diode (which achieves direct clamping), the problem may not be removed. However, the problem will be mitigated when stray inductance is reduced, or when an effective auxiliary clamping is installed.

As a result of the turn-on snubbing problem, using of switching devices like GTO's or IGCT's in the diode clamping inverter is thought to be a challenging subject. dc rails polarized turn-on snubbers [22] will worsen the static over-voltage problem of the inner devices.

As problem (c) is concerned, conventional solution has been to put appropriate number of diodes in series [1], as shown in Fig. 2. The possible over-voltages across the series diodes due to the diversities of diodes switching characteristics as well as their stray parameters call for large RC snubbing network to be introduced leading to expensive and voluminous system.

It is therefore the objective of the present paper to propose an alternative diode clamping inverter, in which problem (c) is removed while a solution for problem (a) is also proposed.

II. New Diode Clamping Inverter and Its Operation

The new diode clamping inverter is shown in Fig. 3. For the five-level case, a total of eight switches and twelve diodes of equal voltage rating are used, which are the same with the conventional diode clamping inverter with diodes in series. This pyramid architecture is extensible to any level unless otherwise practically limited. A M-level inverter leg requires $(M-1)$ storage capacitors, $2(M-1)$ switches and $(M-1)(M-2)$ clamping diodes.

A. Switching Cells and Forward/Freewheeling Paths

The new diode clamping inverter can be decomposed into two-level switching cells as its basic operation units. For the five-level case, one can define (5-1) switching cells as shown in Figs. 4(a), (b), (c) and (d). In cell (a), S_2, S_3 and S_4 are always ON, while S_1 and S_1' work alternatively connecting the inverter output to $V_{\text{dc}}/2$ and $V_{\text{dc}}/4$ respectively. Similarly, in cell (b), S_3, S_4 and S_1' are always ON, while S_2 and S_2' work alternatively connecting the inverter output to $V_{\text{dc}}/4$ and 0 respectively. In cell (c), S_4, S_1' and S_2' are always ON, while S_3 and S_3' work alternatively connecting the inverter output to 0 and $-V_{\text{dc}}/2$ respectively. And finally, in cell (d), S_1', S_2' and S_3' are always ON, while S_4 and S_4' work alternatively connecting the inverter output to $-V_{\text{dc}}/4$ and $-V_{\text{dc}}/2$ respectively.

Each switching cell works actually as a normal two-level inverter, except for that each forward or freewheeling path in the cell involves $M-1$ devices rather than only one. Taking cell (b) as an example, the forward path of the up-arm involves D_1, S_2, S_3 and S_4, whereas the freewheeling path of the up-arm involves S_1', D_{12}, D_8 and D_2, connecting the inverter output to $V_{\text{dc}}/4$ level for either positive or negative current flow, as shown in Fig. 5(a). Meantime, as shown in Fig. 5(b), the forward path of the down-arm involves $S_1', S_2'\, D_{10}$ and D_4, whereas the freewheeling path of the down-arm involves D_3, D_7, S_3 and S_4, connecting the inverter output to zero level for either positive or negative current flow.

The following rules govern the switching operation of a M-level diode clamping inverter:

a) At any moment, there must be $M-1$ neighboring switches that are ON.

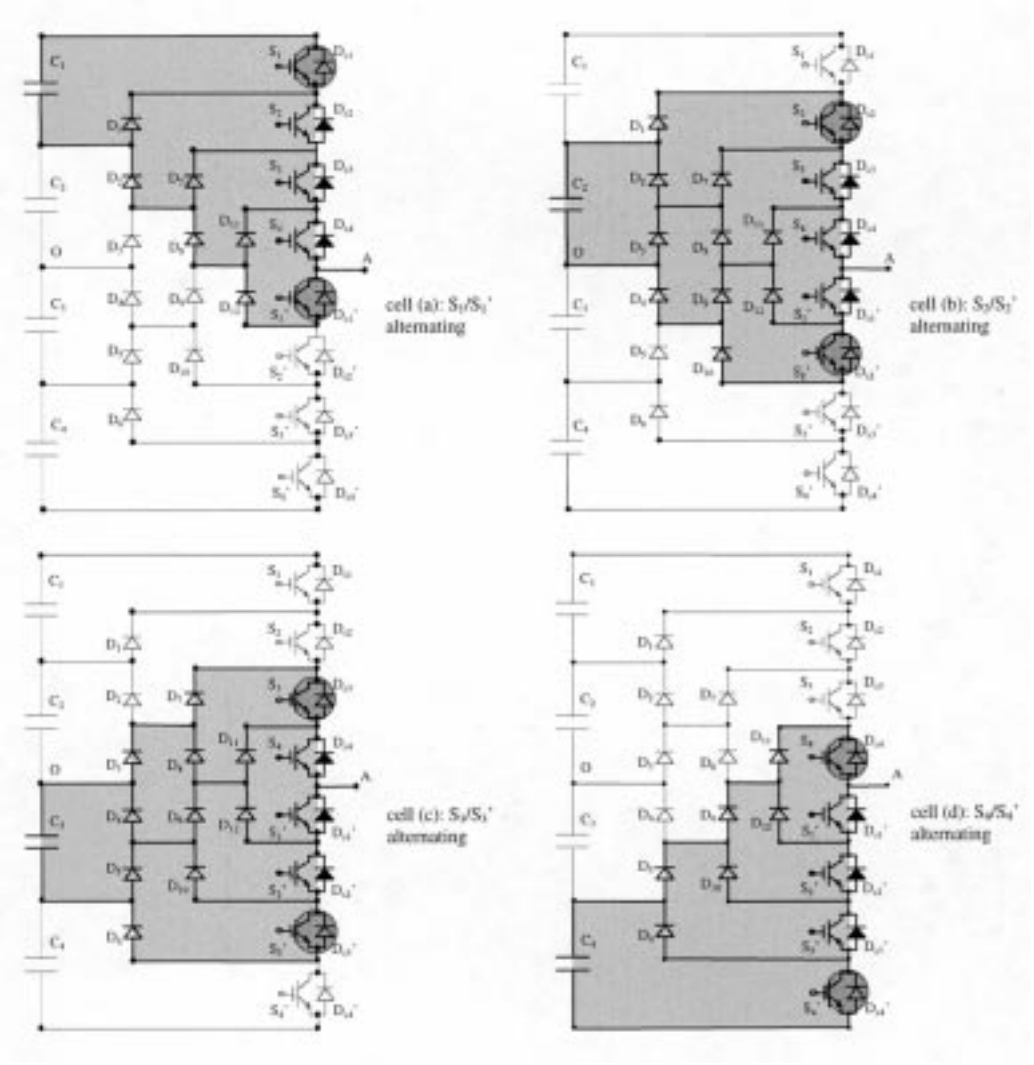


Fig. 4. Four switching cells of the proposed new diode clamping inverter.

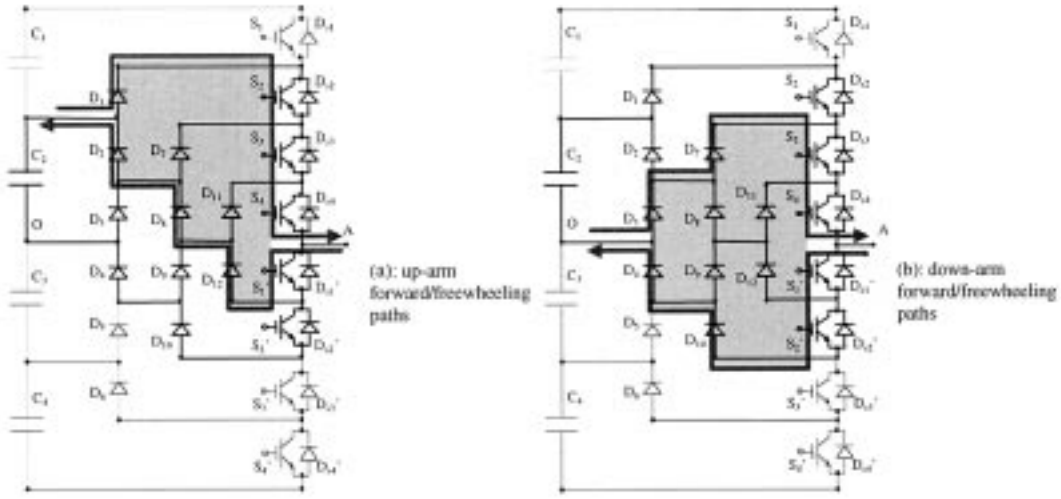


Fig. 5. Forward and freewheeling paths for the up and down arms of cell (b) in the new diode clamping inverter.

b) For each two neighboring switches, the outer switch can only be turned on when the inner switch is ON.

c) For each two neighboring switches, the inner switch can only be turned off when the outer switch is OFF.

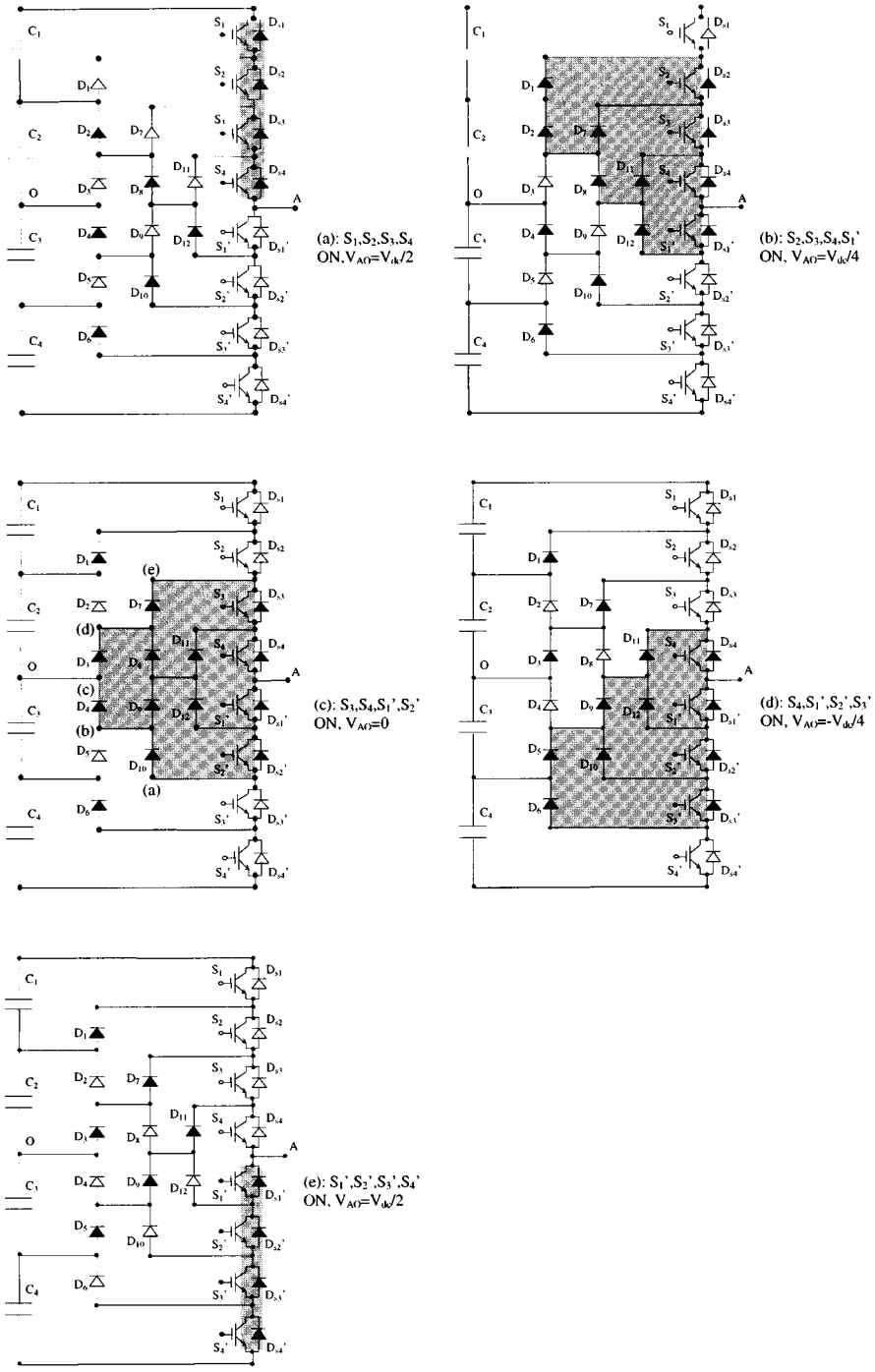


Fig. 6. Changes of the clamping diodes blocking states in relation with the blocking states of the switchs in the new diode clamping inverter.

B. Clamping Diodes Blocking States

Clamping diodes change their blocking states as the switches change their states, as shown in Fig. 6. With inverter output connected to a certain level by relevant switches, the involved clamping diodes will block zero voltage whereas the remaining clamping diodes will block zero or the nominal voltage dependent on their positions in the clamping network.

As an example, when inverter output is connected to level zero with switches S_3, S_4, S_1' and S_2' ON, as shown in Fig. 6(c), the involved clamping diodes including $D_3, D_4; D_7, D_8, D_9, D_{10}$; and D_{11}, D_{12} will all block zero voltage. All outside terminals of the arm including a, b, c, d and e will be of the same potential at zero. Then D_2 must block the nominal voltage as its cathode terminal is at level $V_{\rm dc}/4$ whereas D_5 must also block nominal voltage as its anode terminal is at level $-V_{\rm dc}/4$. Besides, as S_1 and S_4' are OFF, D_1 and D_6 must block zero voltage.

When inverter output is connected to $V_{\rm dc}/2, V_{\rm dc}/4, -V_{\rm dc}/4$ or $-V_{\rm dc}/2$, as it may happen, the corresponding clamping

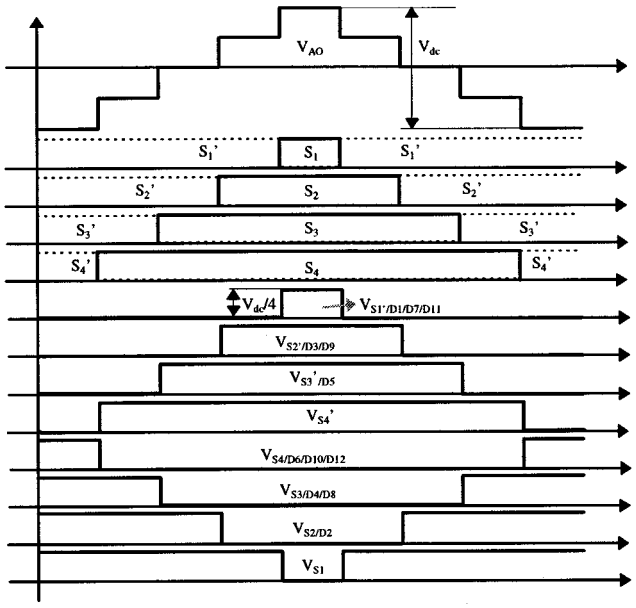


Fig. 7. Inverter output voltage synthesizing in association with the blocking states of switches and clamping diodes in the new diode clamping inverter.

diodes blocking states can be deducted similarly, as shown by the other diagrams in Fig. 6.

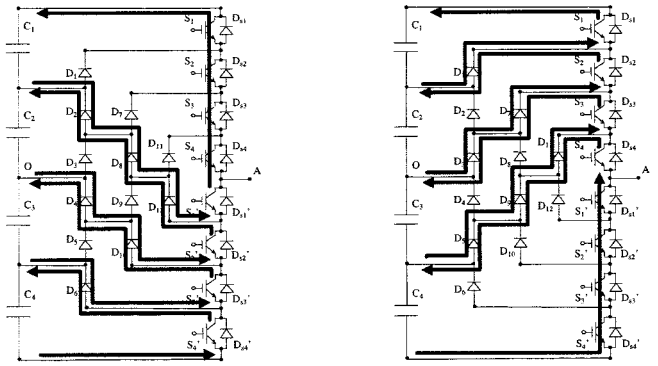
To summarize, in the new diode clamping inverter, D_1, D_7, D_{11} always follow S_1'; D_3, D_9 always follow S_2'; D_5 always follows S_3'; whereas D_6, D_{10}, D_{12} always follow S_4; D_4, D_8 always follow S_3; D_2 always follows S_2, without regard to the inverter output level. Inverter output voltage synthesizing in association with blocking states of switches and clamping diodes is shown in Fig. 7.

III. Clamping Mechanism and Auxiliary Clamping of the New Diode Clamping Inverter

A. Switch and Diode Clamping Mechanism

As the name of the diode clamping inverter implies, any main switch in the string at blocking state must be clamped to a corresponding dc link capacitor via relevant clamping diodes. By which, blocking voltage of the main switch will be constrained to the nominal value. This mechanism in the proposed diode clamping inverter will be discussed below.

Referring back to Fig. 4, in cell (a), S_2, S_3 and S_4 are always ON, while S_2', S_3' and S_4' are always OFF, S_1 and S_1' work alternatively connecting the inverter output to $V_{\rm dc}/2$ and $V_{\rm dc}/4$ respectively. Obviously, S_1 is directly clamped to C_1 by D_1 after it's turn-off, while S_1' in series with D_2, D_8 and D_{12} is indirectly clamped to C_1 by D_{s1}, D_{s2}, D_{s3} and D_{s4} after its turn-off. Further, D_{11} in series with D_2 and D_8 is indirectly clamped to C_1 by D_{s1}, D_{s2} and D_{s3}; D_7 in series with D_2 is indirectly clamped to C_1 by D_{s1} and D_{s2}, while D_1 is directly clamped to C_1 by D_{s1}. Suppose that for cell (a), S_2', S_3' and S_4' each blocks $V_{\rm dc}/4$ voltage, and D_2, D_8, D_{12} each blocks zero voltage. Then, S_1 and S_1', D_1, D_7, D_{11} are all clamped to C_1 at $V_{\rm dc}/4$ when OFF. Among which S_1 and D_1 are directly clamped while S_1', D_7 and D_{11} are indirectly clamped.



(a) (b)

Fig. 8. Clamping mechanism for the new diode clamping inverter. (a) Clamping mechanism for the down-arm switches. (b) Clamping mechanism for the up-arm switches.

Similar mechanism can be witnessed with cell (b), where D_2, D_3 are directly clamped to C_2, while S_2', D_9, S_2 are indirectly clamped to C_2. In cell (c), D_4, D_5 are directly clamped to C_3, while S_3', S_3, D_8 are indirectly clamped to C_3. In cell (d), S_4', D_6 are directly clamped to C_4, while S_4, D_{10}, D_{12} are indirectly clamped to C_4.

Graphical illustration of the clamping mechanism for the new diode clamping inverter is shown in Fig. 8(a) and (b).

In summary, for the proposed new diode clamping inverter, not only the switches are clamped, so are the clamping diodes. Among which, the 8 lateral devices ($S_1, S_4', D_1, D_2, D_3, D_4, D_5$, and D_6) are directly clamped, whereas the remaining devices ($S_2, S_3, D_8, S_4, D_{10}, D_{12}, S_1', D_7, D_{11}, S_2', D_9, S_3'$) are indirectly clamped, to the corresponding dc link capacitors.

B. Indirect Clamping and Blocking Voltage Distribution

Indirect clamping will possibly result in unequal voltage distribution among the blocking devices, due mainly to the stray inductances in the structure. In the following text, the commutation process from S_1', D_{12}, D_8, D_2 to $D_{s4}, D_{s3}, D_{s2}, D_{s1}$ will be considered. As S_1' is indirectly clamped, S_1', D_{11}, and D_7 will have to block more than the nominal voltage during the OFF state.

Prior to commutation, S_2, S_3, and S_4 are ON. Upon the releasing of the turn-off signal for S_1', the stray capacitance of S_1' will first be charged. Until the voltage across the stray capacitance of S_1' reaches $V_{\rm dc}/4$, freewheeling diodes D_{s1}, D_{s2}, D_{s3}, and D_{s4} will conduct, leading to demagnetization of the stray inductance (L_s) in the clamping path, as shown in Fig. 9. The trapped energy in Ls will be absorbed by the stray capacitance of S_1' together with the stray capacitances of S_2', S_3', and S_4'. The stray capacitance of S_1' will continue be charged, whereas the stray capacitances of S_2', S_3', and S_4' will be discharged. Such over-charging and discharging will not be recovered subsequently, as the discharging path for the stray capacitance of S_1', and the charging path for the stray capacitances of S_2', S_3', and S_4' are both blocked by D_2, D_8, and D_{12}. Consequently, S_1' will block more than $V_{\rm dc}/4$ voltage while S_2', S_3', and S_4' together will block less than $3V_{\rm dc}/4$ voltage during the steady state. Moreover, D_2, D_8 and D_{12} together sees the difference

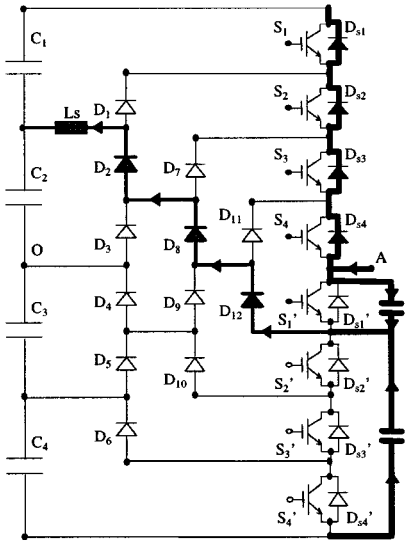


Fig. 9. Stray inductance demagnetization during the commutation process from S_1', D_{12}, D_8 and D_2 to D_{s1}, D_{s2}, D_{s3}, and D_{s4} in the new diode clamping inverter.

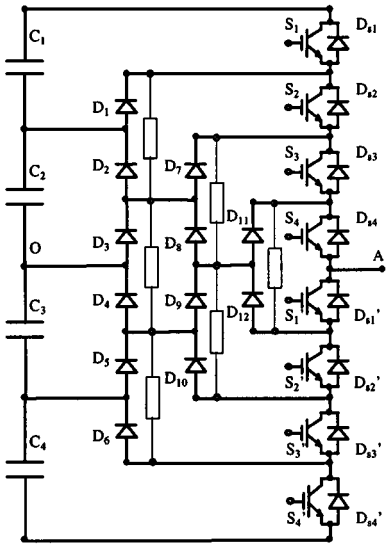


Fig. 10. An auxilairy clamping network configuration for the new diode clamping inverter. Trapped energy in L_s is now absorbed by C_b as S_1' is turned off.

between the blocking voltage of S_1' and $V_{\rm dc}/4$. Meanwhile, D_{11} sees $V_{\rm dc}/4$ plus V_{D2} and V_{D8}, D_7 sees $V_{\rm dc}/4$ plus V_{D2}, while D_1 sees $V_{\rm dc}/4$.

Indirect clamping and the subsequent unequal blocking voltage distribution problem holds also for S_2' and S_2, S_3' and S_3, and S_4, together with their relevant clamping diodes in cell (b), cell (c) and cell (d).

Due to the fact that the stray capacitance of the neighboring outer switch experiences one more discharging than the inner switch, among the blocking devices, the outer switch will always block less voltage while the inner device will always block more voltage. The center device will always be exposed to the highest voltage stress.

Unequal blocking voltage distribution problem arising from indirect clamping exists also with the conventional diode clamping inverter as mentioned in Section I. The severity of this problem is dependent on the stray inductances of the structure. With refined bus-bar designing technique, and in particular, appropriate positioning of an auxiliary clamping, the problem will be mitigated.

Fig. 10 shows a resistive auxiliary clamping network for the new diode clamping inverter. A similar network for the conventional diode clamping inverter is given in Fig. 11. The basic principle has been discussed in [23].

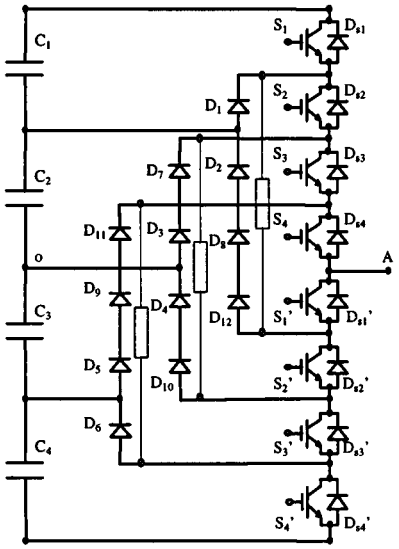


Fig. 11. An auxiliary clamping for the conventional diode clamping inverter. Each auxiliary clamping diode is subject to multiple blocking voltage.

IV. Experimentation Results

A scaled laboratory prototype has been built for verification of the new diode clamping inverter. For the half bridge five-level prototype, four 120 V dc power sources are employed as the dc supplies for the dc link. The series inductor has been added just to make the dc source operational. As the load for the inverter, a 8 mH inductor in series with a 12 Ω resistor are connected between the inverter output and the dc neutral point. Fundamental frequency modulation scheme eliminating the fifth and the seventh harmonics is implemented. For the small power prototype, no auxiliary clamping has been installed.

Fig. 12(a)–(d) shows the experimental output voltage in relation to the blocking voltages across S_4, S_3, S_2 and S_1 respectively, which clearly demonstrate the operation and clamping of the proposed new diode clamping inverter. The nonrigidity of the individual voltage level has been caused by the inductor in series with the corresponding dc supply.

V. Conclusion

From the analysis and experimentation presented above, the following conclusions are obtained regarding the new diode clamping inverter:

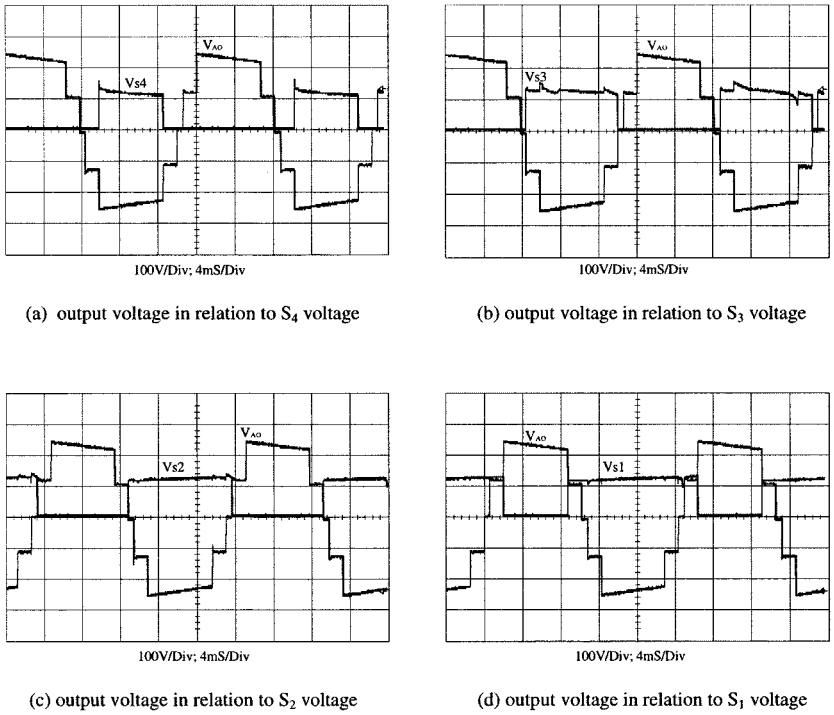


Fig. 12. Experimental output voltage of the new inverter in relation to the blocking voltages across $S_4, S_3, S_2,$ and S_1 respectively. Each main switch sees the nominal blocking voltage.

1) The new diode clamping inverter solves the diodes series problem of the conventional diode clamping inverter. In the new structure, not only the main switches are clamped by the clamping diodes, the clamping diodes are also clamped mutually by themselves. The need for the large RC network dealing with voltage sharing problem among series diodes is removed.

2) The unequal blocking voltage distribution problem resulted from indirect clamping is expected to be mitigated by adding an auxiliary clamping network.

Even though the turn-on snubbing problem and the dc link unbalance problem are not resolved, the new diode clamping inverter represents a relevant improvement over the conventional structure and will facilitate the practical application of the diode clamping multilevel inverter in large power conversion area.

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