ARCPI Resonant Snubber for the Neutral-Point-Clamped Inverter

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***Abstract*—This paper reports a resonant snubber for the neutral-point-clamped (NPC) inverter using the auxiliary resonant commutated pole inverter (ARCPI) technique. The proposal guarantees zero-voltage switching of the main switches and zero-current switching of the auxiliary switches without incurring any voltage or current spikes across or through the main switches and without being subjected to any modulation constraints. The operation principle of the ARCPI NPC inverter is illustrated. A simple method dealing with the static overvoltage problem of the inner switches is described. Commutation durations and current stresses in the basic ARCPI circuit are analyzed. The results enable mathematical understanding and practical designing of the basic ARCPI circuit. In particular, the self-balancing quality and controlling possibility of the dc center potential in the basic ARCPI circuit are investigated. The proposal is verified by a 3-kW half-bridge ARCPI NPC inverter laboratory prototype.**

***Index Terms*—Auxiliary resonant commutated pole inverter, neutral-point-clamped inverter, snubber, soft switching.**

I. Introduction

THE NEUTRAL-POINT-CLAMPED (NPC) inverter [1] has been playing a growing role in the recent decade, especially in traction [2], [3] and power system applications [4], due to the expanded capacity with the existing switches without the problematic series association of switches as well as the reduced output harmonics. To limit the dv/dt and di/dt rates of change when gate-turn-off thyristors (GTO's) are used, different snubber schemes utilizing either *RCD* snubbers [4] or low-loss snubbers [5], [6] have been developed, where the switching frequency is significantly limited due to the enormous snubber loss. Regenerative snubbers avoid the loss at the expense of the considerable hardware complexity [7]–[9], including even baby snubbers for the recovery choppers [10]. Moreover, snubbers either dissipative or regenerative, suffer from such other problems as voltage/current spikes, series inductor loss, as well as the adverse effects from the snubbing diodes, etc.

Several previous publications have resorted to soft-switching techniques for snubbing of the NPC inverter. Besides the early thyristor three-state inverter [11] originated from the modified McMurray two-level inverter, which works actually with zero-current switching, zero-voltage-switching NPC schemes [12], [13] using quasi-resonant dc-link [14] and auxiliary resonant commutated pole inverter (ARCPI) [15]–[17] were also explored. The auxiliary switches in [11] and [13], however, are subject to 2 and 1.5 times the main switches blocking voltage, respectively.

Recognizing that the NPC inverter is always used to advantage in high-power applications, the ARCPI circuit which was deemed the best for high-power use [18], has the most potential in securing an applicable zero-voltage-switched high-power NPC inverter. An uncertainty which remains with the basic ARCPI circuit, however, is the stability of the dc center potential, as mentioned in [19].

It is the objective of this paper to propose an alternative ARCPI NPC inverter. Like the basic ARCPI circuit, the auxiliary switches in the proposal see only one-half of the main switches blocking voltage. Understandings of self-balancing and controlling of the dc center potential in the basic ARCPI circuit are reported.

II. Proposed ARCPI NPC Inverter

A. Commutation Principle

Fig. 1(a) shows the proposed ARCPI NPC inverter. The circuit can actually be decoupled into two ARCPI cells, as shown in Fig. 1(b) and (c). When S_2 is ON and S_4 is OFF, auxiliary switches S_{a1} and S_{a3} assist the commutations between S_1 and S_3 connecting the output to the plus and the neutral rail alternatively and forming the first ARCPI cell, while $V_{cr2} = 0$, $V_{cr4} = V_{\rm dc}$ and $i_{Lr24} = 0$. On the other hand, when S_3 is ON and S_1 is OFF, auxiliary switches S_{a2} and S_{a4} assist the commutations between S_2 and S_4 connecting the output to the neutral and the minus rail alternatively and forming the second ARCPI cell, while $V_{cr3} = 0$, $V_{cr1} = V_{\rm dc}$ and $i_{Lr13} = 0$. To understand the operation of the circuit, commutations in the first ARCPI cell between S_1/D_1 and S_3/D_3 when the load current is negative ($D_1 \leftrightarrow S_3$) will be explained. The following assumptions are made.

- DC capacitor voltage $V_{C11} = V_{C12} = V_{C21} = V_{C22} = V_{\rm dc}/2$.
- Neutral line stray inductance is neglected.
- Clamping resistor R_c is neglected.

Note that, for the load current and each resonant inductor current, a current sensor is installed. Note further that, for each

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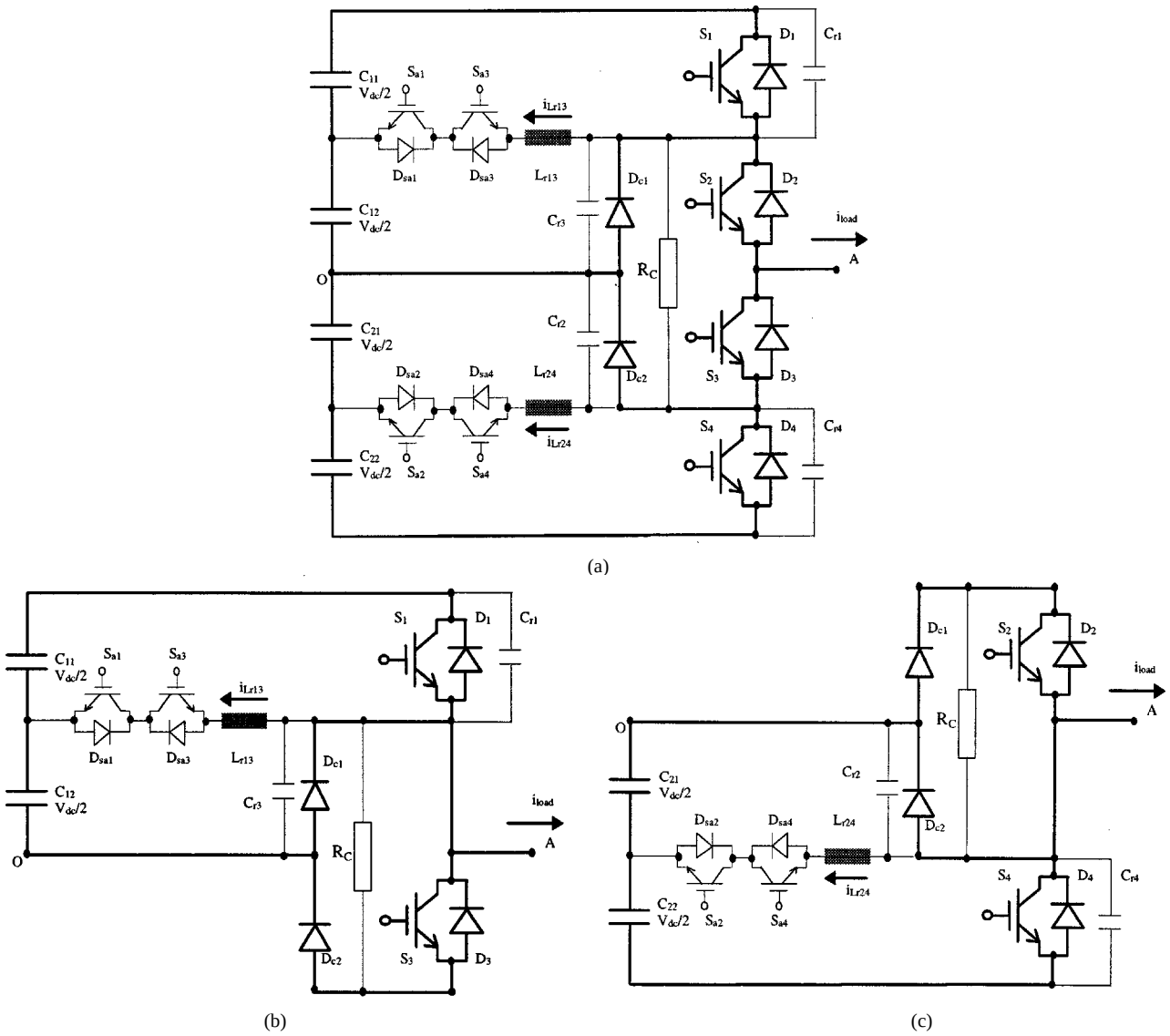


Fig. 1. Configuration of the proposed ARCPI NPC inverter leg. S_{a1}/S_{a3} assist cell S_1/S_3, while S_{a2}/S_{a4} assist cell S_2/S_4, both exactly in the same way as the basic ARCPI circuit. R_c is clamping resistor to prevent overvoltage from happening across either of the inner switches S_2 and S_3. (a) ARCPI NPC inverter configuration. (b) First ARCPI cell: S_2 is ON and S_4 is OFF; $V_{cr2} = 0$ and $V_{cr4} = V_{\rm dc}$. (c) Second ARCPI cell: S_3 is ON and S_1 is OFF; $V_{cr3} = 0$ and $V_{cr1} = V_{\rm dc}$.

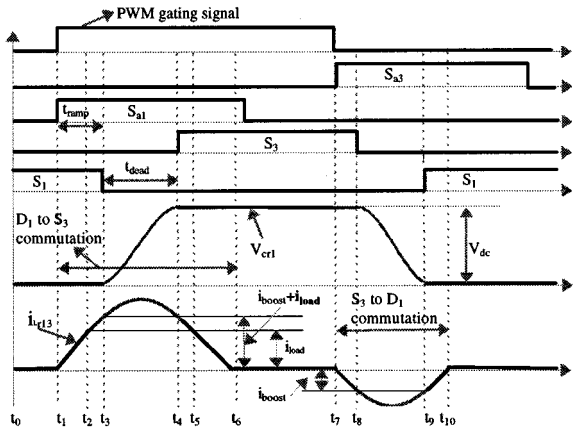


Fig. 2. Predicted waveforms for commutations between S_1/D_1 and S_3/D_3 when the load current is negative ($D_1 \leftrightarrow S_3$). Note that "$i_{\rm boost}$" for switch to diode commutation is equal to the "$i_{\rm boost}$" for diode to switch commutation, and is consistently applied without regard to the level of the load current.

snubbing capacitor, a zero-voltage detector is installed. The predicted commutation waveforms are shown in Fig. 2. The commutation step diagrams are shown in Fig. 3.

Step 1 (t_0–t_1): Circuit steady state. Output is connected to the plus rail by D_2 and D_1.

Step 2 (t_1–t_2): Auxiliary switch S_{a1} is turned on at t_1, causing current decreasing in D_1, current increasing in L_{r13} while current in D_2 keeps.

Step 3 (t_2–t_3): D_1 blocks at t_2 while S_1 begins carrying the increasing difference between the resonant inductor current and the load current.

Step 4 (t_3–t_4): S_1 is turned off at t_3 when the current in S_1 reaches $I_{\rm boost}$, resulting in resonance between L_{r13} and C_{r1}, C_{r3}. C_{r1} is charged while C_{r3} is discharged.

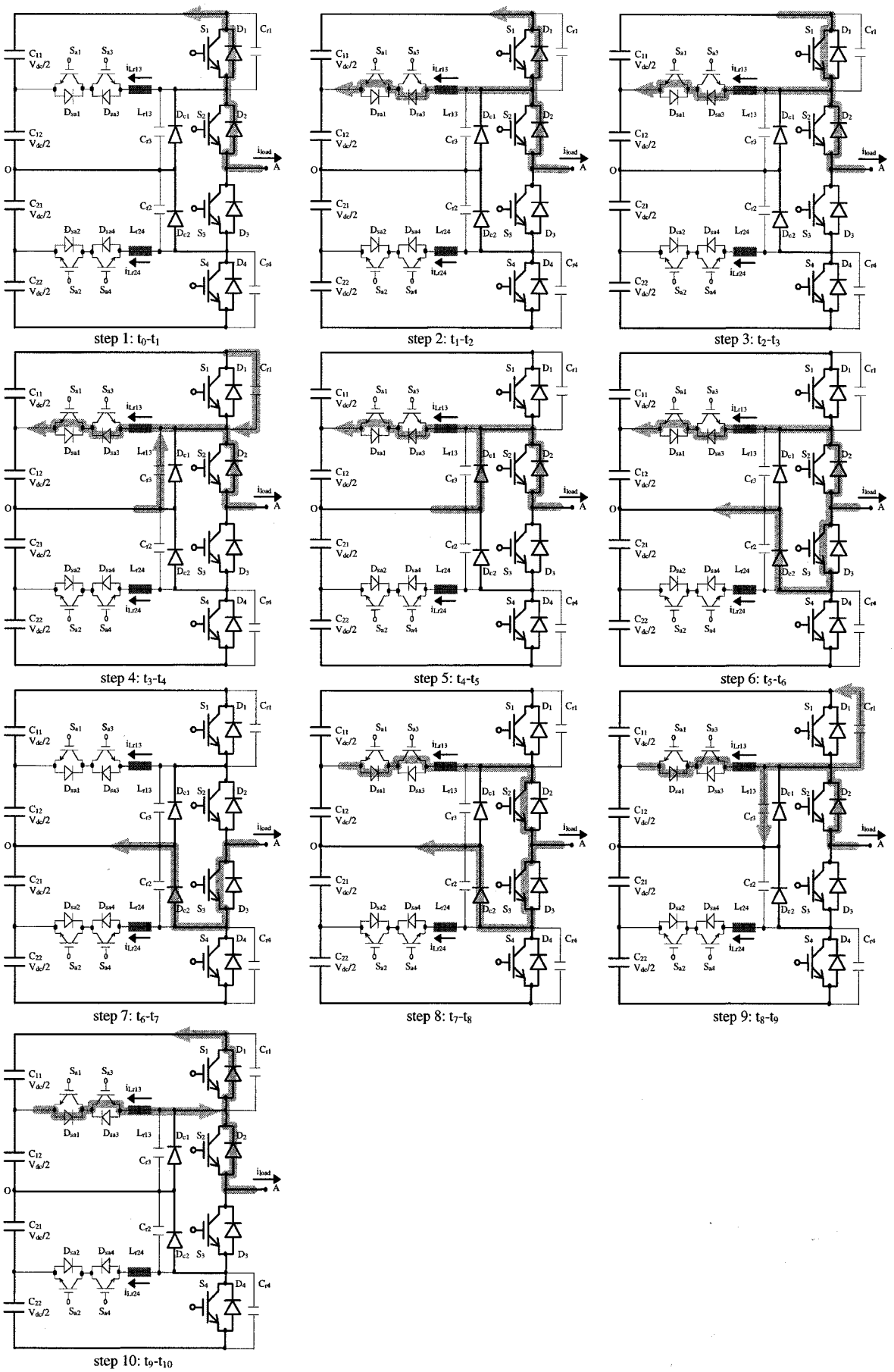


Fig. 3. Step diagram for commutations between D_1 and S_3 in the proposed ARCPI NPC inverter when the load current is negative.

Step 5 (t_4–t_5): Currents changeover from C_{r1} and C_{r3} to D_{c1} at t_4 instantly when voltage across C_{r1} reaches $V_{\rm dc}$. S_3 gating signal is then released by the zero-voltage-detecting circuit installed across C_{r3}.

Step 6 (t_5–t_6): S_3 and D_{c2} start carrying current at t_5 when current in L_{r13} decreases to the load current level.

Step 7 (t_6–t_7): S_3 and D_{c2} carry the full load current at t_6 when L_{r13} current arrives at zero. S_{a1} gating signal can be withdrawn. Circuit reaches steady state. S_3 and D_{c2} connect the output to the neutral rail.

Step 8 (t_7–t_8): S_{a3} is turned on at t_7, increasing the current flowing in S_3 and D_{c2}. L_{r13} current ramps up in the reverse direction.

Step 9 (t_8–t_9): S_3 is turned off at t_8 when the L_{r13} current is promoted to $I_{\rm boost}$, leading to resonance between C_{r3}, C_{r1}, and L_{r13}. C_{r3} is charged and C_{r1} is discharged.

Step 10 (t_9–t_{10}): D_1 starts conducting current at t_9 when C_{r3} voltage reaches $V_{\rm dc}$. S_1 gating signal is then released by the zero-voltage-detecting circuit across C_{r1}. L_{r13} current starts decreasing until extinguishing at t_{10}. S_{a3} gating signal can then be withdrawn. D_2 and D_1 connect the output to the plus rail as shown in Step 1(t_0–t_1).

Commutations between S_1/D_1 and S_3/D_3 when the load current is positive ($S_1 \leftrightarrow D_{c1}$) as well as the commutations between S_2/D_2 and S_4/D_4 when the load current is either positive ($S_2 \leftrightarrow D_4$) or negative ($D_{c2} \leftrightarrow S_4$) can be analogously inferred. Obviously, with the assistance of the auxiliary branches, all the main switches work with zero-voltage turn-on and capacitive turn-off, while all the auxiliary switches work with zero-current turn-off and inductive turn-on. Moreover, all the auxiliary switches block only $V_{\rm dc}/2$, which is one-half of the main switches blocking voltage.

B. Static Overvoltage Limitation for the Inner Switches

Indirect clamping resulting in static overvoltage of inner switches is one of the most serious disadvantages of the diode clamping multilevel inverter [20]. The problem in the NPC inverter case can be clearly observed [5]. Solutions were also pursued [21]–[23], but with limited effectiveness. Inner switches in [23] even suffer from significant turn-on current impulse due to the discharging of the snubbing capacitors through the inner switches without any resistive dampings.

The problem can be effectively and economically resolved by connecting a clamping resistor across the inner switches, as illustrated in Fig. 4(a) and (b). While the value of this resistor can be set as high as possible as long as the corresponding clamping diode (D_{c1}/D_{c2}) can conduct, loss accrued from the clamping resistor is negligible. Note that the solution is theoretically extensible to any level diode clamping multilevel inverter reported in [20], [24], and [25].

Without regard to the clamping resistor R_c, the snubbing capacitor (C_{r3}/C_{r2}) in parallel with the clamping diode (D_{c1}/D_{c2}), as shown in Fig. 2(a), also help to mitigate the overvoltage problem [20]. The reverse-recovery energy accumulated in the neutral line parasitic inductance is snubbed by the snubbing capacitor (C_{r3}/C_{r2}), rather than by the parasitic capacitance of the clamping diode (D_{c1}/D_{c2}) alone in the hard-switching case, allowing mitigated voltage stress across the clamping diode (D_{c1}/D_{c2}) and, hence, mitigated overvoltage across the inner switch (S_2/S_3).

III. Basic ARCPI Circuit

For the analysis of the basic ARCPI circuit, the following assumptions are made.

- Resonant inductance $L_{r13} = L_{r24} = L_r$. Snubbing capacitance $C_{r1} = C_{r2} = C_{r3} = C_{r4} = C_r$. Angle frequency $\omega_o = [1/(2C_rL_r)]^{1/2}$. Resonant impedance $Z_o = [L_r/(2C_r)]^{1/2}$. Switching cycle T.
- Ohmic losses in the resonant loops are neglected.
- Unit current $\overline{i} = iZ_o/V_{\rm dc}$. Unit voltage $\overline{V} = V/V_{\rm dc}$. Unit time $\overline{t} = t\omega_o$.
- $\overline{i}_{\rm boost} = 20\%$ or as specified. $V_{C11} = V_{C12} = V_{C21} = V_{C22} = V_{\rm dc}/2$ or as specified.

A. Commutation Durations and Current Stresses

1) Total Commutation Durations and Duty Cycle Limitation: Total commutation durations decide the auxiliary switch gating signal width. They impose yet duty cycle limitation on modulation leading to reduced dc-link voltage utilization. The next commutation can start only after the conclusion of the previous commutation. Expressions for total commutation durations corresponding to diode to switch (t_{ds}) and switch to diode (t_{sd}) commutation are given in (1) and (2), respectively,

$$\overline{t_{ds}} = 2a\cos\frac{\overline{i_{\rm boost}}}{\sqrt{\frac{1}{4}+\overline{i_{\rm boost}}^2}} + 4[\overline{i_{\rm load}} + \overline{i_{\rm boost}}] \qquad (1)$$

$$\overline{t_{sd}} = 2a\cos\frac{\overline{i_{\rm boost}} + \overline{i_{\rm load}}}{\sqrt{\frac{1}{4}+[\overline{i_{\rm boost}} + \overline{i_{\rm load}}]^2}} + 4\overline{i_{\rm boost}}. \qquad (2)$$

Variations of the total commutation durations with load current are shown in Fig. 5. Apparently, for diode to switch commutation, the total commutation duration increases with load current. For switch to diode commutation, however, it decreases with load current. The auxiliary switch gating signal width should be set covering the maximum commutation duration for diode to switch commutation at the peak load current level and remains constant throughout the low-frequency cycle.

2) Resonant Inductor Peak Currents: Resonant inductor peak currents concern the rating of the auxiliary switch and the designing of the resonant inductor. Expressions for resonant inductor peak currents corresponding to diode to switch

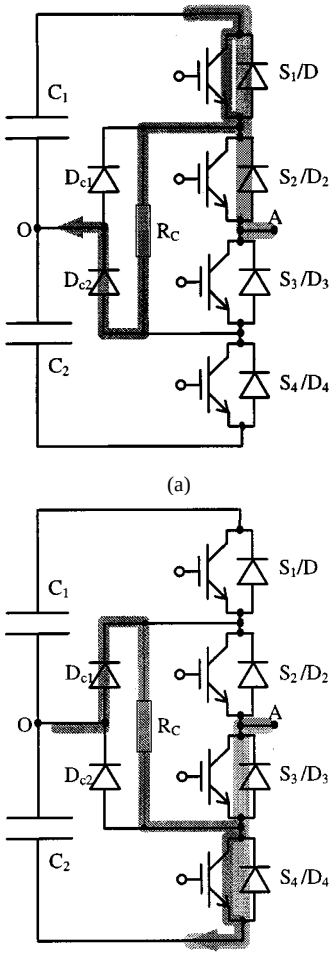


Fig. 4. Voltage limitation mechanism for the inner switches S_3 and S_2 by the clamping resistor R_c. (a) For S_3: when S_3 and S_4 are OFF and S_1 and S_2 are ON, D_{C2} will conduct due to the clamping resistor R_c, making S_4 voltage clamped to C_2 and S_3 voltage clamped to C_1. (b) For S_2: when S_1 and S_2 are OFF and S_3 and S_4 are ON, D_{C1} will conduct due to the clamping resistor R_c, making S_1 voltage clamped to C_1 and S_2 voltage clamped to C_2.

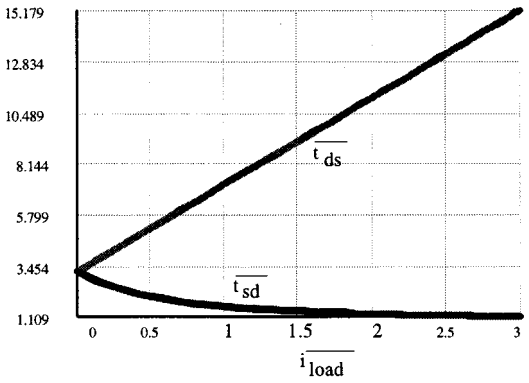


Fig. 5. Total commutation durations for diode to switch commutation (t_{ds}: t_6–t_1) and switch to diode commutation (t_{sd}: t_{10}–t_7) versus load current.

commutation and switch to diode commutation solved over the switch cycle are given in (3) and (4), respectively

$$\overline{i_{Lrp1}} = \overline{i_{\text{load}}} + \sqrt{\frac{1}{4} + \overline{i_{\text{boost}}}^2} \tag{3}$$

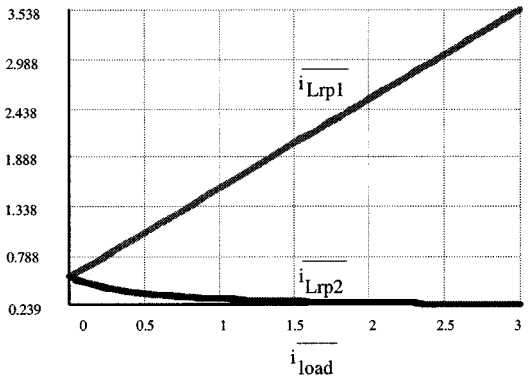


Fig. 6. Resonant inductor peak currents solved over the switching cycle for diode to switch commutation ($\bar{i}_{Lrp1}$) and switch to diode commutation ($\bar{i}_{Lrp2}$) versus load current.

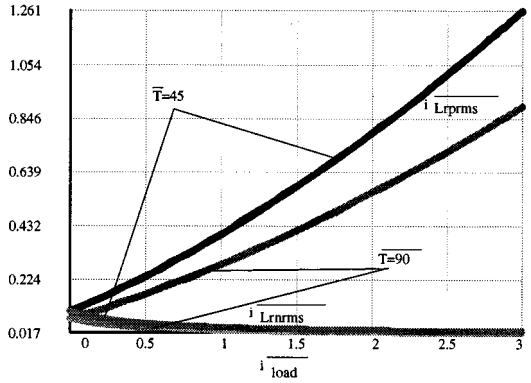


Fig. 7. Resonant inductor rms currents solved over the switching cycle for diode to switch commutation ($\bar{i}_{Lrp\,\text{rms}}$) and switch to diode commutation ($\bar{i}_{Lrn\,\text{rms}}$) versus load current and switching cycle.

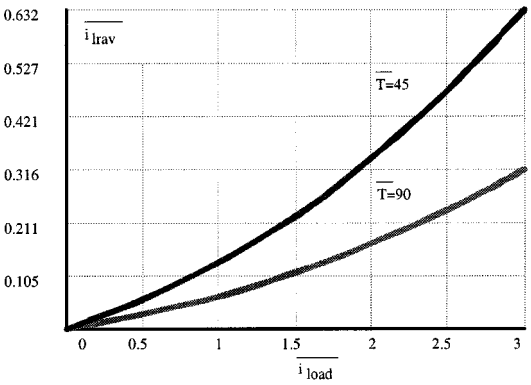


Fig. 8. Resonant inductor average current $\bar{i}_{Lrav}$ solved over the switching cycle flowing out of the center potential corresponding to positive load current versus load current and switching cycle.

$$\overline{i_{Lrp2}} = -\overline{i_{\text{load}}} + \sqrt{\frac{1}{4} + (\overline{i_{\text{boost}}} + \overline{i_{\text{load}}})^2}. \tag{4}$$

Variations of the peak currents with load current are shown in Fig. 6(a) and (b). Obviously, for diode to switch commutation, the peak current increases with load current. For switch to diode commutation, the peak current decreases with load current.

3) Resonant Inductor RMS Currents: Resonant inductor rms currents concern the rating of the auxiliary switch and the

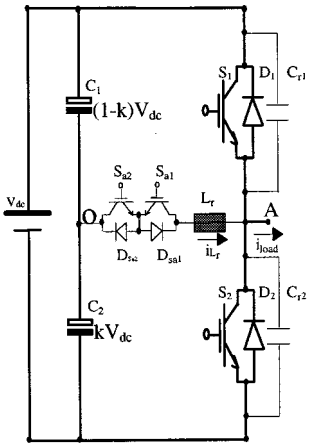
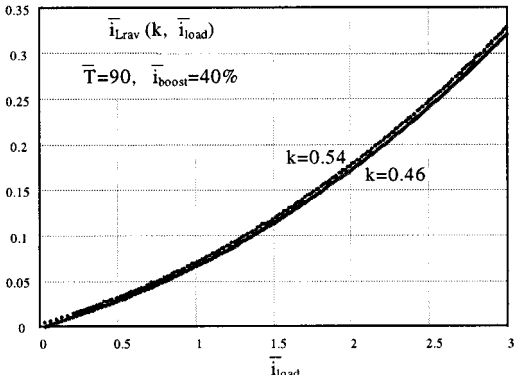
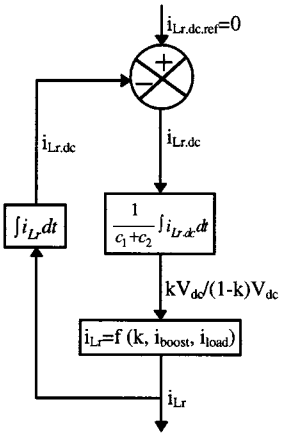


Fig. 9. Basic ARCPI circuit structure with dc voltage distribution factor of k.



(a)



(b)

Fig. 10. (a) Resonant inductor average current $\bar{i}_{Lrav}$ solved over the switching cycle flowing out of the dc center potential corresponding to positive load current versus load current and dc-link voltage distribution factor k. (b) Neutral line current feedback loop and self-balancing of the dc center potential in the basic ARCPI circuit.

designing of the resonant inductor. Auxiliary switch carries the diode to switch commutation current for one load current direction and the switch to diode commutation current for the other load current direction. For the two currents, the

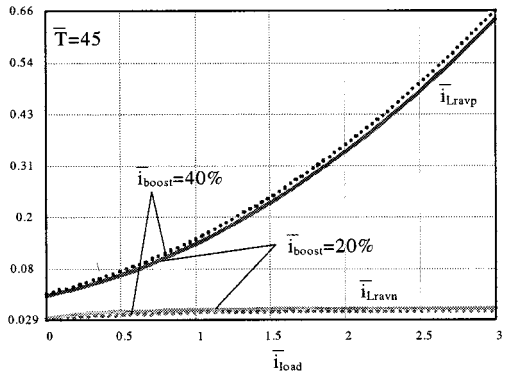


Fig. 11. Resonant inductor average current averaged over the switching cycle versus load current, switching cycle, and $\bar{i}_{\rm boost}$ for diode to switch commutation ($\bar{i}_{Lravp}$) and switch to diode commutation ($\bar{i}_{Lravn}$).

rms expressions solved over switching cycle are $\bar{i}_{Lrp\,\rm rms}$ and $\bar{i}_{Lrn\,\rm rms}$, respectively, as given in (5) and (6)

$$\overline{i_{Lrp\,\rm rms}} = \sqrt{\frac{2}{\overline{T}}\int_0^{2(\overline{i_{\rm load}}+\overline{i_{\rm boost}})} \frac{1}{4}\bar{t}^2\,d\bar{t} + \frac{1}{\overline{T}}\int_0^{2a\cos\left(\overline{i_{\rm boost}}\Big/\sqrt{1/4+\overline{i_{boost}}^2}\right)} \cdot\left(\overline{i_{\rm load}}+\frac{1}{2}\sin\bar{t}+\overline{i_{\rm boost}}\cos\bar{t}\right)^2 d\bar{t}} \tag{5}$$

$$\overline{i_{Lrn\,\rm rms}} = \sqrt{\frac{2}{\overline{T}}\int_0^{2\overline{i_{\rm boost}}} \frac{1}{4}\bar{t}^2\,d\bar{t} + \frac{1}{\overline{T}}\int_0^{2a\cos\left((\overline{i_{\rm boost}}+\overline{i_{\rm load}})\Big/\sqrt{1/4+(\overline{i_{\rm boost}}+\overline{i_{\rm load}})^2}\right)} \cdot\left(\overline{i_{\rm load}}-\frac{1}{2}\sin\bar{t}-(\overline{i_{\rm load}}+\overline{i_{\rm boost}})\cos\bar{t}\right)^2 d\bar{t}} \tag{6}$$

Variations of the two currents with load current and switching cycle are shown in Fig. 7(a) and (b). Analogous to the previous cases, the resonant inductor rms current corresponding to diode to switch commutation increases with load current, but decreases with switching cycle. In the meanwhile, the resonant inductor rms current corresponding to switch to diode commutation decreases with both load current and switching cycle.

This result justifies the gating plan in this paper to impose the "boost" current consistently for switch to diode commutation, no matter what is the load current level. The additional loss accrued is negligible, while it brings considerable control simplification.

4) Resonant Inductor Average Current: Resonant inductor average current allows for understanding of the static fluctuation of the dc-link center potential. Expression for the resonant inductor average current solved over the switching cycle flowing

out of the dc center potential corresponding to positive load current is given in (7)

$$\begin{aligned}\overline{i_{Lrav}} = &\frac{2}{\overline{T}}\int_0^{2(\overline{i_{\rm load}}+\overline{i_{\rm boost}})}\frac{1}{2}\,\bar{t}\,d\bar{t}\\ &+\frac{1}{\overline{T}}\int_0^{2a\cos\left(\overline{i_{\rm boost}}\Big/\sqrt{1/4+\overline{i_{\rm boost}}^2}\right)}\\ &\cdot\left(\overline{i_{\rm load}}+\frac{1}{2}\sin\bar{t}+\overline{i_{\rm boost}}\cos\bar{t}\right)d\bar{t}\\ &+\frac{2}{\overline{T}}\int_0^{2\overline{i_{\rm boost}}}\frac{1}{2}\,\bar{t}\,d\bar{t}\\ &+\frac{1}{\overline{T}}\int_0^{2a\cos\left((\overline{i_{\rm boost}}+\overline{i_{\rm load}})\Big/\sqrt{1/4+(\overline{i_{\rm boost}}+\overline{i_{\rm load}})^2}\right)}\\ &\cdot\left(\overline{i_{\rm load}}-\frac{1}{2}\sin\bar{t}-(\overline{i_{\rm load}}+\overline{i_{\rm boost}})\cos\bar{t}\right)d\bar{t}.\end{aligned}\tag{7}$$

Variations of this current with load current and switching cycle are shown in Fig. 8. Evidently, the current increases with load current, but decreases with switching cycle. Note that the resonant inductor average current flowing into the dc center potential corresponding to negative load current is equal in value at a given load current level.

B. Current Feedback Loop of the Neutral Line Current and Self Balancing of the DC Center Potential

Referring to Fig. 9, assuming that, in the basic ARCPI circuit, the dc-link voltage distribution factor is k, capacitor C_2 voltage is $kV_{\rm dc}$, while capacitor C_1 voltage is $(1-k)\,V_{\rm dc}$. The resonant inductor average current solved over the switching cycle flowing out of the dc center potential corresponding to positive load current is then given by (8), shown at the bottom of the page. Note that, for this expression, it has been assumed that the circuit is always in zero-voltage-switching operation in spite of the dc center potential fluctuation.

Variations of this current with load current and the dc voltage distribution factor k are shown in Fig. 10(a). Evidently, the current increases with the dc-link voltage distribution factor k. In the same sense, the resonant inductor average current solved over the switching cycle flowing into the dc center potential corresponding to negative load current will decrease with the dc-link voltage distribution factor k.

Consequently, for disturbance leading to increase of the capacitor C_2 voltage, the average resonant inductor current flowing out of the dc center potential will increase making capacitor C_2 more discharged and capacitor C_1 more charged, while the current flowing into the dc center potential will decrease making capacitor C_2 less charged and capacitor C_1 less discharged. The implication of this regulation is the negative feedback in the neutral line current loop and, in turn, self-balancing of the dc center potential, as illustrated in Fig. 10(b).

Under symmetrical operation conditions, the neutral line current will be averaged to zero when the dc-link voltage distribution factor is 0.5. It is mainly in this sense that the dc center potential is deemed self-balancing.

C. Controlling of the DC-Link Center Potential

Referring again to Fig. 10, the neutral line current feedback loop does not guarantee $k = 0.5$. When asymmetrical operation conditions arise, zero neutral line current will correspond to dc-link voltage distribution factor different from 0.5. Depending on the extent of the asymmetry, the dc center potential may drift beyond the range where zero-voltage switching can still be secured. An active voltage feedback loop for the dc center potential is, hence, needed in this case.

To look at the possibility of such controlling, expressions for the resonant inductor average currents averaged over the

$$\begin{aligned}\overline{i_{Lrav}} = &\frac{1}{\overline{T}}\int_0^{((\overline{i_{\rm load}}+\overline{i_{\rm boost}})/k)}k\bar{t}\,d\bar{t}+\frac{1}{\overline{T}}\int_0^{\pi-a\cos\left(\left((1-k)\right)\Big/\sqrt{k^2+\overline{i_{\rm boost}}^2}\right)-a\cos\left(k\Big/\sqrt{k^2+\overline{i_{\rm boost}}^2}\right)}\\ &\cdot(\overline{i_{\rm load}}+k\sin(\bar{t})+\overline{i_{\rm boost}}\cos(\bar{t}))\,d\bar{t}+\frac{1}{\overline{T}}\int_0^{\left(\left(\sqrt{k^2+\overline{i_{\rm boost}}^2+(1-k)^2}+\overline{i_{\rm load}}\right)\Big/(1-k)\right)}\\ &\cdot\left(\sqrt{k^2+\overline{i_{\rm boost}}^2-(1-k)^2}+\overline{i_{\rm load}}-(1-k)\bar{t}\right)d\bar{t}+\frac{1}{\overline{T}}\int_0^{(\overline{i_{\rm boost}}/(1-k))}(k-1)\bar{t}\,d\bar{t}\\ &+\frac{1}{\overline{T}}\int_0^{\pi-a\cos\left(k\Big/\sqrt{(1-k)^2+(\overline{i_{\rm load}}+\overline{i_{\rm boost}})^2}\right)-a\cos\left((1-k)\Big/\sqrt{(1-k)^2+(\overline{i_{\rm load}}+\overline{i_{\rm boost}})^2}\right)}\\ &\cdot(\overline{i_{\rm load}}+(k-1)\sin\bar{t}-(\overline{i_{\rm load}}+\overline{i_{\rm boost}})\cos\bar{t})\,d\bar{t}+\frac{1}{\overline{T}}\int_0^{\left(\left(\sqrt{(1-k)^2+(\overline{i_{\rm load}}+\overline{i_{\rm boost}})^2-k^2}-\overline{i_{\rm load}}\right)\Big/k\right)}\\ &\cdot\left(-\sqrt{(1-k)^2-k^2+(\overline{i_{\rm load}}+\overline{i_{\rm boost}})^2}+\overline{i_{\rm load}}+k\bar{t}\right)d\bar{t}\end{aligned}\tag{8}$$

switching cycle contributed from diode to switch and switch to diode commutation are given by (9) and (10), respectively

$$\overline{i_{Lravp}} = \frac{2}{\overline{T}} \int_0^{2(\overline{i_{\rm load}}+\overline{i_{\rm boost}})} \frac{1}{2}\,\bar{t}\,d\bar{t} + \frac{1}{\overline{T}} \int_0^{2a\,\cos\left(\overline{i_{\rm boost}}\Big/\sqrt{1/4+\overline{i_{\rm boost}}^2}\right)} \cdot \left(\overline{i_{\rm load}} + \frac{1}{2}\,\sin\,\bar{t} + \overline{i_{\rm boost}}\,\cos\,\bar{t}\right) d\bar{t} \quad (9)$$

$$\overline{i_{Lravn}} = \frac{2}{\overline{T}} \int_0^{2\overline{i_{\rm boost}}} \frac{1}{2}\,\bar{t}\,d\bar{t} + \frac{1}{\overline{T}} \cdot \int_0^{2a\,\cos\left((\overline{i_{\rm boost}}+\overline{i_{\rm load}})\Big/\sqrt{1/4+(\overline{i_{\rm boost}}+\overline{i_{\rm load}})^2}\right)} \cdot \left(\overline{i_{\rm load}} - \frac{1}{2}\,\sin\,\bar{t} - (\overline{i_{\rm load}} + \overline{i_{\rm boost}})\,\cos\,\bar{t}\right) d\bar{t}. \quad (10)$$

Variations of the resonant inductor average currents with load current, switching cycle, and $i_{\rm boost}$ are shown in Fig. 11. From this figure, the resonant inductor average current contributed from diode to switch commutation increases with $i_{\rm boost}$, while the resonant inductor average current contributed from switch to diode commutation decreases with $i_{\rm boost}$. Such relationship creates an opportunity for controlling of the dc center potential.

If k is detected to be higher than 0.5, then when the load current direction is positive, $i_{\rm boost}$ will be increased by a controller for both diode to switch and switch to diode commutation. The resonant inductor average current flowing out of the center potential will get increased allowing the dc-link capacitor C_2 to be more discharged and the dc-link capacitor C_1 to be more charged. On the other hand, $i_{\rm boost}$ should be kept when the load current direction is negative.

If k is detected to be lower than 0.5, then when the load current direction is negative, $i_{\rm boost}$ will be increased by a controller for both diode to switch and switch to diode commutation. The resonant inductor average current flowing into the center potential will get increased allowing the dc-link capacitor C_2 to be more charged and the dc-link capacitor C_1 to be more discharged. Again, $i_{\rm boost}$ should be kept when the load current is positive in this case. Again, $i_{\rm boost}$ should be kept when the load current direction is positive.

The overall control concept combining the intrinsic neutral line current feedback loop and the extrinsic dc center potential voltage feedback loop is shown in Fig. 12.

Note that, for the half-bridge ARCPI case under consideration, while charge balance (amperes $\times$seconds) of the dc-link capacitors will be lost during the fundamental frequency cycle leading to center potential drift when asymmetrical operation conditions arise, flux balance (volts $\times$seconds) of the resonant inductor will be automatically maintained for each commutation, no matter what the operation conditions are, as long as the resonant inductor current can return to zero during the commutation.

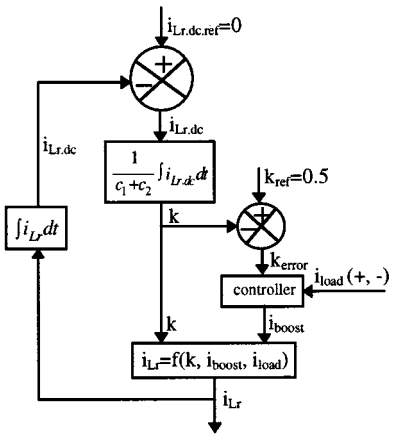


Fig. 12. DC center potential control system including the intrinsic neutral line current feedback loop and the extrinsic dc center potential voltage feedback loop.

D. Resonant Circuit Designing of the Basic ARCPI Circuit

For designing the resonant circuit, current valve $i_{\rm boost}$ should be set first dependent on the actual resonant loop ohmic loss to ensure the pole voltage swinging to the rail level during the commutation [16]. A margin must also be considered for $i_{\rm boost}$ to ensure zero-voltage switching under dc center potential fluctuation to some reasonable extent. Snubbing capacitance should be set as per the allowable switch turn-off loss [26]. Auxiliary switch gating signal width and pulsewidth modulation (PWM) signal duty cycle limitation should be designed according to the maximum commutation duration given in Fig. 5. Resonant inductance can be designed according to Fig. 7 with information regarding the accepted resonant inductor rms current and the expected switching frequency. Rating of the auxiliary switch can be selected according to the peak current and the rms current information given in Figs. 6 and 7.

Note that the resonant inductor average current is not in linear relationship with the load current according to Fig. 8. The net neutral line current average value in a three-phase ARCPI system will not be zero for each switching cycle and will see a third-order harmonic current. The expression for this current can be deducted analogously and will help the designing of the dc-link capacitors.

IV. Experimentation Results

Specifications of the 3-kW half-bridge ARCPI NPC inverter prototype are given in Table I. Considering that the switching frequency taken in today's high-power NPC inverters is limited to some hundreds of hertz for GTO's [7] and to around 1000 hertz for insulated gate bipolar transistors (IGBT's) [27], [28] or integrated gate commutated thyristors (IGCT's) [29], the switching frequency chosen for this prototype is 6.5 kHz.

The resonant circuit parameters are $L_{r13} = L_{r24} = 12\ \mu$H and $C_{r1} = C_{r2} = C_{r3} = C_{r4} = 0.1\ \mu$F. Auxiliary switch gating signal width is 14.4 μs. Minimum and maximum PWM signal widths are 16.8 and 136.8 μs, respectively. In addition, $i_{\rm boost} = 5$ A.

Four 3300-μF/350-V capacitors are used at the dc link. Ripple of each dc-link center potential is, therefore, minimized

TABLE I
SPECIFICATIONS OF THE HALF-BRIDGE ARCPI NPC INVERTER PROTOTYPE

DC input voltage	V_{dc}= 600V	Output voltage	$V_{o.rms}$= 122V	Modulation index	M= 0. 62
Output power	P_o= 3kW	Load current	$I_{o.rms}$= 25A	Switching frequency	f_c= 6.5kHz

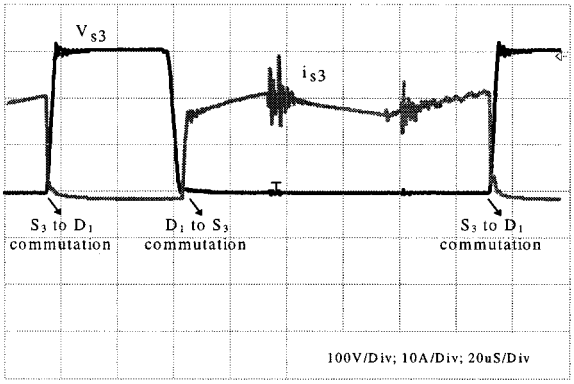


Fig. 13. Experimental voltage and current waveforms of the inner main switch S_3 during D_1 to S_3 and S_3 to D_1 commutations. Main switches work with capacitive turn-off and zero-voltage turn-on. Besides, static overvoltage problem of the inner switches has been resolved by the clamping resistor R_c.

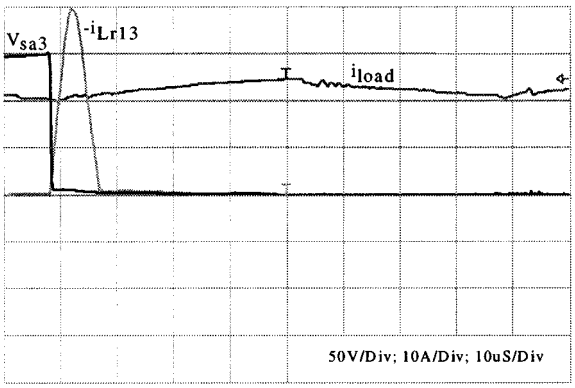


Fig. 14. Experimental voltage and current waveforms of the auxiliary switch S_{a3} during D_{c1} to S_1 commutation in relation to the load current. Auxiliary switches work with inductive turn-on and zero-current turn-off. Besides, the auxiliary switches block only half of the main switches blocking voltage.

TABLE II
LOSS COMPARISON OF THE 3-kW HALF-BRIDGE NPC INVERTER PROTOTYPE

load current in RMS (A)	measured loss at soft switching (W)	predicted loss at soft switching (W)	measured loss at hard switching (W)
5	52.5	61.1	101.2
10	67.2	73,9	121.5
15	93.1	98.1	170.5
20	115.6	121.6	200.1
25	138.5	142.6	251.1

due to the use of the large capacitance. A second-order LC filter with $L_f = 1.5$ mH and $C_f = 14$ μF is connected at the prototype output. A 5-Ω resistor is used as the load. Main switches S_1–S_4 and auxiliary switches S_{a1}–S_{a4} used are SKM50GB123D (1200 V/50 A), and clamping diodes D_{c1}–D_{c2} used are HFA30T60C (600 V/30 A). A resistor of 6.8 kΩ/25 W is used as the clamping resistor R_c.

Note that, for this prototype, no controlling over the two dc center potentials has been taken. The two potentials are self-balancing due to the two neutral line current feedback loops in the two ARCPI cells, as discussed in Section III-B. No considerable unbalance has been witnessed in the prototype. This result, however, is not necessarily extensible to practical high-power inverters where major asymmetrical operation conditions may arise.

The commutation waveforms of the main switch S_3 and the auxiliary switch S_{a3} are shown in Figs. 13 and 14, respectively. From Fig. 13, obviously, the voltage and current spikes arising during the commutations of the main switch S_3 are negligible in comparison to a conventional snubber case [5]–[7]. However, as an inner main switch, S_3 is also involved in the commutations of its neighboring devices ($D_{c2} \leftrightarrow S_4$) during its ON state and experiences current spikes, as can be observed in Fig. 13, the minimization of which requires fine layout designing of the NPC inverter hardware. In Fig. 14, with a load current of 20.5 A, the measured commutation duration is 8.55 μs and the measured resonant inductor peak current is 40 A, corresponding to the predicted commutation duration of 8.21 μs according to Fig. 5 and the predicted resonant inductor peak current of 40.8 A according to Fig. 6.

Measured conversion losses of the prototype together with the predicted conversion loss are given in Table II. Also shown in the table is the conversion loss in the hard-switching case of the same prototype. Device models discussed in [30] have been taken for the prediction. Note that controlling and gating power are supplied by an additional power source.

V. CONCLUSIONS

The following conclusions are obtained from the analysis and experimentation reported above.

1) The proposed ARCPI resonant snubber for the NPC inverter guarantees the zero-voltage switching of the main switches, without incurring any voltage/current spikes and without being subjected to any modulation constraints.
2) The small rating auxiliary switches in the proposal work with zero-current switching. Like the basic ARCPI circuit, the auxiliary switches block only one-half of the main switches blocking voltage.
3) Due to the installation of the clamping resistor R_c, the static overvoltage problem of the inner switches in the NPC inverter is resolved successfully.
4) Due to the neutral line current feedback loop, the dc center potential in the basic ARCPI circuit is self-balancing to one-half of the dc-link voltage under symmetrical operation conditions. Theoretically, under asymmetrical operation conditions, dc center potential balancing can be achieved by increasing the "boost" current according to the direction of the dc center potential drift, as well as the

direction of the load current. This concept needs yet to be implemented.

5) The proposed ARCPI NPC inverter can be utilized to advantage in advanced high-power applications in which required performance criteria such as high switching frequency, wide control bandwidth, and low dV/dt rate of change, etc., cannot be achieved otherwise.

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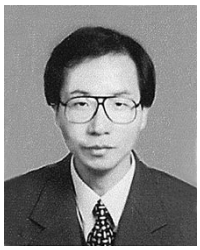

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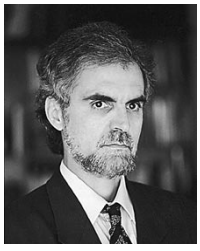

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