Analysis, Designing, and Experimentation of a Transformer-Assisted PWM Zero-Voltage Switching Pole Inverter

Xiaoming Yuan, *Member, IEEE,* and Ivo Barbi, *Senior Member, IEEE*

Abstract—This paper proposes a transformer-assisted pulsewidth modulation (PWM) zero-voltage switching pole inverter. As the auxiliary-resonant-commutated pole inverter (ARCPI), the proposal guarantees zero-voltage switching of the main switch and zero-current switching of the auxiliary switch, with a small power auxiliary circuit and full PWM capability. In particular, problems outstanding with the ARCPI such as control complexity, auxiliary switch protection, and center-tap potential variation, etc., are solved in the proposal. The commutation process is discussed step by step in the paper. A detailed analysis for the auxiliary circuit with regard to commutation duration/duty-cycle limitation, auxiliary switch peak current/rms current, resonant capacitor rms current, as well as pole output voltage loss are presented afterwards. A designing methodology for the auxiliary circuit is recommended based on the analysis. The proposal is experimentally verified with a 4.25-kW half-bridge inverter prototype.

Index Terms—Auxiliary resonant-commutated pole inverter (ARCPI), zero-voltage switching.

I. INTRODUCTION

TODAY'S high-power inverters with either hard switching insulated gate bipolar transistors (IGBT's) or snubbed gate turn-off thyristors (GTO's) are severely constrained in switching frequency limited to a few kilohertz (IGBT) or even a few hundreds hertz (GTO), which fall far behind the needs for such advanced applications as active power filters or high-speed drives, etc. High switching frequency allowing for reasonable control bandwidth is necessarily required to eliminate harmonics up to certain order according to the relevant international standards in the case of active filters, or to offer satisfactory total harmonic distortion factor at certain machine speed to avoid excessive torque ripple or harmonic loss in the case of high-speed drives. Low switching frequency problem can be most promisingly resolved by resonant techniques as has been witnessed in low-power dc/dc converters [1], [2]. Among the varied resonant concepts deemed eligible for the high-power inverter, the auxiliary-resonant-commutated pole inverter (ARCPI) [3]–[5], as shown in Fig. 1, has been mostly favored due to its small rating auxiliary circuit and full

pulsewidth modulation (PWM) operation capability. However, the ARCPI suffers from the following problems.

a) The need for advance triggering of the auxiliary switch necessitates additional measuring and timing with highly demanding resolution [6], which reduces the overall system reliability [7]. Bus inductivity and freewheeling diode reverse recovery current cannot be counted on even though they contribute to boost the resonance toward zero-voltage switching [5], [7]. Without advance triggering, zero-voltage switching will be lost and extra loss will be incurred [8].

b) Measures taken to protect the auxiliary devices against overvoltage due to the reverse recovery energy stored in the resonant inductance result in extra loss and circuit complexity [9], [10].

c) Possible potential variation of the dc link capacitor center tap reduces further the system reliability—this is true especially when a half-bridge inverter feeding a heavy low-frequency load [11]. For a single- or three-phase system where the net current flowing into the center tap during switching cycle may add to zero in theory [5], the stabilization of the center-tap potential may be lost when asymmetrical operation conditions arise between the plus and minus semicycle of the load current in each phase.

Reference [12] solves problem a) by triggering the corresponding auxiliary switch with constant advance set as per the peak load current. Apparently, the main switch to be turned-off will be overboosted for commutations at nonpeak load current levels. Significant loss penalty arises. Also, with constant triggering advance, [13] inserts a current feedback magnetic amplifier to create an initial blocking interval reversely proportional to the load current. With a well-designed magnetic core, a load proportional triggering advance will be obtained. In addition, an alternative solution to problem a) was proposed in [3] and more recently in [14], where the need for advance triggering was removed due to the raised forcing voltage source for the resonance. Complicated battery imbalance compensation circuit must be employed. For all the three proposals, problems b) and c) are left not cared for.

On the other hand, [15] uses a bridge configuration for the auxiliary circuit and offers an encouraging solution to problems b) and c). However, problem a) remains with the circuit. In a quasi-resonant dc link inverter employing the similar configuration, problem a) was addressed [16]. In both cases, magnetization of the autotransformer in the circuit cannot be reset following each commutation, due to the freewheeling
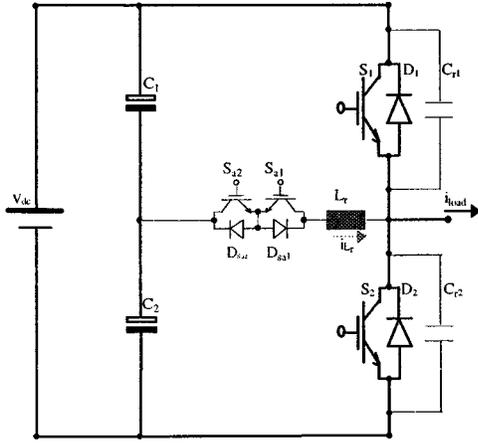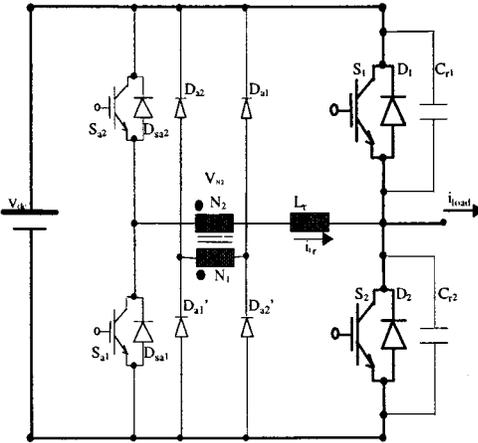
Fig. 1.   Configuration of the ARCPI.

Fig. 2.   Configuration of the transformer-assisted PWM zero-voltage switching pole ($k = N_2/N_1 < 1/2$).

paths existing between the auxiliary devices and the main devices through both windings of the autotransformer [17].

A transformer-assisted PWM zero-voltage switching pole inverter will be studied in this paper. The circuit proposed works free of the three problems mentioned.

II. COMMUTATION PRINCIPLE OF THE TRANSFORMER-ASSISTED PWM ZERO-VOLTAGE SWITCHING POLE INVERTER

The proposed circuit of this paper keeps the bridge configuration in [15] for the auxiliary circuit while a transformer is introduced replacing the autotransformer, as shown in Fig. 2. By setting the transformer ratio ($k = N_2/N_1$) to less than 1/2 as per the resonance loop losses, problem a) is also solved due to the increased forcing voltage source ($>1/2V_{dc}$) for the resonance, similar to the case in [14]. The auxiliary switch can now be turned on simultaneously as the corresponding main switch is turned off, for either diode-to-switch commutation or the reverse. In the meanwhile, as has been the case of ARCPI [11], turn-on signal for the opposite main switch can be released once a zero voltage is detected across it. Transformer magnetization now returns to zero after each commutation.

Refer to Fig. 3 for the commutation step diagrams, and Fig. 4 for the predicted relevant commutation waveforms, the commutation procedure of the proposed circuit during a whole switching cycle under positive load current is described as follows.

Step 1
(t_o–t_1):)   Circuit steady state. Freewheeling diode D_2 carries the load current.

Step 2
(t_1–t_2):) S_2 is turned off and S_{a2} is turned on in the same instant at t_1, leading to conduction of D_{a2} and D'_{a2}. N_2 sees a voltage of kV_{dc} and an enforcing voltage source of $(1 - k)V_{dc}$ is therefore established. Current in D_2 starts decreasing and in L_r increasing.

Step 3
(t_2–t_3):) i_{Lr} rises to the load current level at t_2 leading to blocking of D_2. Resonance among L_r, C_{r2}, and C_{r1} is initiated and forced by $(1 - k)V_{dc}$. C_{r2} is charged while C_{r1} discharged. Recovery current of D_2 enhances the charging current and therefore facilitates the commutation process.

Step 4
(t_3–t_4):) ν_{Cr2} rises to V_{dc} at t_3 leading to conduction of D_1 and releasing of the turn-on signal for S_1. Instantaneous current transfer from C_{r2} and C_{r1} to D_1 will cause oscillation depending on the current loop parasitics and the forward recovery characteristics of D_1. S_1 is turned on at zero voltage.

Step 5
(t_4–t_5):) i_{Lr} falls linearly to load current at t_4 due to the N_2 voltage of kV_{dc} applied across the resonant inductor. D_1 then stops conduction and current through S_1 starts rising linearly.

Step 6
(t_5–t_7):) i_{Lr} extinguishes at t_5 allowing for withdraw of the gating signal for S_{a2} at t_6. S_{a2} is turned off at zero current. S_1 carries the full load current and the circuit reaches another steady state.

Step 7
(t_7–t_8):) S_1 is turned off and S_{a1} is turned on at t_7, which initiates a resonance between L_r and C_{r1}, C_{r2}. N_2 sees a voltage of kV_{dc} due to the conduction of D_{a1} and D'_{a1}. Again, the resonance is forced by a voltage source of $(1 - k)V_{dc}$. C_{r1} is charged and C_{r2} is discharged.

Step 8
(t_8–t_9):) ν_{Cr1} rises to V_{dc} at t_8 leading to conduction of D_2 and releasing of the S_2 turn-on signal. S_2 is then turned on at zero voltage. Also, instantaneous current transition from C_{r1} and C_{r2} to D_2 will cause oscillation due to D_2 diode forward recovery and circuit parasitics.

Step 9
(t_9–t_{10}):) i_{Lr} falls linearly and reaches zero at t_9, due to the reflected voltage of kV_{dc} on N_2, allowing for withdraw of the gating signal for S_{a1} at t_{10}. S_{a1} is turned off at zero current.
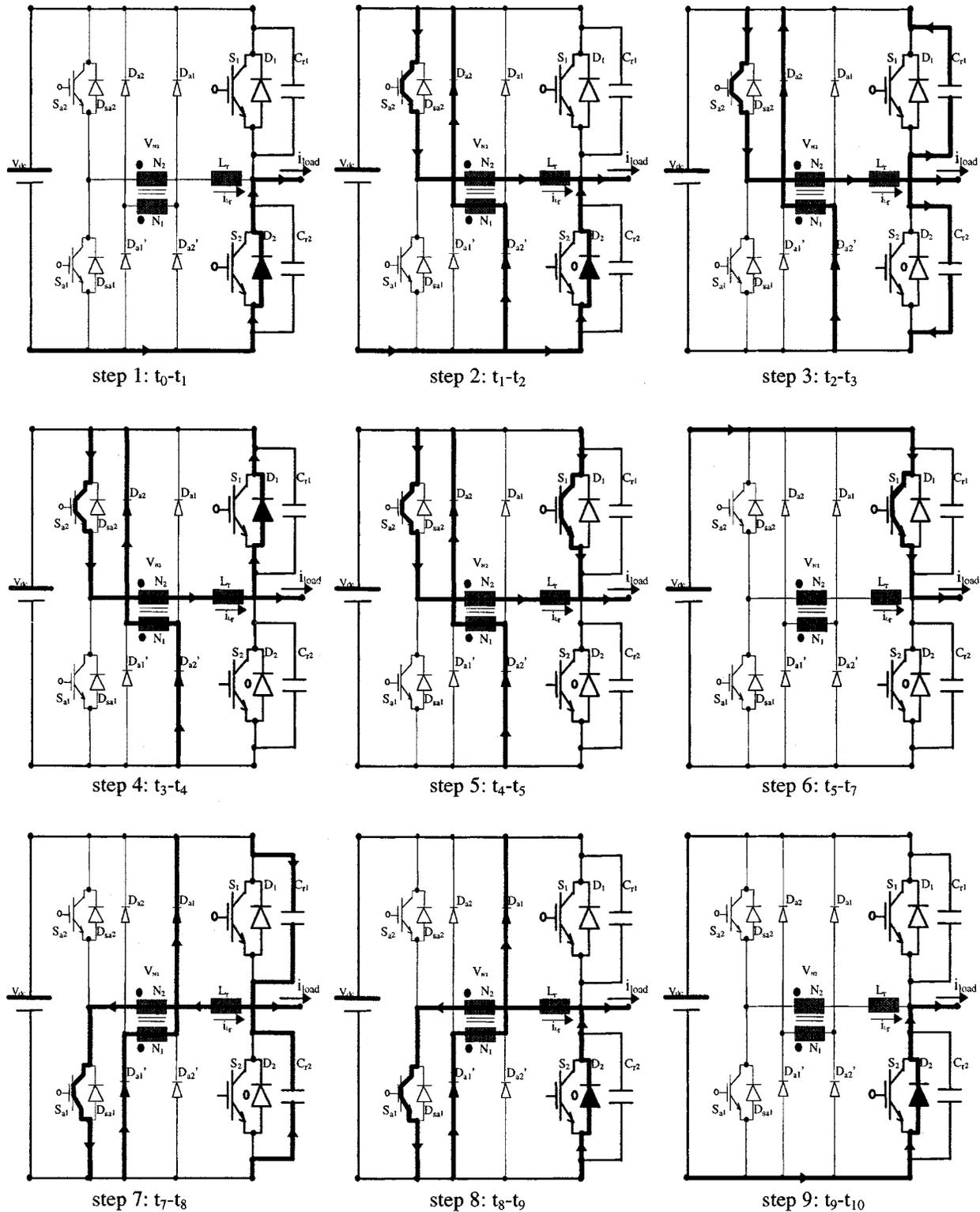
Fig. 3.   Commutation step diagrams of the transformer-assisted PWM zero-voltage switching pole inverter during a switching cycle under positive load current.

The circuit returns to the original steady state. D_2 carries the full load current (same to Step 1).

Commutation procedure under negative load current can be analogously inferred.

To compare with the ARCPI circuit, the proposed circuit has the following features.

a) The introduction of the auxiliary transformer creates a voltage source of $(1 - k)V_{\text{dc}}$ which is higher than $V_{\text{dc}}/2$ forcing the commutation resonance, rather than that con-
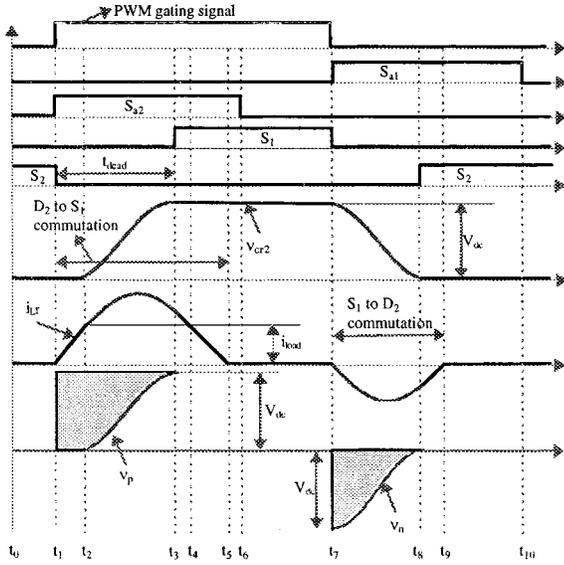
Fig. 4. Predicted commutation waveforms during a switching cycle under positive load current.
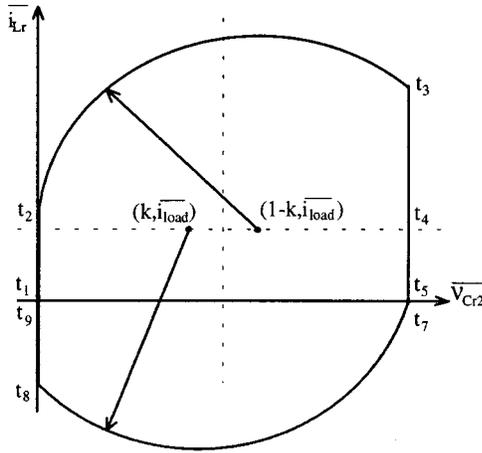

Fig. 5. Phase plane representation of the resonances during a switching cycle under positive load current.

strained at $(1/2)V_{\text{dc}}$ in the ARCPI circuit. The higher voltage source ensures zero-voltage switching and advance triggering is no longer necessary. As such, the main switch and its corresponding auxiliary switch can always be gated simultaneously without any extra monitoring or controlling circuit.

b) Bridge structure of the auxiliary circuit ensures tight clamping of the auxiliary devices. Protection circuit is no longer necessary. On the other hand, despite the bridge structure, no reverse recovery current will occur when turning on the auxiliary switch, as the opposite freewheeling diode has not been in conduction prior to the turning on. The bridge structure also enables the use of module for the auxiliary circuit, which may ease the integration of the system.

c) The need for a dc link capacitor center tap is removed. Possible adverse influence from the center-tap potential vari-

ation is eliminated. It may also imply a capacitor volume reduction in the case where center tap is not readily available.

It is worth noting, however, that the auxiliary transformer in the proposed circuit may cause manufacturing penalty. Moreover, the auxiliary devices now have to block the whole dc link voltage.

III. MATHEMATICAL ANALYSIS OF THE TRANSFORMER-ASSISTED PWM ZERO-VOLTAGE SWITCHING POLE INVERTER

A quantitative analysis of the proposed circuit is presented in this section. The following assumptions are made throughout the analysis.

- Snubbing capacitances $C_{r1} = C_{r2} = C_r$, resonant frequency $\omega_0 = 1/\sqrt{2C_rL_r}$, resonant impedance $Z_0 = \sqrt{L_r/2C_r}$, and switching cycle T.
- Unit current $\bar{i} = iZ_o/V_{\text{dc}}$, unit voltage $\bar{\nu} = \nu/V_{\text{dc}}$, and unit time $\bar{t} = t\omega_0$.

Based on these assumptions, the phase plane representation of the L_r current and C_{r2} voltage loci during the whole switching cycle is shown in Fig. 5. Curve t_1–t_5 depicts the diode-to-switch commutation (D_2 to S_1) procedure, whereas curve t_2–t_3 represents the resonance. Curve t_7–t_9 depicts the switch-to-diode commutation (S_1 to D_2) procedure, whereas the resonance is represented by curve t_7–t_8.

A. Total Commutation Duration and Duty-Cycle Limitation

Total commutation duration decides the auxiliary switch gating signal width. It imposes yet a duty-cycle limitation on modulation. The next commutation can start only after the conclusion of the previous commutation. Expressions for total commutation duration are given in Table I. Variations of the total commutation duration with load current and transformer ratio are shown in Fig. 6(a) and (b).

Apparently, for diode-to-switch commutation, the total commutation duration increases with load current and decreases with transformer ratio. For switch-to-diode commutation, however, the total commutation duration decreases with both load current and transformer ratio. The auxiliary switch gating signal width should be set covering the maximum commutation duration at peak load current and remains constant over the low-frequency cycle.

B. Auxiliary Switch Peak Current

Peak current concerns the rating of the auxiliary switch and the designing of resonant inductor. Expressions for the peak current are given in Table II. Variations of the peak current with load current and transformer ratio are shown in Fig. 7(a) and (b).

Obviously, for diode-to-switch commutation, the peak current increases with load current and decreases with transformer ratio. For switch-to-diode commutation, the peak current decreases with both load current and transformer ratio.

C. Auxiliary Switch RMS Current

Auxiliary switch rms current concerns the rating of the auxiliary devices. Auxiliary switch flows the diode-to-switch

TABLE I
TOTAL COMMUTATION DURATION EXPRESSIONS FOR DIODE-TO-SWITCH COMMUTATION AND SWITCH-TO-DIODE COMMUTATION

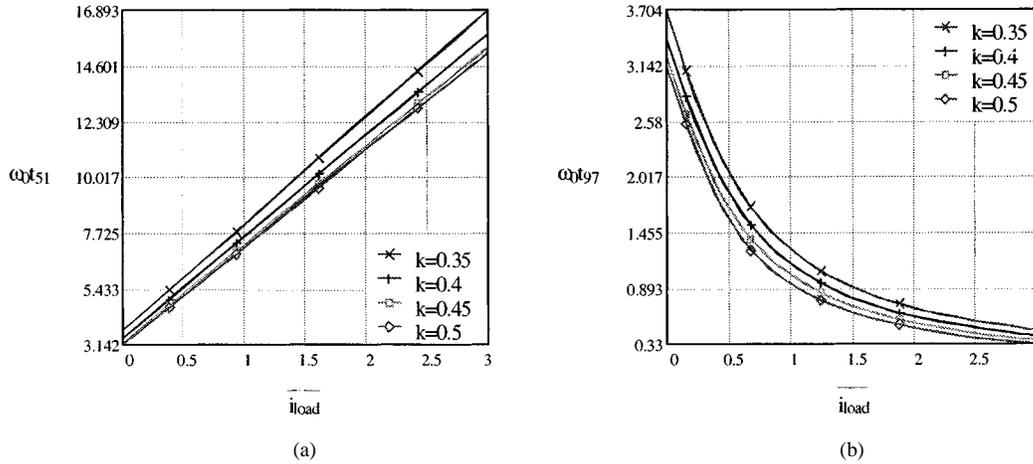|	actual expressions		expressions in unit value	
diode to switch commutation	$i_{sap1} = i_{load} + \dfrac{\sqrt{(1-k)^2(V_{dc})^2}}{Z_o}$	(5)	$\overline{i_{sap_1}} = (\overline{i_{load}} + 1 - k)$	(7)
switch to diode commutation	$i_{sap2} = \dfrac{\sqrt{(1-k)^2(V_{dc})^2 + [i_{load}Z_o]^2}}{Z_o} - i_{load}$	(6)	$\overline{i_{sap_2}} = (\sqrt{(1-k)^2 + \overline{i_{load}}^2} - \overline{i_{load}})$	(8)

Fig. 6. Variations of commutation durations t_{51} and t_{97} with load current and transformer ratio: (a) diode-to-switch commutation and (b) switch-to-diode commutation.

TABLE II
PEAK RESONANT CURRENT EXPRESSIONS FOR DIODE-TO-SWITCH COMMUTATION AND SWITCH-TO-DIODE COMMUTATION

	actual expressions		expressions in unit value	
diode to switch commutation	$i_{sap1} = i_{load} + \dfrac{\sqrt{(1-k)^2(V_{dc})^2}}{Z_o}$	(5)	$\overline{i_{sap_1}} = (\overline{i_{load}} + 1 - k)$	(7)
switch to diode commutation	$i_{sap2} = \dfrac{\sqrt{(1-k)^2(V_{dc})^2 + [i_{load}Z_o]^2}}{Z_o} - i_{load}$	(6)	$\overline{i_{sap_2}} = (\sqrt{(1-k)^2 + \overline{i_{load}}^2} - \overline{i_{load}})$	(8)

commutation current for one load current direction and the switch-to-diode commutation current for the other load current direction. For the two currents, the rms expressions solved over switching cycle are i_{saprms} and i_{sanrms}, respectively, as given in Table III. Variations of the two currents with load current, transformer ratio, and switching cycle are shown in Fig. 8(a) and (b).

Analogous to the previous cases, the auxiliary switch rms current corresponding to diode-to-switch commutation increases with load current, but decreases with transformer ratio and switching cycle. In the meanwhile, the auxiliary switch rms current corresponding to switch-to-diode commutation decreases with load current, transformer ratio, and switching cycle.

This result strongly justifies the gating plan in this paper triggering the corresponding auxiliary switch simultaneously when the main switch is turned off, either for diode-to-switch commu-

tation or for switch-to-diode commutation, no matter what are the load current amplitude or direction. Even though triggering of the auxiliary switch for switch-to-diode commutation at load current beyond an adequate level is not necessary, it causes negligible extra loss while brings significant control simplification.

The resonant inductor rms current essential for resonant inductor and auxiliary transformer designing is given by

$$i_{lrrms} = \sqrt{i_{saprms}^2 + i_{sanrms}^2}.$$

Variations of this current with load current, transformer ratio, and switching cycle is shown in Fig. 9.

D. Resonant Capacitor RMS Current

Resonant capacitor rms current information is essential for resonant capacitor rating. Resonant capacitor current consists of the diode-to-switch commutation component and the switch-to-
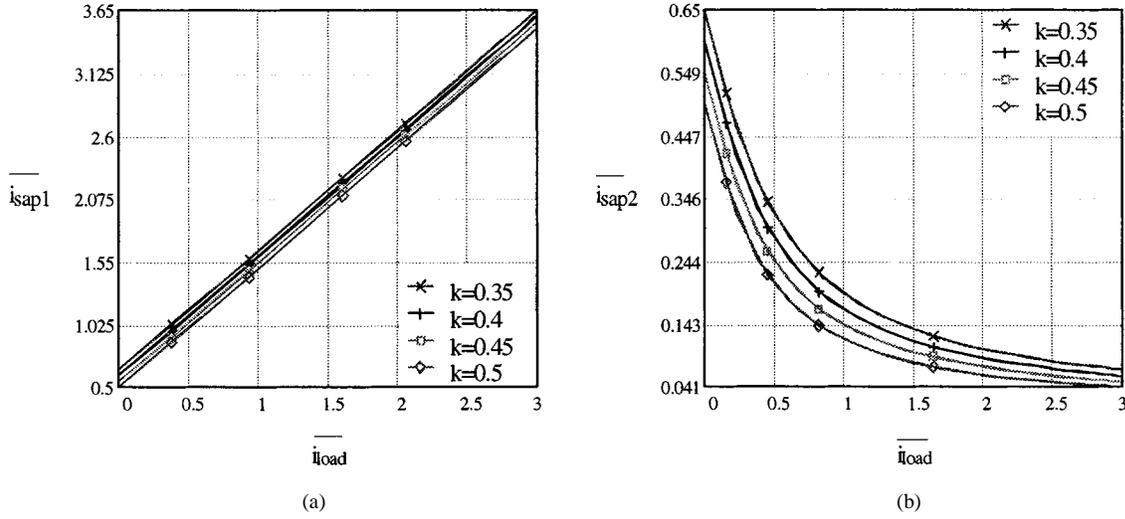
Fig. 7. Variations of the auxiliary switch peak currents with load current and transformer ratio: (a) diode-to-switch commutation and (b) switch-to-diode commutation.

TABLE III
AUXILIARY SWITCH RMS CURRENT EXPRESSIONS FOR DIODE-TO-SWITCH AND SWITCH-TO-DIODE COMMUTATIONS

	actual expressions	expressions in unit value
diode to switch commutation	$$i_{saprms} = \sqrt{\frac{1}{T}\int_0^{k_{1p}} i_{1p}{}^2 dt + \frac{1}{T}\int_0^{k_{2p}} i_{2p}{}^2 dt + \frac{1}{T}\int_0^{k_{3p}} i_{3p}{}^2 dt} \quad (9)$$ where: $$i_{1p} = \frac{V_{dc}(1-k)}{L_r}t$$ $$k_{1p} = i_{load}\frac{L_r}{(1-k)V_{dc}}$$ $$i_{2p} = i_{load} + (1-k)\frac{V_{dc}}{Z_o}\sin(\omega_o t)$$ $$k_{2p} = \frac{\pi - a\cos(\frac{k}{1-k})}{\omega_o}$$ $$i_{3p} = \frac{V_{dc}}{Z_o}\sqrt{(1-k)^2 - k^2} + i_{load} - \frac{kt}{L_r}V_{dc}$$ $$k_{3p} = \frac{L_r i_{load}}{kV_{dc}} + \frac{L_r\sqrt{(1-k)^2 - k^2}}{kZ_o}$$	$$(\overline{i_{saprms}})^2 = \frac{1}{T}\int_0^{\overline{k_{1p}}}[(1-k)\bar{t}]^2 d\bar{t}$$ $$+ \frac{1}{T}\int_0^{\overline{k_{2p}}}[\overline{i_{load}} + (1-k)\sin(\bar{t})]^2 d\bar{t} + \frac{1}{T}\int_0^{\overline{k_{3p}}}[\sqrt{1-2k} + \overline{i_{load}} - k\bar{t}]^2 d\bar{t}$$ (10) where: $$\overline{k_{1p}} = \overline{i_{load}}/(1-k)$$ $$\overline{k_{2p}} = \pi - a\cos(\frac{k}{1-k})$$ $$\overline{k_{3p}} = (\overline{i_{load}} + \sqrt{1-2k})/k$$
switch to diode commutation	$$i_{sanrms} = \sqrt{\frac{1}{T}\int_0^{k_{1n}} i_{1n}{}^2 dt + \frac{1}{T}\int_0^{k_{2n}} i_{2n}{}^2 dt} \quad (11)$$ where: $$i_{1n} = i_{load} - \frac{(1-k)\sin(\omega_o t)}{Z_o}V_{dc} - i_{load}\cos(\omega_o t)$$ $$k_{1n} = \frac{\pi - a\cos\frac{kV_{dc}}{\sqrt{(1-k)^2 V_{dc}{}^2 + [i_{load}Z_o]^2}}}{\omega_o} - \frac{a\cos\frac{(1-k)V_{dc}}{\sqrt{(1-k)^2 V_{dc}{}^2 + [i_{load}Z_o]^2}}}{\omega_o}$$ $$i_{2n} = -\frac{\sqrt{(V_{dc})^2[(1-k)^2 - k^2] + [i_{load}Z_o]^2}}{Z_o} + i_{load} + \frac{ktV_{dc}}{L_r}$$ $$k_{2n} = \{\sqrt{[(1-k)^2 - k^2]V_{dc}{}^2 + [i_{load}Z_o]^2} - i_{load}Z_o\}\frac{L_r}{kZ_o V_{dc}}$$	$$(\overline{i_{sanrms}})^2 = \frac{1}{T}\int_0^{\overline{k_{1n}}}[\overline{i_{load}} + (k-1)\sin(\bar{t}) - \overline{i_{load}}\cos(\bar{t})]^2 d\bar{t}$$ $$+ \frac{1}{T}\int_0^{\overline{k_{2n}}}[-\sqrt{1-2k + (\overline{i_{load}})^2} + \overline{i_{load}} + k\bar{t}]^2 d\bar{t}$$ (12) where: $$\overline{k_{1n}} = \pi - a\cos\frac{k}{\sqrt{(1-k)^2 + (\overline{i_{load}})^2}} - a\cos\frac{1-k}{\sqrt{(1-k)^2 + (\overline{i_{load}})^2}}$$ $$\overline{k_{2n}} = (\sqrt{(1-k)^2 + (\overline{i_{load}})^2} - \overline{i_{load}})/k$$

diode commutation component during a switching cycle. The rms expressions for both components are given in Table IV. Resonant capacitor rms current $i_{crrms} = \sqrt{i_{cprms}^2 + i_{cnrms}^2}$. Variations of the resonant capacitor rms current with load current, transformer ratio and switching cycle are shown in Fig. 10.

From Fig. 10, the resonant capacitor rms current decreases with transformer ratio and switching cycle. For load current within 1 unit amplitude, it decreases also with load current. Beyond which, it becomes independent of the load current.
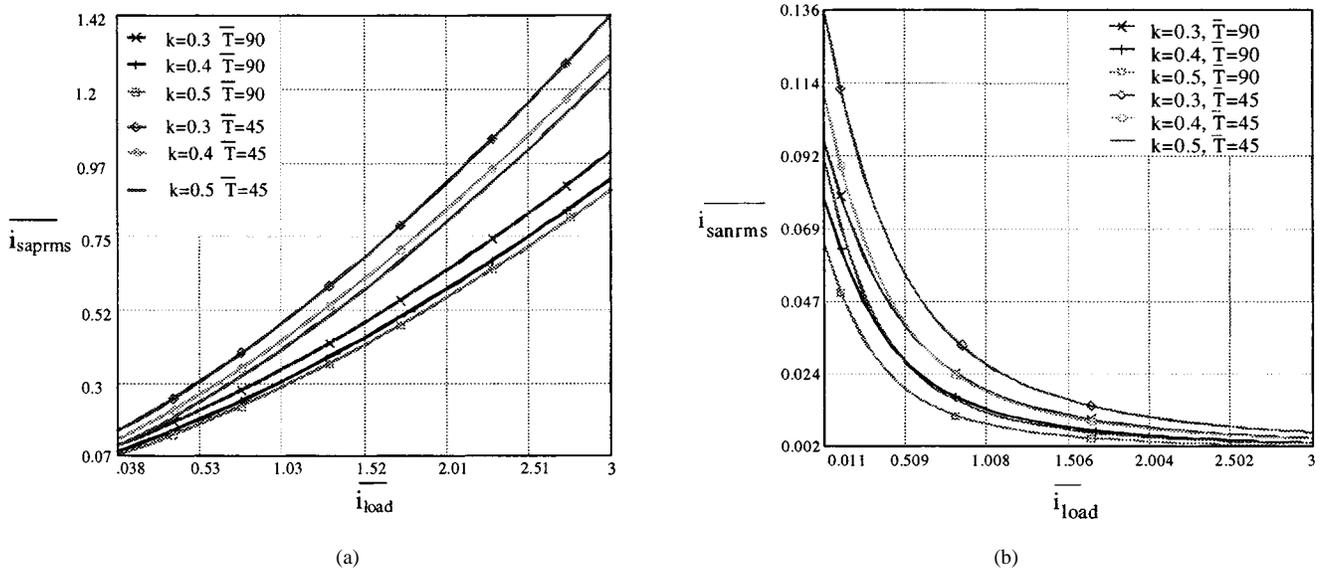
(a)

(b)

Fig. 8. Variations of the auxiliary switch rms currents with load current, transformer ratio, and switching cycle: (a) diode-to-switch commutation and (b) switch-to-diode commutation.

TABLE IV
RESONANT CAPACITOR RMS CURRENT EXPRESSIONS FOR DIODE-TO-SWITCH AND SWITCH-TO-DIODE COMMUTATIONS

	actual expressions		expressions in unit value	
diode to switch commutation	$i_{cprms} = \sqrt{\dfrac{1}{T}\displaystyle\int_0^{k_2 p}(\dfrac{(1-k)V_{dc}\sin(\omega_0 t)}{2Z_0})^2\,dt}$	(13)	$\overline{i_{cprms}} = \sqrt{\dfrac{1}{\overline{T}}\displaystyle\int_0^{\overline{k_2 p}}(\dfrac{(1-k)V_{dc}\sin(\overline{t})}{2})^2\,d\overline{t}}$	(15)
switch to diode commutation	$i_{cnrms} = \sqrt{\dfrac{1}{T}\displaystyle\int_0^{k_2 p}(\dfrac{i_{load}(1-\cos(\omega_0 t))}{2}+\dfrac{V_{dc}(k-1)\sin(\omega_0 t)}{2Z_0})^2\,dt}$	(14)	$\overline{i_{cnrms}} = \sqrt{\dfrac{1}{\overline{T}}\displaystyle\int_0^{\overline{k_2 p}}(\dfrac{\overline{i_{load}}(1-\cos(\overline{t}))}{2}+\dfrac{(k-1)\sin(\overline{t})}{2})^2\,d\overline{t}}$	(16)

E. Pole Voltage Loss

Under zero-voltage switching, pole voltage (ν_{cr2}) during commutation period is not defined by the PWM gating signal, but by the load current direction together with the resonance. Pole voltage loss is caused due to the difference of the actual output voltage from the ideal PWM output voltage, as shown by the shaded areas in Fig. 4. Expression for such pole voltage loss is given in Table V. Variations of the pole voltage loss with load current, transformer ratio and switching cycle are shown in Fig. 11.

Fig. 11 indicates that with positive load current, the actual pole output voltage is lower than the ideal PWM output. The difference increases with load current and transformer ratio, but decreases with switching cycle. For negative load current, the relationship remains, but the sign of the difference will be negative and the actual output will be higher than the ideal PWM output. This result is similar to the dead-time effect in conventional inverter [18]. However, unlike the current case, the voltage loss due to dead-time effect is not associated with load current amplitude.
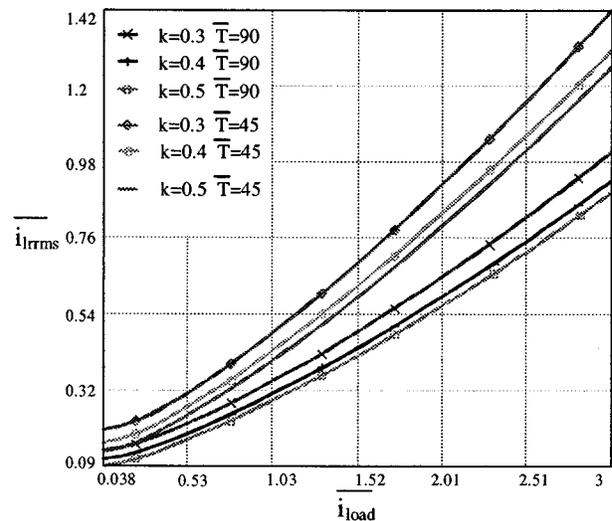

Fig. 9. Variations of the resonant inductor rms current with load current, transformer ratio, and switching cycle.
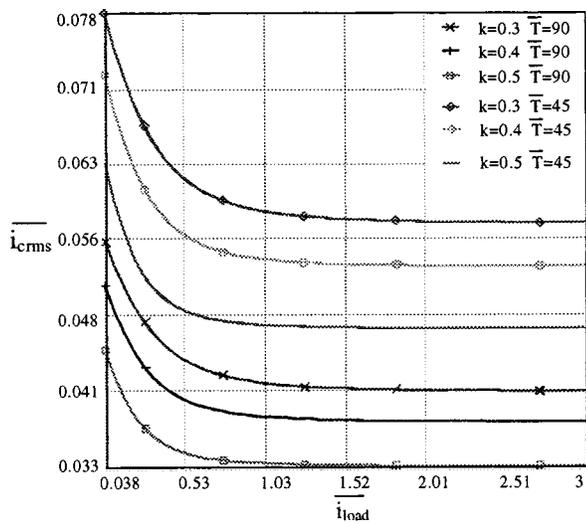
Fig. 10. Variations of the resonant capacitor rms current with load current, transformer ratio, and switching cycle.
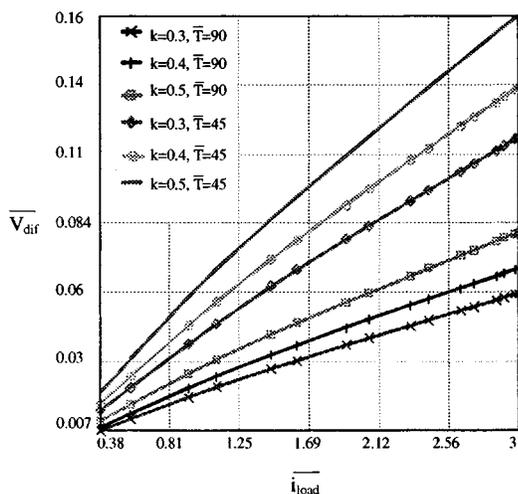

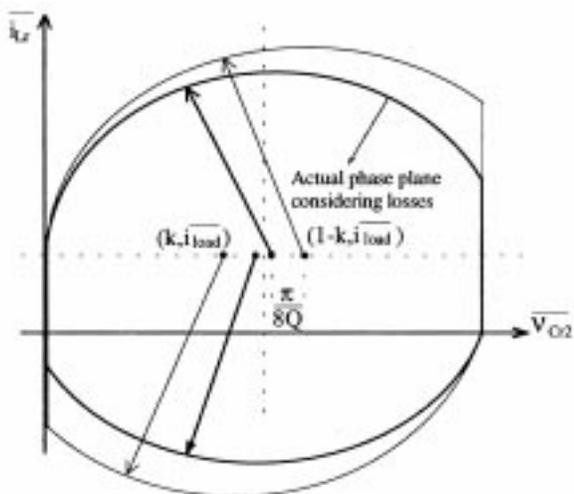Fig. 11. Variations of the pole voltage loss with load current, transformer ratio, and switching cycle.

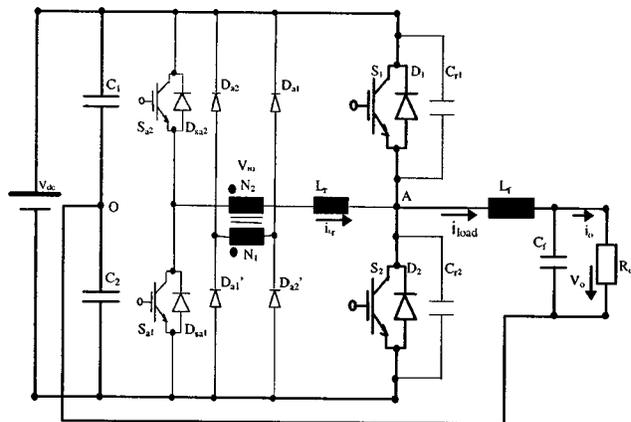Fig. 12. Actual phase plane for the resonance after considering the losses in the process.

Fig. 13. Configuration of the 4.25-kW half-bridge IGBT inverter prototype.

IV. DESIGNING METHODOLOGY OF THE TRANSFORMER-ASSISTED PWM ZERO-VOLTAGE SWITCHING POLE INVERTER

A. Transformer Ratio k

When losses in the resonance process are considered, the actual phase plane becomes changed due to the damping effect of the losses, as shown in Fig. 12 by the hard line locus. To guarantee that the pole voltage can still reach the rail level in this case, the transformer ratio k should meet

$$(1 - k) - \frac{\pi}{8Q} \geq \frac{1}{2} \tag{19}$$

where $Q = (\omega_o L_r)/R$ and R is the equivalent resistance of the resonance loop. For either the diode-to-switch commutation resonance or the switch-to-diode commutation resonance, the center point of the phase plane is shifted by $\pi/8Q$ to include the effect of losses. Equation (19) can be simplified to

$$k \leq \frac{1}{2} - \frac{\pi}{8Q}. \tag{20}$$

Transformer ratio should get the minimum value under the condition defined in (20). This will keep minimum commutation duration and minimum rms stress with the auxiliary switch. Even though less transformer ratio produces less pole voltage loss which means better dc voltage utilization.

B. Resonant Frequency ω_o

The resonant frequency should be set by optimizing the rms current stress of the auxiliary switch according to Fig. 8(a) based on the desired switching frequency of the system.

C. Resonant Capacitance C_r and Resonant Inductance L_r

The resonant capacitance should be optimized for the main switch turn-off loss [2]. Based on the resonant frequency and the resonant capacitance, the resonant inductance is then decided.

D. Auxiliary Switch Gating Signal Width/Duty-Cycle Limitation

The minimum width of the auxiliary switch gating signal must be set covering the maximum commutation duration, as

TABLE V
POLE VOLTAGE LOSS EXPRESSION

actual expression		expression in unit value	
$V_{dif} = \frac{1}{T}(\int_0^{k_{1p}} V_{dc}\,dt + \int_0^{k_{2p}} (V_{dc} - v_p)\,dt + \int_0^{k_{1n}} v_n\,dt)$	(17)	$\overline{V_{dif}} = \frac{1}{T}(\int_0^{\overline{k_{1p}}} dt + \int_0^{\overline{k_{2p}}}(1 - \overline{v_p})\,d\bar{t} + \int_0^{\overline{k_{1n}}} \overline{v_n}\,d\bar{t})$	(18)
where:		where:	
$v_p = (1-k)V_{dc} + (k-1)V_{dc}\cos(\omega_o t)$		$\overline{v_p} = (1-k) + (k-1)\cos(\omega_o t)$	
$v_n = -[kV_{dc} + (1-k)V_{dc}\cos(\omega_o t) - i_{load}Z_o\sin(\omega_o t)]$		$\overline{v_n} = -[-k + (1-k)\cos(\omega_o t) - \overline{i_{load}}\sin(\omega_o t)]$	

100V/Div; 20A/Div; 5mS/Div
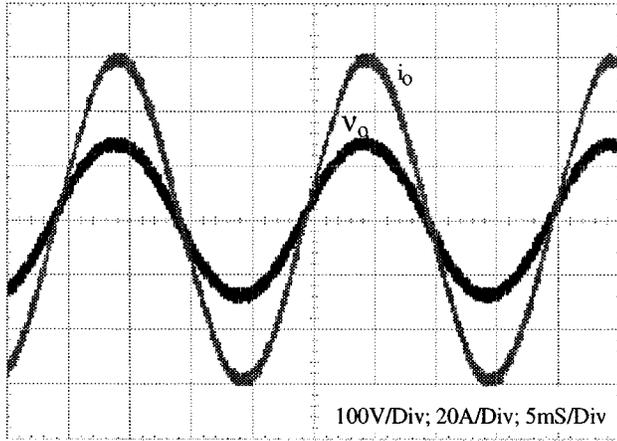
Fig. 14. Experimental load-side output voltage and filter inductor current.
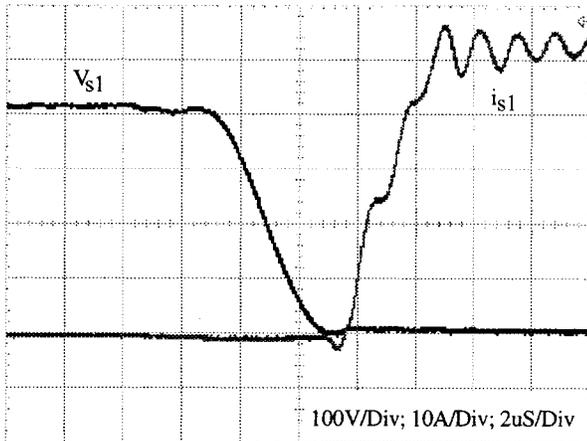

100V/Div; 10A/Div; 2uS/Div

Fig. 15. Experimental zero-voltage turn on of the main switch (S_1).

demonstrated in Fig. 6(a). In the meanwhile, inverter duty cycle should be set to allow for conduction duration of main switch not less than the auxiliary switch gating signal width.

E. Rating of the Auxiliary Switch

Due to zero-current switching in the auxiliary circuit and due also to the high switching frequency with respect to the thermal inertia of the device, the rating of the auxiliary switch should be chosen according to its rms stress as illustrated in Fig. 8(a). However, auxiliary switch peak current defined from Fig. 7(a) should not exceed the device peak output current rating, which is normally 25% higher than the device peak switching current in the case of IGBT.

F. Magnetics Designing

With information of peak current, rms current, and magnetization duration, the resonant inductor and the auxiliary transformer can be designed.

Note that aside from the transformer ratio that is attributed to ensure zero-voltage switching, designing of the resonant parameters is always a compromise among the many factors such as switching loss, device rating, and dc voltage utilization, etc. Practical designing should be oriented for serving the specific designing purpose where one particular requirement may outweigh the others.

V. EXPERIMENTATION OF THE TRANSFORMER-ASSISTED PWM ZERO-VOLTAGE SWITCHING POLE INVERTER

A proof-of-concept 4.25-kW IGBT half-bridge inverter as shown in Fig. 13 has been built, with normal subharmonic sinusoidal PWM modulation pattern. Specifications of the prototype are shown in Table VI. Designing results of the resonant and transformer parameters are shown in Table VII.

As a result of the above designing, the resultant maximum commutation duration is 12.7 uS according to Fig. 6(a). The maximum peak and rms currents of the auxiliary switch are 89.5 and 21.5 A, respectively, according to Figs. 7(a) and 8(a). Thus, the auxiliary switch gating signal width is set at 14.4 uS and the minimum and maximum PWM widths are set at 16.8 and 136.8 uS, respectively. Dead time of 2.4 uS is inserted interlocking the two main switches.

Two SEMIKRON IGBT modules (SKM50GB123D, 1200 V/50 A) are employed as the main and auxiliary switches, four ultrafast HFA30TA60C (600 V/30 A) work as the auxiliary diodes. Two storage capacitors C_1 and C_2 each rated at 350 V/3300 uF form the dc center tap. A low-pass filter ($L_f = 1.45$ mH, $C_f = 12$ uF) is installed at the output.

Besides, four SEMIKRON SKH10 intelligent driver are used for driving of the main and auxiliary IGBT's. Each driver is interfaced by an external zero-voltage detecting circuit [17] to the gate terminal of the IGBT module, which releases the gating signal when the detected voltage becomes zero.

From the load-side output voltage and filter inductor current waveforms shown in Fig. 14, the peak value of the voltage (averaged) at the filter input is deduced to be 142.6 V, indicating a experimental peak voltage loss of 13.4 V. In correspondence, the predicted peak voltage loss according to Fig. 11 is 10 V. In Fig. 15, the details of zero-voltage turn on of the main switch S_1 at $i_{load} = 56$ A are shown. For a predicted dv/dt of 111 V/uS (averaged over t_2-t_3) and di/dt of 20 A/uS, the experimental values are about 114 V/uS and 18 A/uS, respectively.
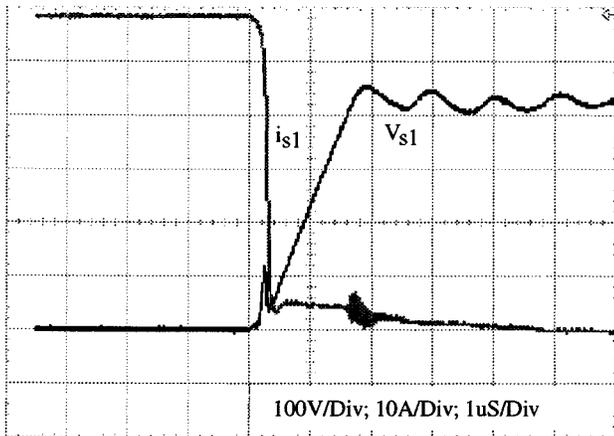
100V/Div; 10A/Div; 1uS/Div

Fig. 16.   Experimental capacitive turn off of the main switch (S_1).

100V/Div; 10A/Div; 5uS/Div

Fig. 18.   Experimental inductive turn on and zero-current turn off of the auxiliary switch (S_{a2}).

100V/Div; 20A/Div; 5uS/Div

Fig. 17.   Experimental zero-voltage turn on of the main switch (S_1) at zero-load current.

100V/Div; 10A/Div; 5uS/Div
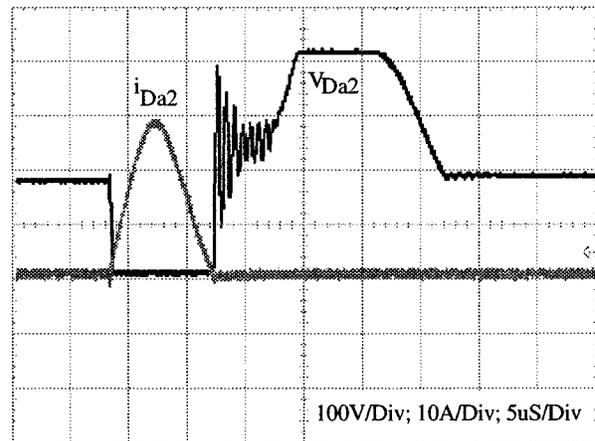
Fig. 19.   Experimental inductive turn on and zero-current turn off of the auxiliary diode (D_{a2}).

In Fig. 16, the details of capacitive turn off of the main switch S_1 at $i_{load} = 56$ A are shown. For a predicted dv/dt of 307 V/uS (averaged over t_7–t_8), the experimental value is about 277 V/uS. The first voltage spike of about 120 V appears due to the stray inductance in the turn-off snubbing path (prolonged loop for measurement objective). Fig. 17 shows the main switch zero-voltage turn on at zero-load current.

Fig. 18 shows the commutation process of the auxiliary switch (S_{a2}) at $i_{load} = 20$ A. For the predicated commutation duration of 7.2 uS according to Fig. 6(a), and the predicted peak current of 47.8 A according to Fig. 7(a), the experimental values are 6.7 uS and 40.5 A, respectively. The turn on is inductive and no reverse recovery current from the opposite diode is seen. Besides, no turn-off voltage spike is generated. The voltage protrusion in the middle screen occurs due to the dynamic charging/discharging of the floating middle potential of the auxiliary leg. Fig. 19 shows the commutation process of the auxiliary diode (D_{a2}) at the transformer primary side. The voltage spike following turn off does not exceed the rail level.

VI. Conclusions

From the above discussion, analysis, and experimentation, the following conclusions are drawn.
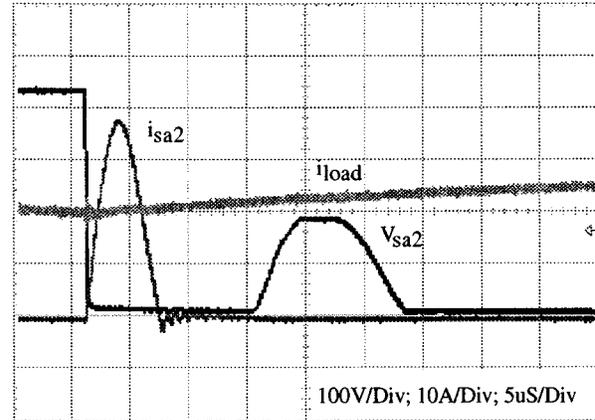
a) With the transformer ratio set less than 1/2 as per the resonance loop losses, the proposed circuit ensures zero-voltage switching of the main switch and zero-current switching of the auxiliary switch without any extra measuring or controlling. The corresponding auxiliary switch can be turned on simultaneously when the main switch is turned off.

b) The auxiliary devices are tightly clamped to the dc rail voltage and protection circuit for the auxiliary devices is no longer necessary. The turn on of the auxiliary device sees no reverse recovery current from the opposite freewheeling diode despite the bridge configuration of the auxiliary circuit. With the transformer structure, magnetization of the transformer core returns to zero following each commutation and no magnetic accumulation is present.

c) Mathematical analysis for the auxiliary circuit regarding commutation duration, auxiliary circuit stresses, and pole voltage loss is validated.

d) The proposed circuit presents an interesting alternative for the ARCPI circuit to be used for high-power advanced applications due to the simplicity and reliability.

TABLE VI
SPECIFICATIONS OF THE 4.25-kW HALF-BRIDGE IGBT INVERTER PROTOTYPE

DC input voltage	V_{dc}=400V	Output voltage	$V_{o.rms}$ =100V	Modulation index	M=0.78
Output power	P_o=4.25kW	Load current	$I_{o.rms}$ =42.5A	Switching frequency	f_c=6.5kHz

TABLE VII
RESONANT AND TRANSFORMER DESIGNING RESULTS FOR THE 4.25-kW HALF-BRIDGE IGBT INVERTER PROTOTYPE

Resonant capacitor	*1*. Capacitance: C_r=0.1uF, *2*. Type: low-loss polypropylene, *3*. Estimated maximum turn-off loss 4W.
Resonant inductor	*1*. Inductance: L_r=12uH, *2*. Structure: 36 turns 15AWG copper wire wound on air core bobbin, *3*. Current rate of change 20A/uS.
Auxiliary transformer	*1*. Transformer ratio: k =0.4, *2*. Structure: Two in parallel each made up of 60 turns Litz wire (7 strands 24AWG) in the primary and 24 turns Litz wire (15 strands 24AWG) in the secondary wound on E65/29 ferrite core, *3*. Allowed equivalent resonant loop resistance around 1.95Ω.

REFERENCES

[1] D. Divan, "Low-stress switching for efficiency," *IEEE Spectrum*, pp. 33–39, Dec. 1996.
[2] R. L. Steigerwald, R. W. De Doncker, and M. Kheraluwala, "A comparison of high power dc–dc soft switched converter topologies," *IEEE Trans. Ind. Applicat.*, vol. 32, pp. 1139–1145, Sept./Oct. 1996.
[3] G. Bingen, "Utilization de Transistors a Fort Courant et Tension Elevee," in *Rec. EPE Conf.*, 1987, pp. 1.15–1.20.
[4] R. W. De Doncker and J. P. Lyons, "The auxiliary resonant commutated pole inverter," in *Rec. IEEE IAS*, 1990, pp. 1228–1235.
[5] W. McMurray, "Resonant snubbers with auxiliary switches," *IEEE Trans. Ind. Applicat.*, vol. 29, pp. 355–362, Mar./Apr. 1993.
[6] F. F. Protiwa and J. Koß, "A 20 kVA auxiliary resonant commutated pole converter—Design and practical experiences," in *Rec. EPE'95*, pp. 2.111–2.116.
[7] K. Iida and H. Matsuo, "The influence of the conducting inductance in the auxiliary resonant commutated pole inverter," in *Rec. IEEE PESC'97*, pp. 1238–1245.
[8] H. J. Beukes, J. H. R. Enslin, and R. Spee, "Integrated active snubber for high power IGBT modules," in *Rec. IEEE APEC*, 1997, pp. 161–167.
[9] H. Matsuo, K. Iida, and K. Harada, "210 kVA soft switching PWM type ac auxiliary power supply system of the electric railway rolling stock using an improved ARCP three phase inverter with SI thyristor switches," in *Rec. IPEC-Yokohama*, 1995, pp. 831–836.
[10] H. G. Eckel, L. Sack, and K. Rascher, "FPGA based control of an ARCP-inverter without additional sensors," in *Rec. EPE'97*, pp. 4.385–4.390.
[11] F. R. Salberta, J. S. Mayer, and R. T. Cooley, "An improved control strategy for a 50-kHz auxiliary resonant commutated pole converter," in *Rec. IEEE PESC*, 1997, pp. 1246–1252.
[12] J. S. Lai, R. W. Young, Sr., G. W. Ott, Jr., J. W. Mckeever, and F. Z. Peng, "A Delta configured auxiliary resonant snubber inverter," in *Rec. IEEE IAS*, 1995, pp. 2618–2624.
[13] K. M. Smith, Jr. and K. M. Smedley, "Intelligent magnetic-amplifier-controlled soft-switching method for amplifiers and inverters," *IEEE Trans. Power Electron.*, vol. 13, no. 1, pp. 84–92, 1998.
[14] A. Toba, T. Shimizu, G. Kimura, M. Shioya, and S. Sano, "Auxiliary resonant commutated pole inverter using two internal voltage-points of dc source," *IEEE Trans. Ind. Electron.*, vol. 45, pp. 200–206, Apr. 1998.
[15] I. Barbi and D. C. Martins, "A true PWM zero voltage switching pole with very low additional RMS current stress," in *Rec. IEEE PESC*, 1991, pp. 261–267.
[16] H. Yonemori, K. Hayashi, and M. Nakaoka, "A novel space voltage vector modulated sinewave three phase inverter with high frequency transformer coupled resonant dc link," in *Rec. IEEE PESC*, 1994, pp. 651–658.
[17] X. Yuan, "Soft switching techniques for multilevel inverters," Ph.D. dissertation, INEP-UFSC, Brazil, May 1998.
[18] Y. Murai, T. Watanabe, and H. Iwasaki, "Waveform distortion and correction circuit for PWM inverters with switching lag-times," *IEEE Trans. Ind. Applicat.*, vol. 23, pp. 881–886, Sept./Oct. 1987.

Xiaoming Yuan (S'97–M'99) received the M.Eng. degree from Zhejiang University, China, and the Ph.D. degree from the Federal University of Santa Catarina, Florianopolis, Brazil, in 1993 and 1998, respectively, both in electrical engineering.

He was an Electrical Engineer with Qilu Petrochemical Corporation, China, from 1986 to 1990. He is currently a Post-Doctoral Researcher with the Power Electronics and Electrometrology Laboratory, Swiss Federal Institute of Technology Zurich, Switzerland, where he is working on flexible ac transmission system (FACTS) devices.

Dr. Yuan was the recipient of the first prize paper award from the industrial power converter committee of the IEEE Industry Applications Society in 1999.

Ivo Barbi (M'78–SM'90) was born in Gaspar, Santa Catarina, Brazil, in 1949. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina, Florianopolis, Brazil, in 1973 and 1976, respectively, and the Dr.Ing. degree from the Institut National Polytechnique de Toulouse, France, in 1979.

He founded the Brazilian Power Electronics Society, the Power Electronics Institute of the Federal University of Santa Catarina, and created the Brazilian Power Electronics Conference. Currently, he is Professor of the Power Electronics Institute of the Federal University of Santa Catarina.

Dr. Barbi has been an Associate Editor in the Power Converters Area of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS since 1992.