A Double ZVS-PWM Active-Clamping Forward Converter: Analysis, Design, and Experimentation

René Torrico-Bascopé, *Member, IEEE,* and Ivo Barbi, *Senior Member, IEEE*

***Abstract*—This paper presents an isolated dc–dc converter based on two ZVS-PWM active-clamping forward converters connected in series and coupled by a single high-frequency transformer. The proposed converter features no switching losses from no-load to full-load operation and low conduction losses. This converter is suitable for high input voltage (>400 Vdc) and high power applications. Operation principles, theoretical analysis and design example, are presented, as well as experimental results taken from a 3 kW laboratory prototype.**

***Index Terms*—DC–DC converter, power supply, soft switching converter.**

I. Introduction

GENERALLY, a power supply is composed of a rectifier (ac–dc converter) and an isolated dc–dc converter. Since almost all the consumed electrical energy is processed, power supplies are of great importance in their application in several systems, such as computers, sound equipments, domestic appliances, hospital apparatus, telecommunications, etc. Nowadays, the harmonic current pollution of the ac power systems is being restrained by international standards [1], and in consequence power factor correction PFC rectifiers are being incorporated to the power supplies. To obtain power factor correction, the topology generally used is the boost rectifier, which presents a higher output voltage than input voltage. For example, when a three-phase input voltage of 380 Vac is utilized, the output voltage of the rectifier is always higher than 600 Vdc. Due to the voltage limitations of the devices (semiconductors, capacitors) nowadays there is a demand for DC–DC topologies capable of operating with high bus voltage and low voltage stress across the devices.

Among the alternatives to overcome these drawbacks are the series connection of switches and multilevel topologies. In the series connection of switches, the static and dynamic sharing of the voltage across the switches is difficult to obtain and requires specific techniques. Multilevel topologies seem to be a more effective solution because they can solve the problem of static and dynamic sharing of the voltage and minimize the electromagnetic interference, since the value of dv/dt is reduced [2].

Another alternative to solve the problems of the series connection of switches is the association of two or more converters in series, reducing the voltage stress on each switching device.

Manuscript received January 17, 2000; revised July 20, 2001. Recommended by Associate Editor K. Smedley.

The authors are with the Power Electronics Institute, Federal University of Santa Catarina, Florian polis 88040–970, Brazil (e-mail: ivobarbi@inep.ufsc.br).

Publisher Item Identifier S 0885-8993(01)10576-4.

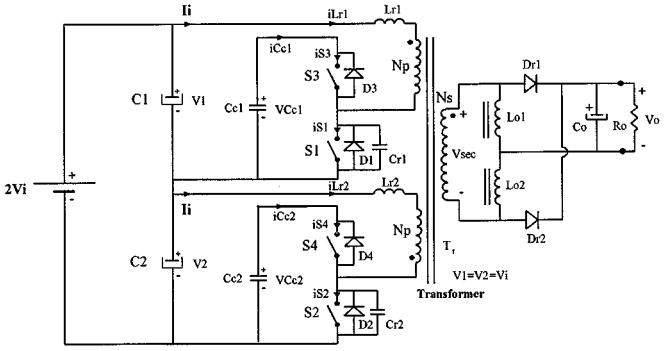

Fig. 1. Proposed dc–dc converter.

This method is appropriate if a perfect division of the voltage between the converters can be guaranteed at any time. This condition is attainable by coupling the converters with a single high-frequency power transformer as explained in [3], [4]. The associated converters coupled by a single transformer are controlled using the same control circuit. Hence, the pulse-width-modulator and drive circuits are identical for all the converters, allowing the voltage to divide itself among the switches. On the other hand, they are capable of automatically balancing the voltages of the input capacitors associated in series, which are connected to a DC bus voltage. If one of the voltages is higher, the respective capacitor transfers energy to the other through the transformer during the on time [5]–[7].

In this paper the converter shown in Fig. 1 is proposed. The converter is described and analyzed in the following sections.

II. Circuit Description and Principle of Operation

A. Circuit Description

The proposed converter, shown in Fig. 1, is composed of the following components: input voltage source 2 V_i, input capacitors C_1 and C_2, clamping capacitors C_{c1} and C_{c2}, main switches S_1 and S_2, auxiliary switches S_3 and S_4, commutation inductors L_{r1} and L_{r2}, commutation capacitors C_{r1} and C_{r2}, antiparallel diodes D_1, D_2, D_3, and D_4, three-winding high-frequency transformer T_r, rectifier diodes D_{r1} and D_{r2}, output filter, consisting of L_{o1}, L_{o2}, and C_o, and load resistance R_o.

B. Principle of Operation

The proposed converter operates in continuous conduction mode (CCM) with soft-commutation of the controlled switches and constant frequency using asymmetrical PWM modulation [8]. The assumed PWM modulation consists of two pulses with width lower than $T_s/2$ to control the switches S_1–S_2, and two

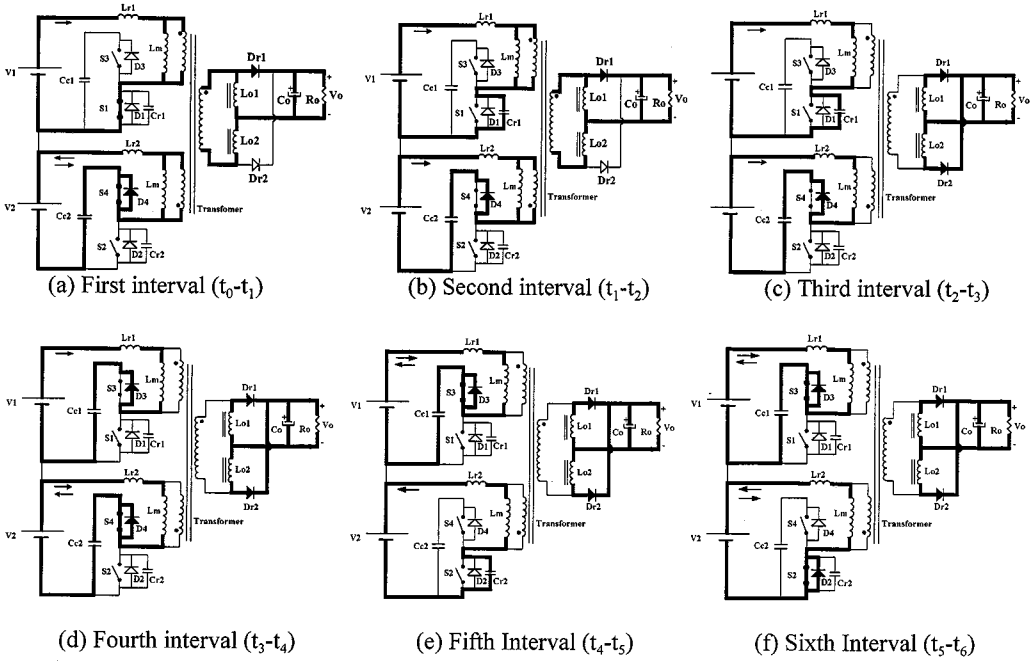

Fig. 2. Topological operation states of the proposed converter.

pulses with width higher than $T_s/2$ to control the switches S_3–S_4. The indicated pulses are complementary and easily obtained in laboratory using regulating pulse width modulator (SG3525) and hex inverting gates (MC14584) integrated circuits.

In [9], [10], other control techniques used in active-clamping converters was found, but they are complex to generate.

To simplify the analysis of the converter, the following assumptions are made:

1) the circuit operates in steady-state;
2) all components are considered ideal;
3) the output inductor filter L_{o1} and L_{o2} are large enough to be considered as current sources with a value equal to the load current $I_o/2$;
4) the voltage across the input capacitors are equal ($V_1 = V_2 = V_i$);
5) the commutation inductors are equal ($L_{r1} = L_{r2} = L_r$);
6) the clamping capacitors are equal ($C_{c1} = C_{c2} = C_c$);
7) the voltage across de clamping capacitors are equal ($V_{Cc1} = V_{Cc2} = V_{Cc}$)
8) the commutation capacitors are equal ($C_{r1} = C_{r2} = C_r$);
9) L_{r1} and L_{r2} absorb the transformer leakage inductance;
10) there is no difference between the duty cycles of the gate signals applied to each pair of switches (S_1–S_2 and S_3–S_4).

Fig. 2 shows the topological states of the converter for a half-period and Fig. 3 shows the main theoretical waveforms for one switching period. The six sequential circuit states are described below.

First Interval (t_o–t_1): During this interval, power is transferred to the load from the input source V_1 through switch S_1 and also from the clamping capacitor C_{c2}, which is discharged through switch S_4. Switches S_2 and S_3 are turned-off and

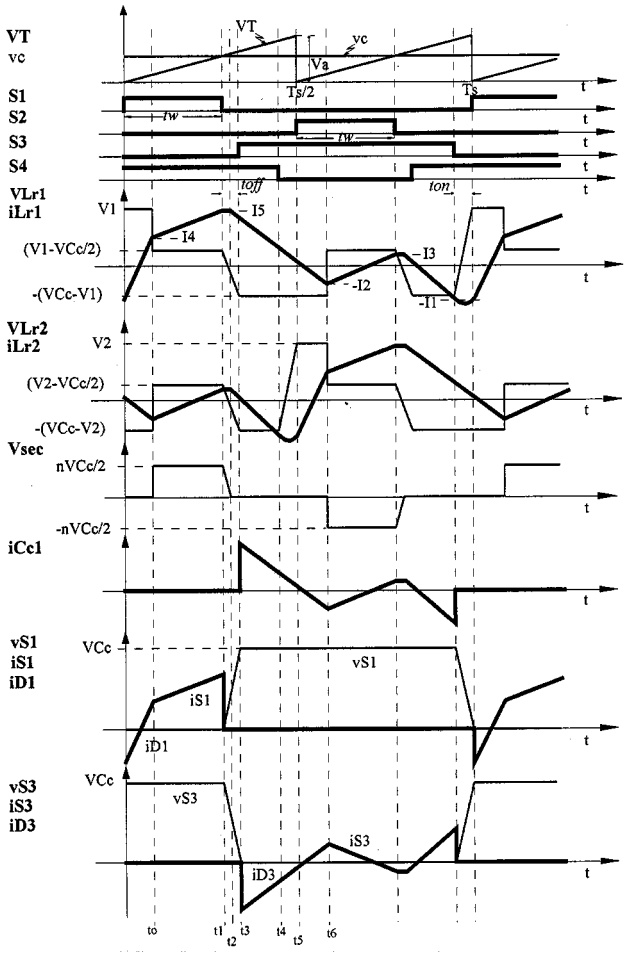

Fig. 3. Main waveforms of the proposed converter.

the voltage across them is equal to the voltage V_{Cc} across the clamping capacitors C_{c1} and C_{c2}.

Second Interval (t_1–t_2): At instant t_1, switch S_1 is turned off with zero voltage. Capacitor C_{r1} is linearly charged with a constant current. This interval finishes when the voltage across S_1 is V_1, and across S_3 is $V_{Cc} - V_1$.

Third Interval (t_2–t_3): At instant t_2, the transformer voltage is zero and consequently, resonance between C_{r1} and L_{r1} takes place. Furthermore, the freewheeling process of the output current I_o starts, involving L_{o1}, L_{o2}, D_{r1}, and D_{r2}. This interval finishes, when the voltage across S_1 reaches V_{Cc} and the voltage across S_3 reaches zero.

Fourth Interval (t_3–t_4): At instant t_3, antiparallel diode D_3 is directly biased and starts conducting the current through L_{r1}, which decreases linearly. In the same manner, the current through L_{r2} decreases linearly. During this interval the load current I_o keeps freewheeling through diodes D_{r1} and D_{r2}. Switch S_3 must be turned on before diode D_3 is reverse biased. This interval finishes when switch S_4 is turned off.

Fifth Interval (t_4–t_5): When switch S_4 is turned off, the current through L_{r2} is deviated to commutation capacitor C_{r2}, which is then discharged in a resonant way. During this interval the load current I_o keeps freewheeling. This interval finishes when the voltage across capacitor C_{r2} is null and the diode D_2 starts to conduct.

Sixth Interval (t_5–t_6): At the instant t_5, diode D_2 is directly biased and begins conducting the commutation inductor current iL_{r2}. During this condition, switch S_2 must be turned on. The current through L_{r2} decreases linearly until it reaches zero. At this point, diode D_2 is blocked, and that current inverts its direction, flowing through switch S_2. During this interval there is no power transferred to the load. Therefore, the duty cycle is reduced.

III. Theoretical Analysis and Relevant Design Curves

The duty cycle (D) and commutation period (T_s) for the proposed converter are defined by (1) and (2)

$$D = \frac{t_w}{T_s/2} \tag{1}$$

$$T_s = \frac{1}{f_s}. \tag{2}$$

In (1) and (2), t_w and f_s are, gate pulse width of switch S_1 or S_2, and commutation frequency.

A. Clamping Characteristic

The clamping voltage V_{Cc} can be obtained by determining the average voltage across the main switch S_1 and applying Kirchhoff's law to the mesh formed by S_1, the transformer's upper primary, L_{r1} and V_1. Therefore,

$$V_{Cc} = \frac{2}{(2-D)} \cdot V_i. \tag{3}$$

In (3), V_i is input voltage.

The graph of clamping voltage V_{Cc}, as a function of the duty cycle D, is shown in Fig. 10(a).

B. Output Characteristic

In the proposed converter the duty cycle reduction ΔD occurs due to the linear variation of the current through the commutation inductors (L_{r1}, L_{r2}) and transformer leakage inductances. During this condition there is no power transfer from the input. The duty cycle reduction is reflected in the transformer secondary voltage (Fig. 3).

According to the waveforms shown in Fig. 3, and considering that the commutation time is much smaller than the switching period, the average output voltage and secondary voltage of the transformer, are given by (4) and (5)

$$V_o = V_{\text{sec}} \cdot \left(\frac{D}{2} - \frac{\Delta t_1}{T_s} \right) \tag{4}$$

$$V_{\text{sec}} = n \cdot \frac{V_{Cc}}{2}. \tag{5}$$

In (4) and (5), Δt_1 and n are, time interval with no power transfer (sixth stage), and transformer turns ratio (N_s/N_p).

The interval Δt_1 in a half period is

$$\Delta t_1 = \frac{n \cdot I_o \cdot L_r \cdot (2-D)}{2 \cdot V_i}. \tag{6}$$

The reduction of the duty cycle in period T_s is given by (7)

$$\Delta D = \frac{2 \cdot \Delta t_1}{T_S}. \tag{7}$$

Substituting (6) in (7) yields

$$\Delta D = \frac{f_s \cdot n \cdot I_o \cdot L_r \cdot (2-D)}{V_i}. \tag{8}$$

In (8), I_o and L_r are, average output current, and inductance of the commutation inductor.

Substituting (3), (5), and (6) in (4), the average output voltage obtained is given by (9)

$$V_o = n \cdot V_i \cdot \left[\frac{D}{2 \cdot (2-D)} - \frac{f_s \cdot L_r \cdot n \cdot I_o}{2 \cdot V_i} \right]. \tag{9}$$

The graph of output voltage V_o as a function of the output current I_o, known as output characteristic, is shown in Fig. 10(b).

C. Commutation Analysis

This converter presents soft turn-on and turn-off commutations.

Turn-On: For analytical purposes, the commutations of switch S_2, (fifth interval) is considered.

The displacement angle at resonant frequency during turn-on for a no-load (critical) condition is given by (10)

$$\theta_{on} = \tan^{-1}\left[\frac{-\pi \cdot (1-D)}{2 \cdot \overline{f}} \right] + \cos^{-1}\left[\frac{-2 \cdot \overline{f} \cdot (2-D)}{D \cdot \sqrt{[\pi \cdot (1-D)]^2 + 4 \cdot \overline{f}^2}} \right]. \tag{10}$$

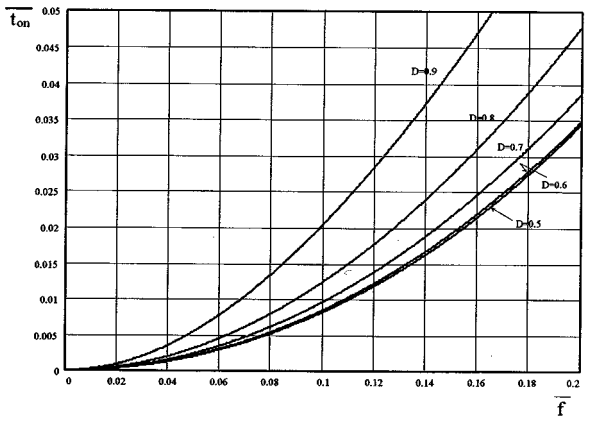

Fig. 4. Normalized discharge time interval $\overline{t_{\rm on}}$, as a function of $\overline{f}$, during turn-on.

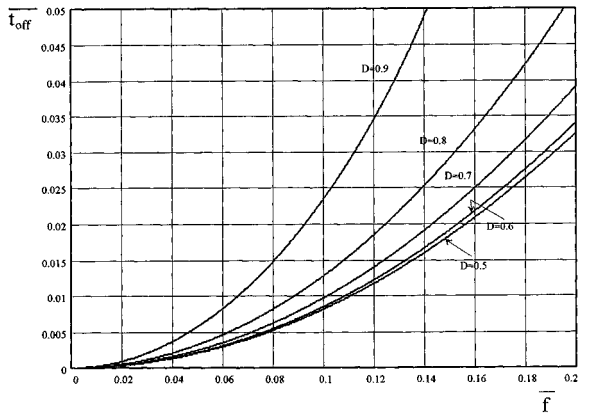

Fig. 5. Normalized charge time interval $\overline{t_{off}}$, as a function of $\overline{f}$, during turn-off.

The normalized frequency ($\overline{f}$), displacement angle at resonant frequency ($\theta_{\rm on}$), and, angular resonant frequency (ω_o), are defined by (11), (12) and (13)

$$\overline{f} = \frac{f_s}{f_o} \tag{11}$$

$$\theta_{\rm on} = \omega_o \cdot t_{\rm on} \tag{12}$$

$$\omega_o = 2 \cdot \pi \cdot f_o = \frac{1}{\sqrt{L_r \cdot C_r}}. \tag{13}$$

In (12), $t_{\rm on}$ is discharge time interval of the resonant capacitor ($C_r = C_{r2}$).

From (10)–(13), the normalized discharge time interval is obtained and represented by (14) and (15)

$$\overline{t_{\rm on}} = \frac{\overline{f}}{2 \cdot \pi} \cdot \tan^{-1}\left[\frac{-\pi \cdot (1-D)}{2 \cdot \overline{f}}\right] + \frac{\overline{f}}{2 \cdot \pi} \cdot \cos^{-1}\left[\frac{-2 \cdot \overline{f} \cdot (2-D)}{D \cdot \sqrt{[\pi \cdot (1-D)]^2 + 4 \cdot \overline{f}^2}}\right] \tag{14}$$

$$\overline{t_{\rm on}} = \frac{t_{\rm on}}{T_s}. \tag{15}$$

The normalized discharge time interval $\overline{t_{\rm on}}$, as a function of $\overline{f}$, during turn-on is shown in Fig. 4.

Turn-Off: The turn-off of switch S_1, which happens in the second and third intervals, is analyzed. During this commutation, capacitor C_{r1} is charged.

The displacement angle at resonant frequency during turn-off for a no-load (critical) condition, is given by (16) and (17)

$$\theta_{\rm off} = \frac{2 \cdot (2-D) \cdot \overline{f}}{\pi \cdot D \cdot (1-D)} + \sin^{-1}\left[\frac{2 \cdot \overline{f}}{\pi \cdot (1-D)}\right] \tag{16}$$

$$\theta_{\rm off} = \omega_o \cdot t_{\rm off}. \tag{17}$$

From (11), (13), (16), and (17), the normalized charge time interval is obtained and given by (18) and (19)

$$\overline{t_{\rm off}} = \frac{\overline{f} \cdot (2-D) \cdot \overline{f}}{\pi^2 \cdot D \cdot (1-D)} + \frac{\overline{f}}{2 \cdot \pi} \cdot \sin^{-1}\left[\frac{2 \cdot \overline{f}}{\pi \cdot (1-D)}\right] \tag{18}$$

$$t_{\rm off} = \frac{t_{\rm off}}{T_s}. \tag{19}$$

The normalized charge time interval $\overline{t_{\rm off}}$, as a function of $\overline{f}$, during turn-off is shown in Fig. 5.

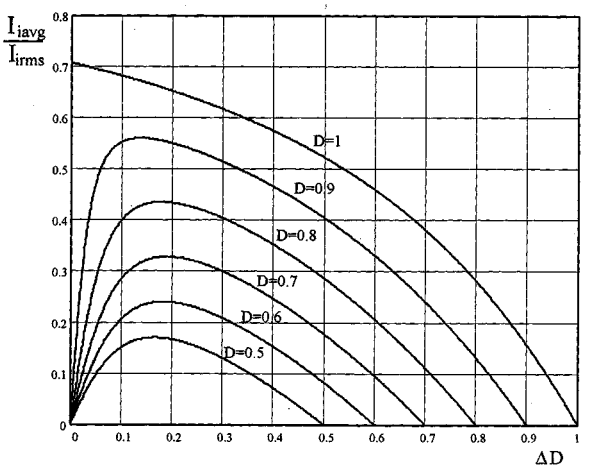

Fig. 6. Average and rms input current ratio.

In no-load condition ($I_o = 0$), the charge and discharge currents of commutation capacitors C_{r1} and C_{r2}, are given by (20)

$$I_{\rm com} = \frac{V_i \cdot D_{\rm min} \cdot (1 - D_{\rm min})}{4 \cdot L_r \cdot f_s \cdot (2 - D_{\rm min})}. \tag{20}$$

From (9), the minimum duty cycle is

$$D_{\rm min} = \frac{4 \cdot V_o}{n \cdot V_i + 2 \cdot V_o}. \tag{21}$$

In the proposed converter, $I_{\rm com}$ permits to charge and discharge the commutation capacitors in no-load condition. Therefore, ZVS commutation of the auxiliary and principal switches is guaranteed. The converter presents such features due to the magnetic coupling of the forward converters using a single transformer.

D. Relevant Design Curves

In Fig. 6, the ratio between the average and the rms input currents, as a function of the duty cycle reduction, is represented, for one forward converter. For a given duty cycle, the maximum point of the curve represents the smallest amount of reactive energy circulating in the primary side of the transformer. In practice, once a maximum duty cycle is assumed, the corresponding curve provides the reduction, ΔD.

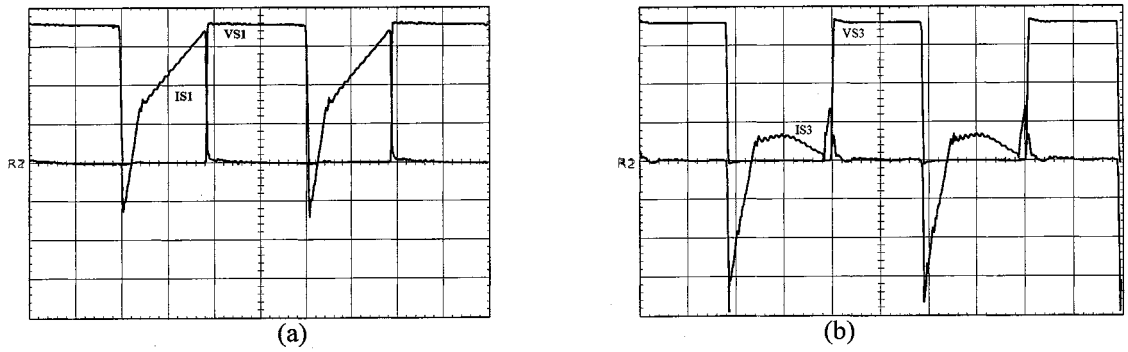

Fig. 7. Voltage and current waveforms in full-load condition: (a) main switch S_1 (scales: 100 V/div., 10 A/div., 10 us/div.), (b) auxiliary switch S_3 (scales: 100 V/div., 10 A/div., 10 us/div.).

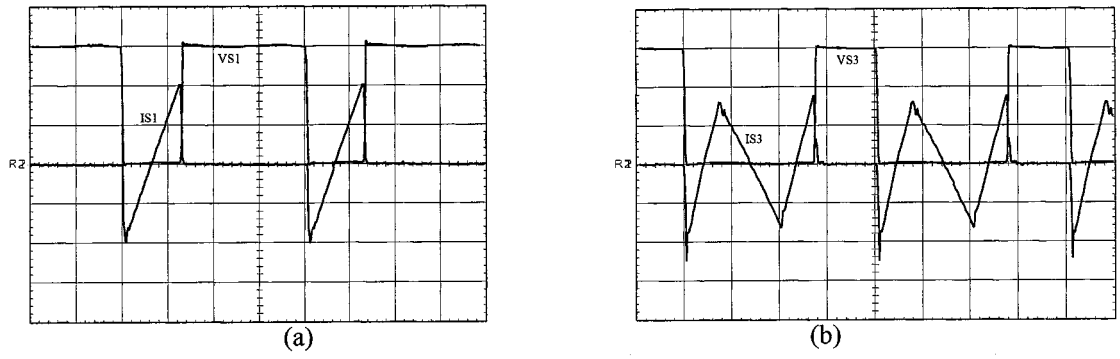

Fig. 8. Voltage and current waveforms in no-load condition: (a) main switch S_1 (scales: 100 V/div., 10 A/div., 10 us/div.), (b) auxiliary switch S_3 (scales: 100 V/div., 10 A/div., 10 us/div.).

IV. Simplified Design Example

A methodology and design procedure is presented in this section.

A. Input Data

$V_i = 200$ V	(input voltage)
$V_o = 60$ V	(output voltage)
$I_o = 50$ A	(output current)
$P_o = 3$ kW	(output power)
$f_s = 25$ kHz	(switching frequency).

B. Design of the Passive Components

Assuming ideal switches, ideal diodes and maximum duty cycle $D_{\max} = 0.8$, the maximum duty cycle reduction, $\Delta D_{\max}$, is obtained from Fig. 6. Therefore

$$\Delta D_{\max} = 0.18.$$

The transformer turns ratio is calculated from (9) as follows:

$$n = \frac{N_S}{N_P} = \frac{2 \cdot (2 - D_{\max})}{(D_{\max} - \Delta D_{\max})} \cdot \frac{V_o}{V_i} = 1.16.$$

The clamping voltage is calculated from (3) as follows:

$$V_{Cc} = \frac{2}{(2 - D_{\max})} \cdot V_i = 333.34 \text{ V}.$$

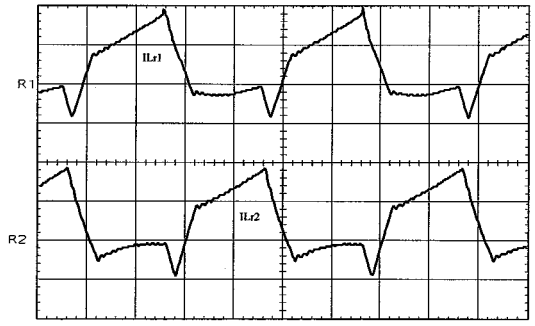

Fig. 9. Currents through inductors L_{r1} and L_{r2} in full-load condition (scales: 20 A/div., 10 us/div.).

1) Commutation Inductors L_{r1} and L_{r2}: Once the value of $\Delta D_{\max}$ is known, the inductance can be calculated from (8) as follows:

$$L_{r1} = L_{r2} = \frac{V_i \cdot \Delta D_{\max}}{f_s \cdot n \cdot I_o \cdot (2 - D_{\max})} = 20.7 \ \mu\text{H}.$$

2) Clamping Capacitors C_{c1} and C_{c2}: To determine the capacitance, the resonance period of the clamping capacitor and commutation inductor is considered correspondent to three times the switching period, T_s. Therefore

$$2 \cdot \pi \cdot \sqrt{L_r \cdot C_{c1}} = 3 \cdot T_s$$

$$C_{c1} = C_{c2} = \frac{2.25}{\pi^2 \cdot L_r \cdot f_s^2} = 17.6 \ \mu\text{F}.$$

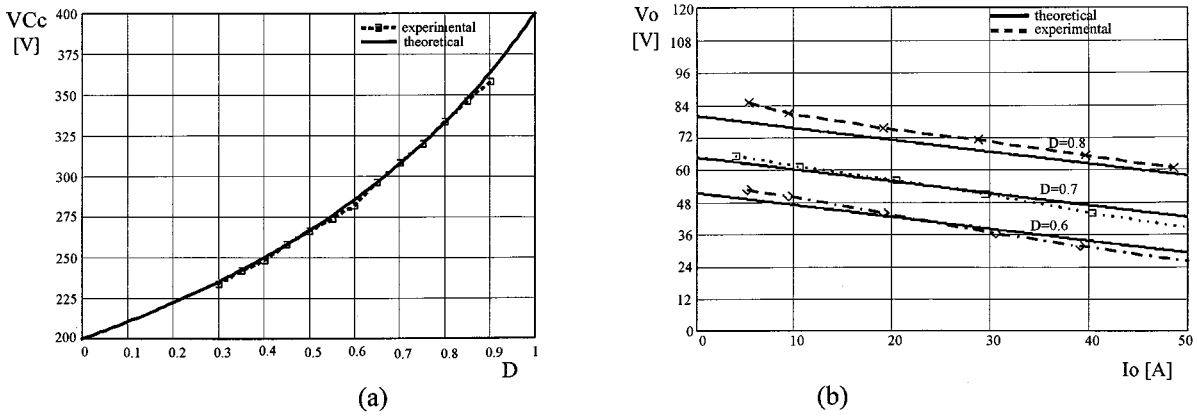

Fig. 10. Experimental curves of (a) clamping characteristic and (b) output characteristic.

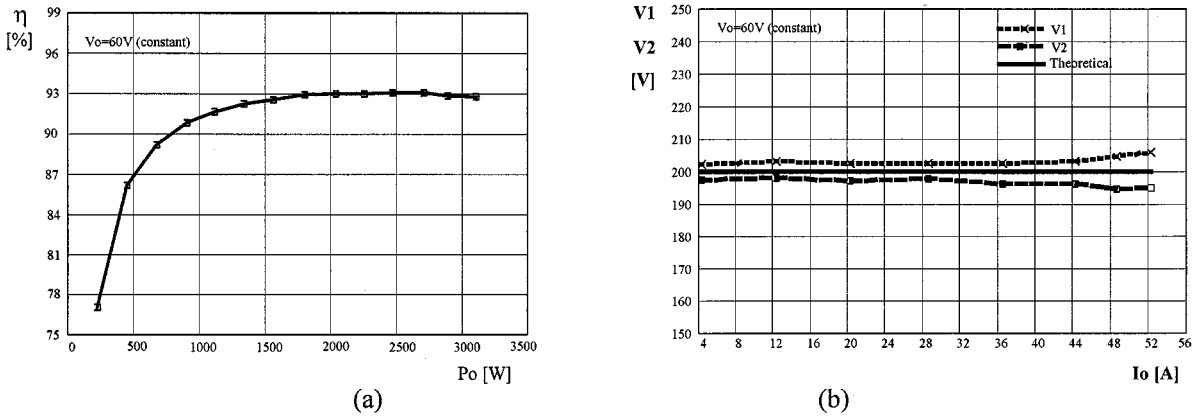

Fig. 11. Experimental curves of (a) measured efficiency of the converter and (b) voltages across input capacitors C_1 and C_2.

3) Commutation Capacitors C_{r1} and C_{r2}: To design C_{r1} and C_{r2}, the minimum duty cycle, $D_{\min}$, and an assumed commutation time interval, during turn-on or turn-off, are required. At no-load, usually a critical situation, the currents during turn-on and turn-off are approximately of the same value. Therefore, either turn-on or turn-off commutation analysis can be used to determine the resonant capacitance. From expression (21) the minimum duty cycle, $D_{\min} = 0.68$, is obtained.

From (19) taking the commutation time interval equal to 1% of $T_s(t_{\text{off}} = 400 \cdot 10^{-9}\ s)$, the normalized commutation time interval is calculated as follows

$$\overline{t_{\text{off}}} = \frac{t_{\text{off}}}{T_s} = 0.01.$$

Using the curves of Fig. 5 and taking $D \cong 0.7$ as a parameter, the normalized frequency is $\overline{f} = 0.104$.

From (11), the resonant frequency, f_o, is

$$f_o = \frac{f_s}{\overline{f}} = 240.4 \text{ kHz}.$$

Finally, from (13) capacitance C_{r1} is obtained:

$$C_{r1} = C_{r2} = \frac{1}{L_r \cdot (2 \cdot \pi \cdot f_o)^2} = 21.2 \text{ nF}.$$

4) Output Filter: This filter is designed for a maximum inductor current ripple $\Delta I_{Lo1} = 10$ A (20% of I_o) and a maximum voltage ripple $\Delta V_o = 0.48$ (0.8% of V_o) across the output capacitor, C_o. The values are

$$L_{o1} = L_{o2} = \frac{2 \cdot V_o \cdot (1 - D_{\min})}{f_S \cdot \Delta I_{Lo}} = 153.6\ \mu\text{H}$$

$$C_o = \frac{\Delta I_{Lo1}}{4 \cdot \pi \cdot f_S \cdot \Delta V_o} = 66.3\ \mu\text{F}.$$

The maximum allowable series resistance for the output capacitor, C_o, must be

$$R_{SE} = \frac{2 \cdot \Delta V_o}{\Delta I_{Lo1}} = 0.096\ \Omega.$$

V. Experimental Results

To verify the practical aspects of the proposed converter, a prototype of 3 kW was built in laboratory. The experimental results obtained from prototype are described as follows.

In this section, experimental waveforms obtained for 3 kW and for 0 W output power are presented.

The waveforms obtained for $P_o = 3$ kW are shown in Fig. 7, and those concerning $P_o = 0$ W are shown in Fig. 8. These results confirm the soft commutation of the switches.

The currents flowing through L_{r1} and L_{r2} are shown in Fig. 9. The clamping characteristic, the output characteristic and the efficiency of the converter are shown in Figs. 10 and

11(a), respectively. These experimental waveforms confirm the theoretical predictions.

In Fig. 11(b) are shown voltages across the input capacitors. The theoretical value of these voltages is $V_i = 200$ V. In the prototype, a maximum unbalance of 5 V is observed, which represents 2.5% of V_i.

VI. Conclusions

A dc–dc converter for high input bus voltage application based on two single ZVS-PWM active-clamping forward converters was proposed in the paper. Analyzes of the clamping process, of the output characteristic, and of the commutation characteristic along with a simplified design example and experimental results were presented.

Experimental results show that the converter presents the following features.

1) Soft commutation of all the controlled switches for any load current.
2) Only two switches, S_1 and S_2, control the power flow from the input to the output causing low conduction losses of the converter. The current flowing through auxiliary switches S_3 and S_4 is very low.
3) Voltage overshoots across the switches caused by energy stored in transformer leakage inductances are eliminated with the use of active clamping circuits.
4) A good distribution of currents through the coupled circuits is observed.
5) A good voltage division among the input capacitors is observed.
6) The efficiency of the converter is 92.8% in full load.

References

[1] T. S. Key and J. S. Lai, "IEEE and international harmonic standards impact on power electronic design," in *Proc. Virginia Power Electron. Sem. (VPEC)*, 1998, pp. 39–45.

[2] E. Deschamps and I. Barbi, "A new DC-to-DC ZVS PWM converter for high input voltage applications," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, 1998, pp. 967–972.

[3] M. Miller, A. Buffin, and U. Carlsson, "High frequency ZVS for high power rectifiers," in *Proc. Int. Telecommun. Energy Conf. (INTELEC)*, 1993, pp. 424–430.

[4] N. Kutkut, G. Luckjitt, and D. Divan, "A dual bridge high current DC-to-DC converter with soft switching capability," in *Proc. IEEE Ind. Applicat. Soc. (IAS) Conf.*, 1997, pp. 1398–1405.

[5] B. Carsten, "Design techniques for transformers active reset circuits at high frequencies and power levels," in *Proc. High Freq. Power Conv. (HFPC) Conf.*, 1990, pp. 235–246.

[6] C. M. C. Duarte and I. Barbi, "A family of ZVS-PWM active-clamping DC-to-DC converters: Synthesis, analysis, design, and experimentation," *IEEE Trans. Circuits Syst.*, vol. 44, pp. 698–704, Aug. 1997.

[7] R. T. Bascopé and I. Barbi, "A double ZVS-PWM active-clamping forward converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 1999, pp. 596–601.

[8] P. Imbertson and N. Mohan, "Asymmetrical duty cycle permits zero switching loss in PWM circuits with no conduction loss penalty," in *Proc. IEEE Ind. Applicat. Soc. Annu. Meeting (IAS)*, 1991, pp. 1061–1066.

[9] R. Watson, F. C. Lee, and G. C. Hua, "Utilization of an active-clamp circuit to achieve soft switching in flyback converters," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, 1994, pp. 909–916.

[10] I. D. Jitaru, "Constant frequency, forward converter with resonant transition," in *Proc. High Freq. Power Conv. (HFPC) Conf.*, 1991, pp. 282–292.

René Torrico-Bascopé (M'00) was born in Cochabamba, Bolivia, in 1967. He received the B.Eng. degree from San Simón University of Cochabamba, Bolivia, in 1992, and the M.Eng. and Dr.Eng. degrees from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1994 and 2000, respectively.

During 1995 and 1996, he was Research Engineer in the Power Electronics Institute, Federal University of Santa Catarina. Since March 2001, he has been an Assistant Professor at the Univali University of Itajaí, Santa Catarina, Brazil. His main interests include telecommunication power supplies, power factor correction techniques, and no-break systems.

Ivo Barbi (SM'79) was born in Gaspar, Santa Catarina, Brazil in 1949. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1973 and 1976, respectively, and the Dr.Ing. degree from the Institut National Polytechnique de Toulouse, France, in 1979.

He founded the Brazilian Power Electronics Society, the Power Electronics Institute, Federal University of Santa Catarina, and created the Brazilian Power Electronics Conference. Currently, he is a Professor of the Power Electronics Institute, Federal University of Santa Catarina.

Dr. Barbi has been an Associate Editor in the Power Converters Area of the IEEE Transactions on Industrial Electronics since January 1992.