Isolated DC-DC Converters With High-Output Voltage for TWTA Telecommunication Satellite Applications

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***Abstract*—Two alternatives for the implementation of an isolated dc-dc converter operating with a high output voltage and supplied by an unregulated low input voltage are presented in this paper. The proposed topologies are especially qualified for the implementation of travelling wave tube amplifiers (TWTA) utilized in telecommunication satellite applications due to their low mass and volume and their high-efficiency.**

The converters studied follow different principles and the main operational aspects of each topology are analyzed.

A two-stage structure composed by a regulator connected in series with a ZVS/ZCS isolated dc-dc converter is the first topology proposed.

The second topology studied is an isolated single-stage converter that continues being highly efficient even with a large input voltage variation.

The experimental results obtained from two prototypes, implemented following the design procedures developed, are presented, verifying experimentally the characteristics and the analysis of the proposed structures.

The prototypes are developed for an application requiring an output power of 150 W, a total output voltage of 3.2 kV and an input voltage varying from 26 V to 44 V. The minimum efficiency obtained for both converters operating at the nominal output power, is equal to 93.4% for the two-stage structure and equal to 94.1% for the single-stage converter.

***Index Terms*—Active clamping, communication satellite, electronic power conditioner, high efficiency, travelling wave tube amplifier.**

I. Introduction

THERE are different applications where the use of high level dc voltages (thousands of volts) is necessary. Typical examples are CO_2 laser-based systems, medical and industrial x-rays and telecommunications equipments with travelling wave tube (TWT), utilized in communication satellites. Therefore, several high-voltage dc–dc switching power converters are used in different types of electronic equipments. The designer of high voltage power supplies faces many problems that are not present in low voltage designs, and the choosing the most adequate solution depends on the design requirements of each specific application.

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The design difficulty of high-voltage converters is increased in satellite applications due to the severe requirements and specifications that must be attended. The launch cost is very high and there is a permanent interest in efficiency improvement and in the reduction of the mass and volume of the satellite's equipment. High efficiency is important, especially since the primary power source of a satellite is a solar array and batteries, which contributes significantly to the total mass, volume and cost of the satellite.

The final stage amplifier in the transponder of the communication satellite is the travelling wave tube amplifier (TWTA). In this kind of satellite, the payload mass and power consumption is mainly given by the presence of the TWTA, which represents about 35% of the total mass and 70% to 90% of the overall dc power consumption [1]. Therefore, the design of the TWTA has been continuously improved in order to realize lighter and more efficient equipment.

The TWTA consists of a microwave amplifier tube (TWT), which mainly determines the radio frequency (RF) performance, and an electronic power conditioner (EPC) for power matching the dc interface. The high voltage dc–dc converter can be considered the most important part of the EPC because it is the critical point in the design of a high efficiency and competitive TWTA.

II. High-Voltage Isolated DC–DC Converters

The operation of the isolated converter is influenced by the presence of the intrinsic elements of the power transformer. In low-voltage applications, the power transformer can be represented by its magnetizing and leakage inductances, when considering its operation without losses. However, in a step-up transformer for high-voltage applications, there is also an equivalent winding capacitance, referred to the primary side, that must be included in the transformer's equivalent model. Due to the high number of turns in the secondary winding and the high transformer turns ratio, this equivalent capacitance becomes important in the converter's operation.

Fig. 1 presents the simplified high-voltage transformer model constituted by the leakage inductance $(L_{\rm d})$, the magnetizing inductance $(L_{\rm m})$ and the equivalent capacitance referred to the primary side $(C_{\rm p})$ [1]–[3].

This model is adopted in the analyzes of the operation principles of the two proposed topologies.

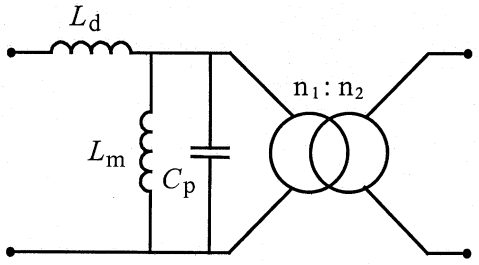

Fig. 1. Simplified equivalent circuit of the high voltage and high frequency transformer.

There are some operational characteristics that an isolated topology must present for its utilization in high output voltage applications, in order to maintain high efficiency, low volume and mass. The main operational characteristics are:

1) high switching frequency, reducing the reactive elements, such as inductors, filter capacitors and the power transformer;
2) soft-commutation in the power switches, avoiding an efficiency reduction due to the increment of the switching frequency;
3) incorporation of the intrinsic elements of the circuit in the converter's operation, like the switch capacitance, the leakage inductance and the equivalent capacitance of the high-voltage transformer, thus avoiding the dissipation of the energy stored in these elements;
4) constant switching frequency, allowing to choose the optimum switching frequency with respect to the mass, volume and efficiency;
5) voltage source output characteristic, because the multiple high-voltage outputs necessary to supply the TWT makes the utilization of output filter inductors in the high-voltage session unfeasible, in order to obtain a current source output characteristic;
6) input current source behavior, because the nonpulsating input current allows the input filter to be reduced;
7) a step-up output characteristic, reducing the transformer's turns ratio and minimizing the effects of the transformer equivalent capacitance referred to the transformer's primary side;
8) good load regulation and operation with a large input voltage variation;
9) low di/dt in the high-voltage rectifier diodes, minimizing the effects of the recovery current of these diodes.

Considering as criteria for choosing the isolated converters, all of the operational characteristics presented above, two topologies were selected and studied for the implementation of a TWTA.

III. Two-Stage Topology

The input voltage presents a large variation range and the first solution proposed for the implementation of the TWTA power stage is composed of two dc-dc converters connected in series (two-stage topology), presented in Fig. 2.

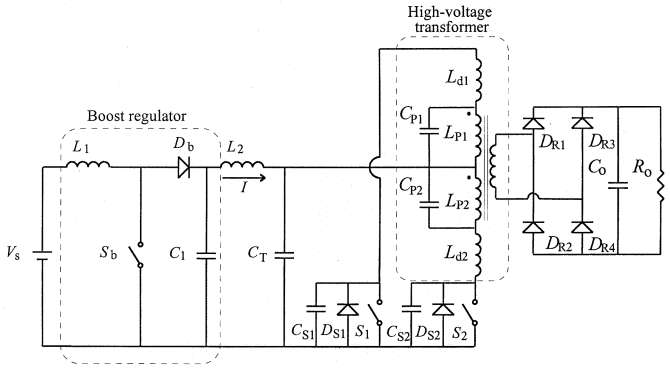

Fig. 2. Proposed power circuit of the two-stage topology.

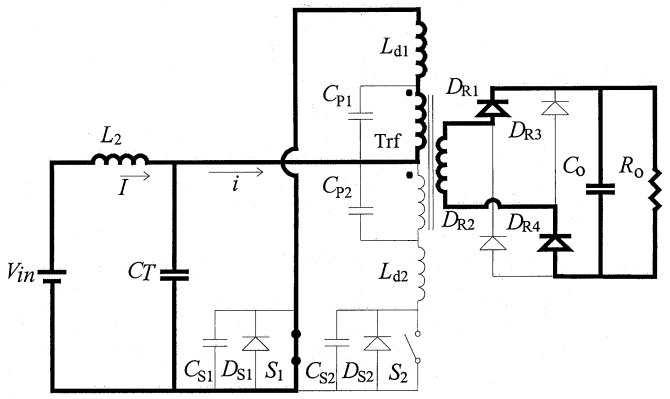

Fig. 3. First operation stage $(t_o - t_1)$.

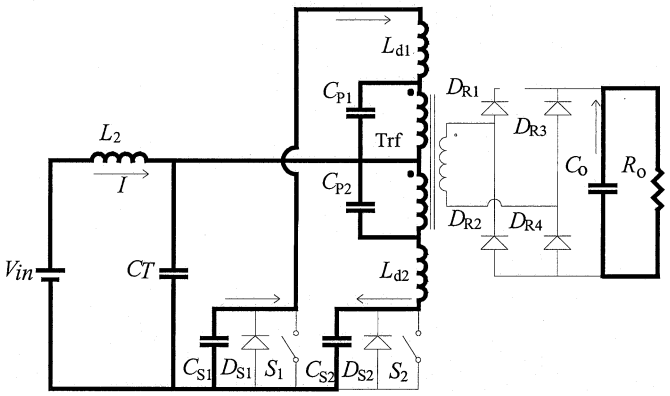

Fig. 4. Second operation stage $(t_1 - t_2)$.

A. Proposed Circuit

The first converter of the two-stage structure is a boost dc-dc converter composed of input inductor L_1, power switch S_b, diode D_b and filter capacitor C_1. The boost converter regulates the input voltage variations and operates with PWM modulation and hard switching. However, operating at a low input voltage and using a schottky diode in the boost output, it is possible to reach high-efficiency operating at a high switching frequency (see Figs. 3 and 4).

The second stage is an isolated dc-dc converter with a resonant operation, generating the different high voltage outputs to supply the TWT [4]. In this case, the isolated dc-dc converter operates in at an optimized operation point, with a con-

stant switching frequency and a fixed duty-ratio. The isolated topology is a resonant push-pull current fed dc-dc converter composed by two power switches (S_1 and S_2), an input inductor (L_2), a resonant capacitor ($C_{\rm T}$) and the push-pull transformer. The intrinsic parameters of the transformer ($L_{\rm d1}$, $L_{\rm d2}$, $C_{\rm p1}$ and $C_{\rm p2}$) are also presented in Fig. 2.

A full-bridge rectifier and a filter capacitor compose the output.

The push-pull converter operates with zero current and zero voltage switching techniques (ZCS/ZVS). The input current source characteristic of the push-pull converter is obtained by way of inductor L_2.

B. Operation Principles

The push-pull ZVS/ZCS operation principle can be described in the two operation stages presented below. To simplify the analysis, the components are considered ideal, however the switch capacitance, the leakage inductance and the equivalent capacitance of the high-voltage transformer are included in this analysis.

The output voltage of the boost regulator is substituted by a constant voltage source $V_{\rm in}$.

1) First Operation Stage $(t_o - t_1)$*:* The current in the transformer center tap (i) is initially zero and during the conduction of switch $\rm S_1$, resonance between center tap capacitance $C_{\rm T}$ and leakage inductance $L_{\rm d1}$ occurs. The current (i) increases, reaches its maximum value and drops to zero, finishing this operation stage.

During this stage, the center tap current (i) flows through the filter capacitor and the load, by way of the transformer's windings and rectifier diodes $D_{\rm R1}$ and $D_{\rm R4}$.

2) Second Operation Stage $(t_1 - t_2)$*:* When the current in switch S_1 becomes zero, the rectifier diode is blocked and the energy stored in the magnetizing inductance is transferred to the switch capacitance and the equivalent capacitance of the high-voltage transformer. The voltage in the equivalent capacitance of the circuit changes in a resonant way and switch S_2 turns-on with soft-commutation.

The main theoretical waveforms of the isolated converter are presented in Fig. 5. The commutation loss in the power switches is very low. The maximum voltage across the switches is equal to two times the push-pull input voltage (boost output voltage) plus the voltage ripple in the center tap capacitor $C_{\rm T}$. Therefore, this converter is indicated for low input voltage applications.

C. Main Mathematical Results and Simplified Design Procedure

The main mathematical results obtained from the theoretical analysis are presented and utilized in a simplified design procedure.

1) Specifications and Parameters: The following specifications are considered in the design of the two-stage topology.

Input voltage	$V_{\rm s} = 26/44$ V.
Boost output voltage	$V_2 = 50$ V.
Total output voltage	$V_{\rm o} = 3200$ V.
Output power	$P_{\rm o} = 150$ W.
Push-pull switching frequency	$F_{\rm s} = 80$ kHz.
Boost switching frequency	$F_{\rm b} = 120$ kHz.

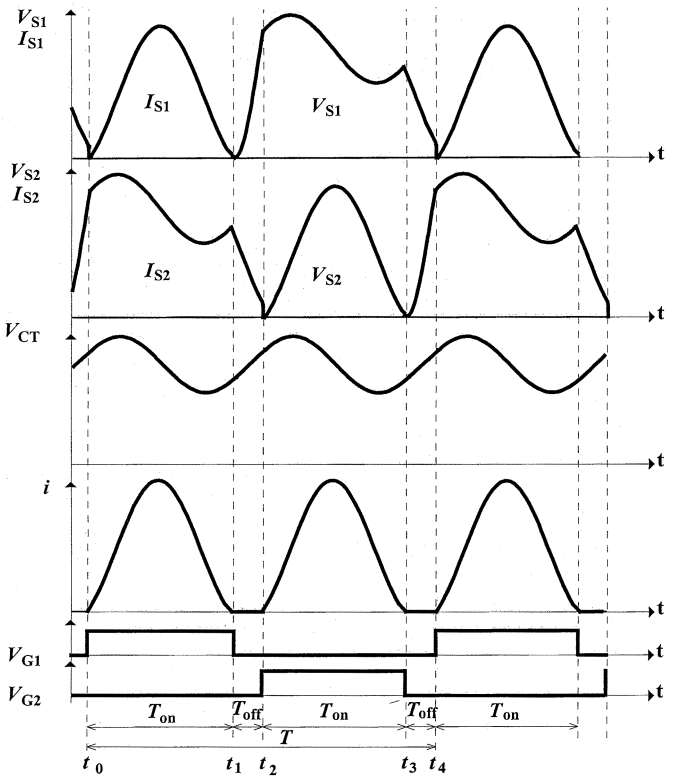

Fig. 5. Main theoretical waveforms.

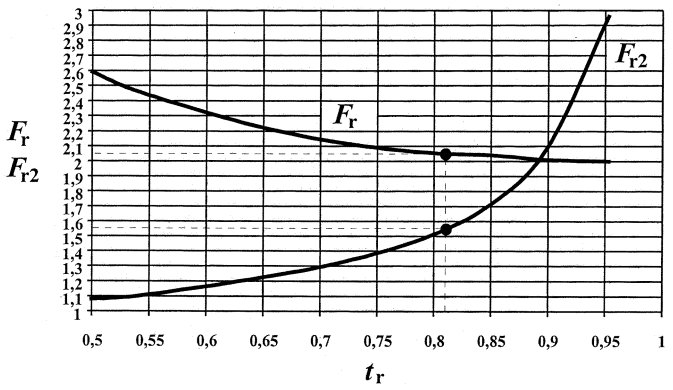

Fig. 6. Optimized operation point.

The parameters of the implemented circuit are as follows.

Magnetizing inductance with gap	$L_{\rm m} = 85\ \mu$H.
Leakage inductance	$L_{\rm d} = 1.3\ \mu$H.
Winding capacitance	$C_{\rm p} = 8.75$ nF.
Switch capacitance	$C_{\rm s} = 1$ nF.

2) Operation Point of the Push-Pull Converter: The switch current must be zero at the end of period $T_{\rm on}$ (Fig. 5, instant $\rm t_1$) and the voltage across the switch that will be turned-on must reach a low value at the end of period $T_{\rm off}$ (Fig. 5, instant $\rm t_2$) for the push-pull converter to operate optimally. These two conditions are defined mathematically by (1) and (2), respectively. The design procedure is simplified by solving (1) and (2) numerically, and the results obtained are plotted in Fig. 6

$$\cos(\pi \cdot F_r \cdot t_r) - \frac{\pi \cdot F_r \cdot (1 - t_r)}{2} \cdot sin(\pi \cdot F_r \cdot t_r) - 1 = 0 \qquad (1)$$

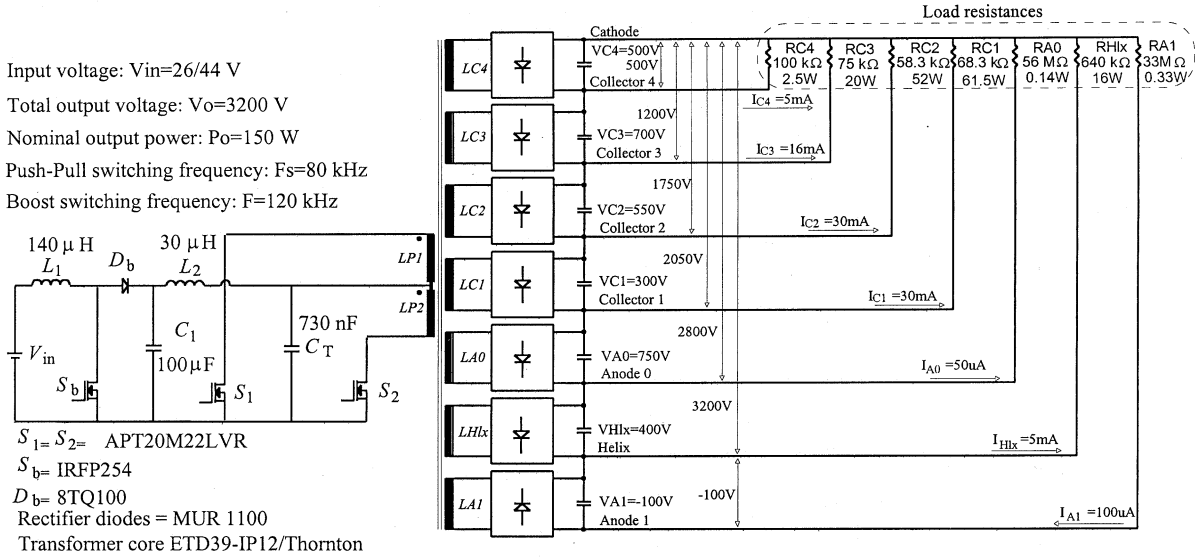

Fig. 7. Implemented two-stage power circuit.

$$2 \cdot \cos(\pi \cdot F_{r2} \cdot (1 - tr)) - \pi \cdot F_{r2} \cdot tr \cdot sin(\pi \cdot F_{r2} \cdot (1 - tr)) + 2 = 0 \quad (2)$$

where

$$t_r = \frac{2 \cdot T_{on}}{T} \quad (3)$$

$$F_r = \frac{1}{2 \cdot \pi \cdot \sqrt{L_d \cdot C_T}} \cdot \frac{1}{F_s} \quad (4)$$

$$F_{r2} = \frac{1}{2 \cdot \pi \cdot \sqrt{2 \cdot L_m \cdot C_{eq}}} \cdot \frac{1}{F_s}. \quad (5)$$

The relative frequency $F_{\rm r}$, is the relationship between the resonance frequency of the leakage inductance and the center tap capacitance, and the switching frequency. This resonance occurs during the conduction of the power switch. $F_{\rm r2}$ is the relationship between the resonant frequency of the magnetizing inductance and equivalent circuit capacitance, and the switching frequency. This resonance occurs when both switches are turned off.

Substituting the specifications and parameters in (7) yields

$$C_{eq} = C_{s1} + C_{p1} \quad (6)$$

$$F_{r2} = \frac{1}{2 \cdot \pi \cdot \sqrt{2 \cdot L_m \cdot C_{eq}}} \cdot \frac{1}{F_s} = 1,5453. \quad (7)$$

The frequency $F_{\rm r2}$ calculated must be higher than 1.1 to obtain soft-commutation. The components' stresses are reduced for a relative frequency $F_{\rm r}$ close to 2, and a relative conduction time $t_{\rm r}$ close to 1. The energy stored in the magnetizing inductance causes the voltage transitions in the equivalent circuit capacitance. Therefore, the magnetizing inductance can be reduced by inserting a gap in the transformer, which permits choosing a good operation point.

With the relative frequency $F_{\rm r2}$ calculated, the value of the switch conduction time $(t_{\rm r})$ is defined by the use of Fig. 6

$$t_{\rm r} = 0.81.$$

The switch turn-on and turn-off periods are calculated by

$$T_{on} = \frac{t_r}{2 \cdot F_s} = 5\ \mu{\rm s} \quad (8)$$

$$T_{\rm off} = \frac{T}{2} - T_{\rm on} = 1.25\ \mu{\rm s}. \quad (9)$$

3) Center Tap Capacitance $(C_{\rm T})$: Fig. 6 also defines the relative frequency $F_{\rm r}$

$$F_{\rm r} = 2.05 \quad (10)$$

$$F_o = F_s \cdot F_r = 164\ kHz \quad (11)$$

$$\omega_o = 2 \cdot \pi \cdot F_o. \quad (12)$$

The center tap capacitance can be calculated by

$$C_T = \frac{1}{L_d \cdot {\omega_o}^2} = 724\ nF. \quad (13)$$

4) Current and Voltage Stresses: The input current (I) is defined by (14), considering an efficiency of $\eta = 95\%$

$$I = \frac{P_o}{V_2 \cdot \eta} = 3.158\ A. \quad (14)$$

The switch peak current $(I_{\rm pk})$ is calculated by

$$\varphi = a\tan\ g\left(\frac{\pi \cdot F_r \cdot (1 - t_r)}{2}\right) = 0.549 \quad (15)$$

$$I_{pk} = I \cdot \left[1 + \frac{1}{\cos(\varphi)}\right] = 6.86\ A. \quad (16)$$

The switch rms current is

$$i_{Srms} = \sqrt{\frac{I_{pk} \cdot t_r}{4}} = 3.09\ A. \quad (17)$$

The maximum blocking voltage across the switch $(V_{\rm Spk})$ is

$$Zn = \sqrt{\frac{L_d}{C_T}} = 1.34 \quad (18)$$

$$V_{Spk} = \frac{I \cdot Zn}{\cos(\varphi)} + 2 \cdot V_2 = 105\ V. \quad (19)$$

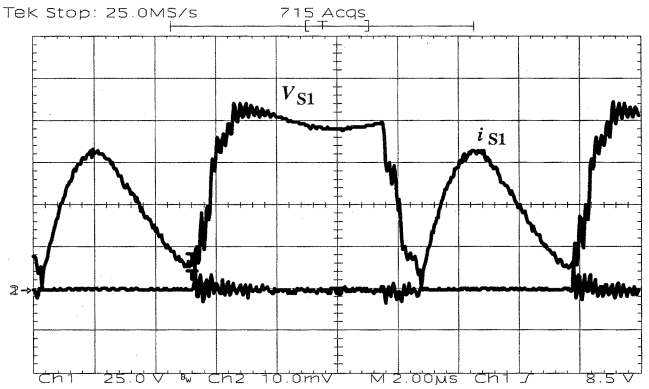

Fig. 8. Power switch voltage and current (25 V/2 A/2 μs/div).

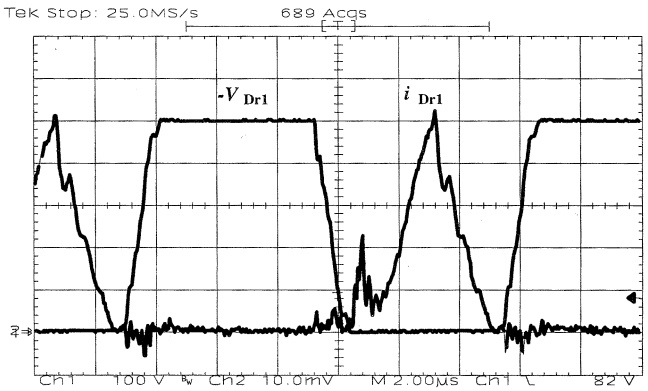

Fig. 9. Rectifier diode voltage and current (100 V/50 mA/2 μs/div).

5) Output Voltage Ripple: The parameterized output voltage ripple is calculated by

$$\delta = a\tan\ g\left(\frac{\pi \cdot F_r \cdot (1 - t_r)}{2}\right) \tag{20}$$

$$\overline{\Delta V} = \frac{\Delta V_{Co} \cdot C_o \cdot F_s}{I_o} = \frac{1}{\pi} \cdot \frac{2}{F_r \cdot \cos(\delta)} \tag{21}$$

where

I_o average current of each output;
C_o filter capacitor;
ΔV_{Co} output voltage ripple;

D. Experimental Results

A laboratory prototype was implemented following the optimized design procedure developed. Some waveforms obtained from this prototype, operating at a minimal input voltage and nominal output power, are presented. The details regarding the power circuit implemented are shown in Fig. 7. A typical configuration of load resistance representing the TWT, for testing of the power supply was used. The different current and voltage levels in each output and the nominal output power are defined by the kind of TWT adopted in the design.

The main experimental results of the push-pull converter operating with nominal output power are presented in Figs. 8 and 9.

Fig. 8 presents the soft-commutation obtained in the power switch of the push-pull converter. The peak voltage is about 120 V.

Fig. 9 shows the voltage and current in a high-voltage rectifier diode of the push-pull.

The efficiency curve of the two-stage topology (boost and Push-pull) operating with nominal output power and variable input voltage is presented in Fig. 10. The lowest efficiency obtained, with nominal output power, is equal to 93.4%.

IV. Single Stage Topology

A critical point in the utilization of the two-stage topology is the converter series connection that causes a reduction of the overall efficiency. Both converters must present very high efficiency in order to maintain an adequate efficiency for satellite communication applications.

The second solution proposed for the implementation of a competitive TWTA is a high-efficiency single-stage converter. The isolated dc-dc converter operates with a variable operation

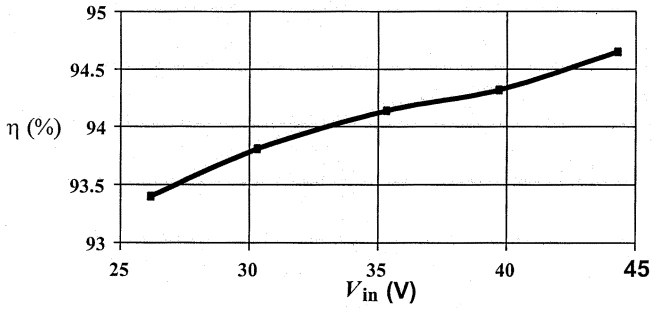

Fig. 10. Efficiency curve, when operating with nominal output power and variable input voltage.

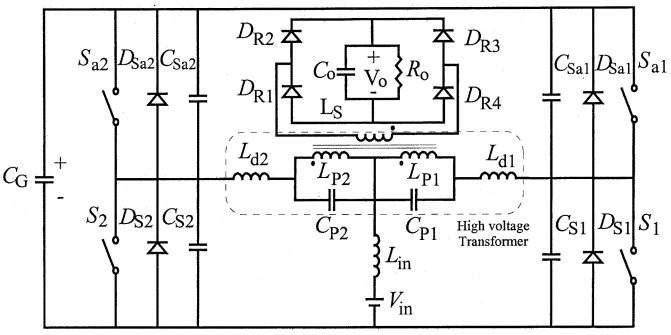

Fig. 11. Proposed power circuit of the single-stage topology.

point (nonoptimum) due to the regulation action of the converter. Thus, the single stage topology must present all of the suitable operation characteristics for high-voltage applications described in Section II and maintain a high efficiency in the range of the input voltage variation.

A. Proposed Circuit

The proposed topology, presented in Fig. 11, is based on the current-fed push-pull dc-dc converter operating with PWM modulation, active clamping and ZVS commutation [5].

Two main switches (S_1 and S_2), two auxiliary clamping switches (S_{a1} and S_{a2}), a clamping capacitor (C_G) and a push-pull transformer composes the converter. The outputs are formed by full-bridge rectifiers and filter capacitors.

The anti-parallel diode and intrinsic capacitance of the MOSFET are used in the circuit operation. The current source input is provided by the voltage source V_{in}, in series with the

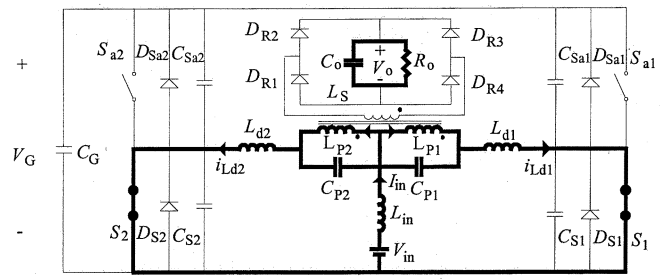

Fig. 12. First operation stage (t_o, t_1).

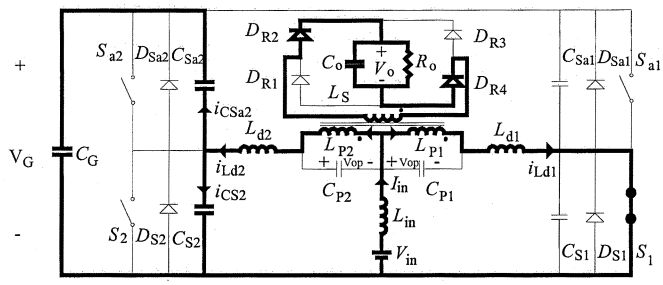

Fig. 13. Second operation stage (t_1, t_2).

input inductor $L_{\rm in}$. The intrinsic parameters of the transformer are also presented in Fig. 11.

B. Operation Principles

Only operation in continuous conduction mode and with a main switch duty ratio (D) higher than 0.5 is considered in this theoretical analysis (boost operation). The converter duty ratio (d) is defined by the period which both main switches are simultaneously conducting in the switching period.

The seven sequential circuit states that describe the operation principles are presented below:

1) First Stage ([t_o, t_1] Fig. 12): Both main switches are conducting and the currents flowing through the primary windings have the same absolute value and opposite direction. Thus, the rectifier diodes are blocked and input inductor $L_{\rm in}$ stores energy. The resonance between the leakage inductance and the parasitic capacitance of the transformer occurs during this stage but does not influence the operation of the converter.

2) Second Stage ([t_1, t_2] Fig. 13): At instant $\rm t_1$, switch $\rm S_2$ is turned off at zero voltage and the charge and discharge of capacitors $\rm C_{S2}$ and $\rm C_{Sa2}$ occur linearly with a constant current. When the currents in the primary windings become different, the power is transferred from the input source to the load. This stage finishes when $V_{\rm CSa2}(\rm t) = 0$.

3) Third Stage ([t_2, t_3] Fig. 14): The voltage across $\rm C_{Sa2}$ drops to zero and diode $\rm D_{Sa2}$ discharge the energy stored in the leakage inductance to the clamping capacitor. The auxiliary switch $S_{\rm a2}$ must be enabled to conduct during the conduction of diode $D_{\rm Sa2}$.

4) Fourth Stage ([t_3, t_4] Fig. 15): Current $\rm i_{Ld2}$ inverts its direction and clamping capacitors $C_{\rm G}$ transfers the energy received during the third stage, to the load, by way of $S_{\rm a2}$.

5) Fifth Stage ([t_4, t_5] Fig. 16): Auxiliary switch $\rm S_{a2}$ is turned off. The energy stored in the leakage inductance $L_{\rm d2}$ causes the charge and discharge of capacitors $C_{\rm S2}$ and $C_{\rm Sa2}$ in a resonant way. The voltage in the main switch decreases to zero [6]–[8].

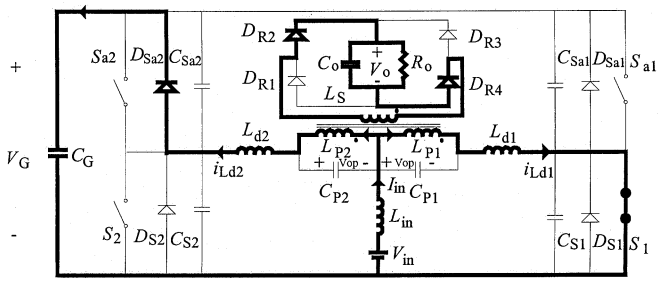

Fig. 14. Third operation stage (t_2, t_3).

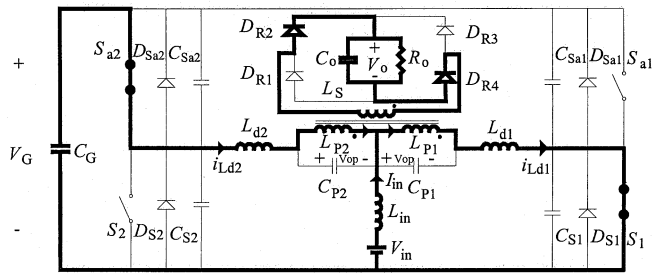

Fig. 15. Fourth operation stage (t_3, t_4).

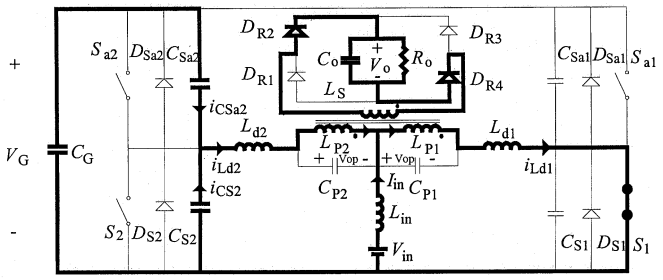

Fig. 16. Fifth operation stage (t_4, t_5).

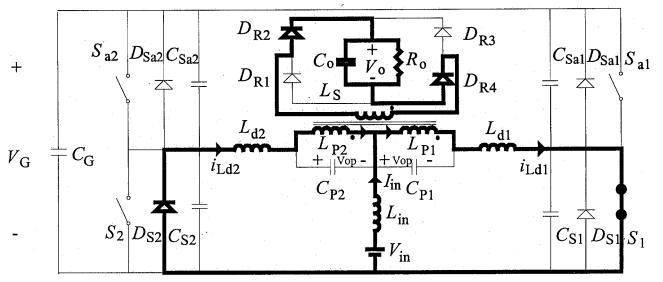

Fig. 17. Sixth operation stage (t_5, t_6).

6) Sixth Stage ([t_5, t_6] Fig. 17): When capacitor $C_{\rm Sa2}$ reaches clamping voltage $V_{\rm G}$, diode $D_{\rm S2}$ starts to conduct and current $i_{\rm Ld2}$ decreases due to the output voltage referred to the primary side $(V_{\rm op})$. The main switch S_2 must be enabled to conduct during the conduction of diode $D_{\rm S2}$.

7) Seventh Stage ([t_6, t_7] Fig. 18): The current flowing through S_2 inverts its direction. When the currents in the primary windings become equal, the rectifier diodes are blocked, thus returning to the first operation stage.

The main theoretical waveforms are presented in Fig. 19.

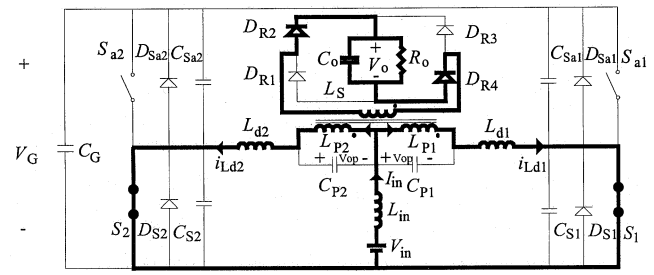

Fig. 18. Seventh operation stage (t_6, t_7).

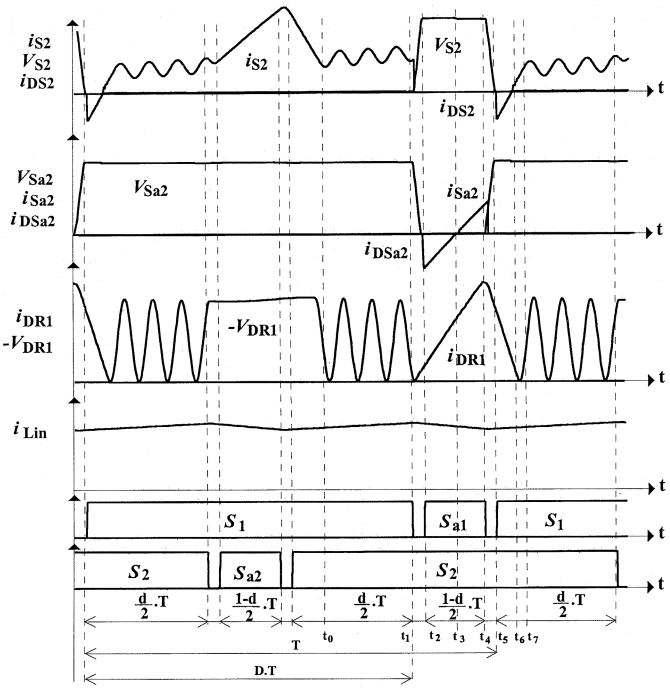

Fig. 19. Main theoretical waveforms.

The active clamping allows operation with soft-commutation in all of the switches until a minimal load, where the energy stored in the leakage inductance is not enough to complete the voltage transitions in the commutation capacitor. The voltage across the blocked switch is limited to the clamping voltage.

An important characteristic of this structure is its operation with a main switch duty-ratio (D) higher than and lower than 0.5 (with overlapping and no overlapping). The auxiliary switches operate in a complementary way in relation with the respective main switch. For a main switch duty-ratio lower than 0.5, the converter operates like a sepic dc-dc converter and with a step-down output characteristic. For operation with a main switch duty-cycle higher than 0.5, the converter operates like an isolated boost converter with a step-up output characteristic. Therefore, this converter does not present inrush current for a progressive variation of the duty-cycle and endures a large input voltage variation.

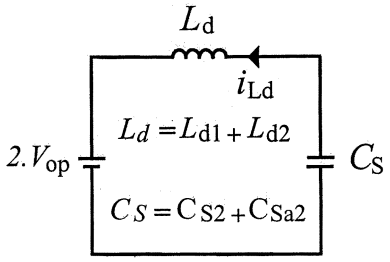

Fig. 20. Equivalent circuit of the auxiliary switch turn-off.

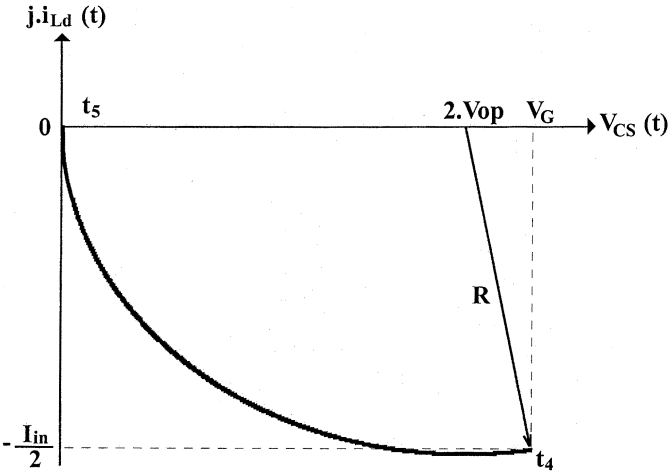

Fig. 21. State plane of the commutation.

C. Main Mathematical Results and Simplified Design Procedure

A simplified design procedure is presented using the main equations obtained from the theoretical analysis of the proposed converter.

1) Specifications and Parameters: The following specifications are considered in the design.

Input voltage	$V_{\rm in} = 26/44$ V.
Total output voltage	$V_{\rm o} = 3200$ V.
Output power	$P_{\rm o} = 150$ W.
Push-pull switching frequency	$F_{\rm s} = 80$ kHz.

The parameters of the implemented circuit are as follows.

Magnetizing inductance	$L_{\rm m} = 85\ \mu$H.
Leakage inductance	$L_{\rm d} = 6\ \mu$H.
Winding capacitance	$C_{\rm p} = 8.75$ nF.

2) Operation Point of the Push-Pull Converter: The output voltage referred to the primary side $(V_{\rm op})$ adopted in the design is equal to 50 V, considering the main switch duty-ratio higher than 0.5 and a step-up output characteristic.

The static gains, operating with minimum and maximum input voltages, are determined, respectively, by

$$q_m = \frac{V_{op}}{Vin_{\min}} = \frac{50}{26} = 1.9231 \tag{22}$$

$$q_x = \frac{V_{op}}{Vin_{\max}} = \frac{50}{44} = 1.1364. \tag{23}$$

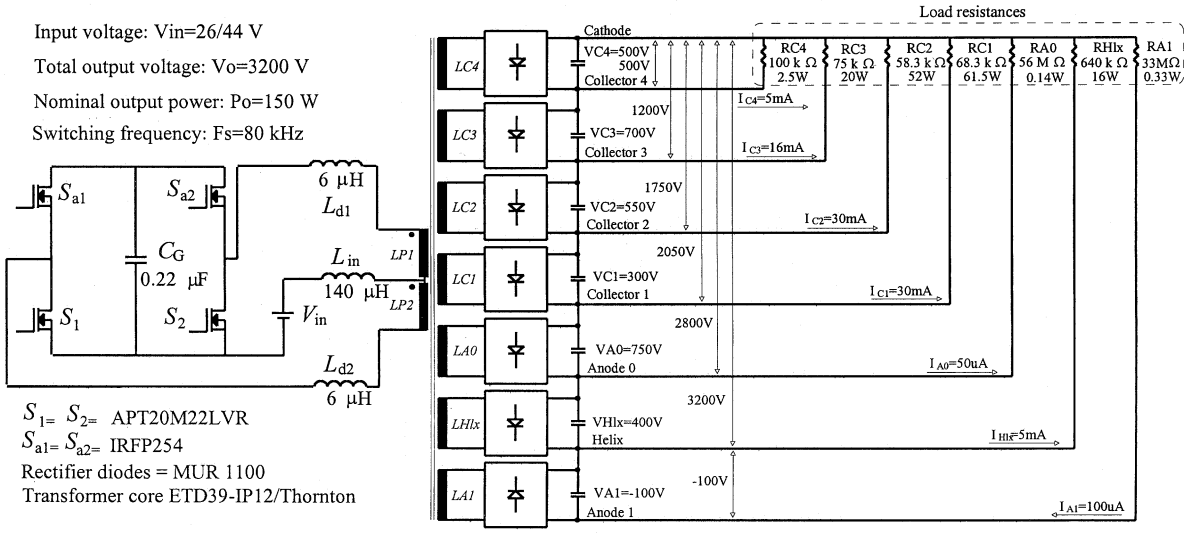

Fig. 22. Implemented single stage power circuit.

The nominal input currents, operating with minimum and maximum input voltages, considering the operation without losses, are

$$Iin_m = \frac{P_o}{Vin_{\min}} = 5.77\ A \tag{24}$$

$$Iin_x = \frac{P_o}{Vin_{\max}} = 3.41\ A. \tag{25}$$

The parameter γ represents a reduction of the effective converter duty ratio due to the presence of the active clamping circuit. This characteristic is common in most ZVS-PWM converters. This parameter is proportional to the leakage inductance and the output current. Considering minimum and maximum input voltages, γ results in

$$\gamma_m = \frac{Iin_m \cdot L_d \cdot F_s}{V_{op}} = 0.08308 \tag{26}$$

$$\gamma_x = \frac{Iin_x \cdot L_d \cdot F_s}{V_{op}} = 0.04909. \tag{27}$$

The nominal converter duty-ratio, for minimum and maximum input voltages are

$$d_m = \frac{q_m + 2 \cdot \gamma_m - 1}{q_m} = 0.646 \tag{28}$$

$$d_x = \frac{q_x + 2 \cdot \gamma_x - 1}{q_x} = 0.218. \tag{29}$$

3) Voltage Stress: The clamping voltages, operating with nominal output power and minimum and maximum input voltages are

$$V_{Gm} = Vin_{\min}\frac{2}{1-d_m} = 147\ V \tag{30}$$

$$V_{Gx} = Vin_{\max}\frac{2}{1-d_x} = 112.5\ V. \tag{31}$$

When the converter operates without a load, the clamping voltage is

$$V_G = 2 \cdot V_{op} = 2 \cdot 50 = 100\ V. \tag{32}$$

Thus, the clamping voltage varies from 100 V until 147 V and this is the maximum blocking voltage across the active switches.

4) Current Stresses Operating With the Minimum Input Voltage: Main switch

$$i_{Srms} = Iin_m \cdot \frac{\sqrt{6}}{12} \cdot \sqrt{15 \cdot \gamma_m + 13 - 7 \cdot d_m} = 3.672\ A. \tag{33}$$

Auxiliary switch

$$i_{Sarms} = Iin_m \cdot \frac{\sqrt{3}}{12} \cdot \sqrt{1 - d_m} = 0.945\ A. \tag{34}$$

5) Current Stresses Operating With the Maximum Input Voltage: Main switch

$$i_{Srms} = Iin_x \cdot \frac{\sqrt{6}}{12} \cdot \sqrt{15 \cdot \gamma_x + 13 - 7 \cdot d_x} = 2.432\ A. \tag{35}$$

Auxiliary switch

$$i_{Sarms} = Iin_x \cdot \frac{\sqrt{3}}{12} \cdot \sqrt{1 - d_x} = 0.435\ A. \tag{36}$$

6) Soft-Commutation Range: The auxiliary switches are turned-off when the energy is transferred from the clamping capacitors to the load and only the energy stored in the leakage inductance is available to cause the charge and discharge of he commutation capacitors. Thus, the soft-commutation is maintained until a minimal input current, when the energy stored in the leakage inductance is lower than the energy stored in the commutation capacitors. The auxiliary switch turn-off is considered to be the critical commutation and defines the soft-commutation range of the converter. The equivalent circuit of this commutation is presented in Fig. 20.

The voltage and current variations in the commutation equivalent circuit are

$$i_{Ld}(t) = \frac{(2 \cdot V_{op} - V_G)}{Zn} \cdot sin(\omega_o \cdot t) - \left(\frac{I_{in}}{2}\right) \cdot \cos(\omega_o \cdot t) \tag{37}$$

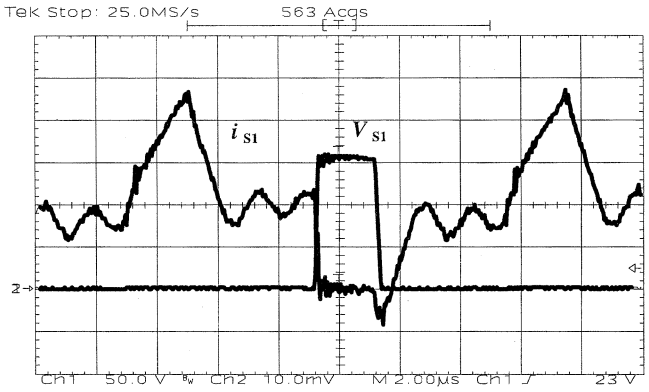

Fig. 23. Main switch voltage and current operating with minimum input voltage (50 V/2 A/2 μs/div).

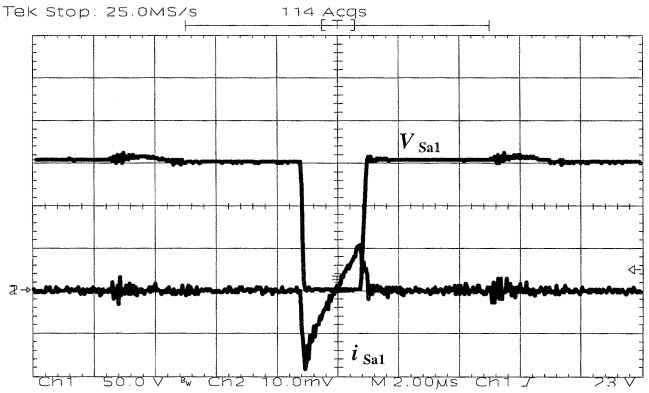

Fig. 24. Auxiliary switch voltage and current operating with minimum input voltage (50 V/2 A/2 μs/div).

$$V_{CS}(t) = 2 \cdot V_{op} - (2 \cdot V_{op} - V_G) \cdot \cos(\omega_o \cdot t) - \left(\frac{I_{in}}{2}\right) \cdot Zn \cdot sin(\omega_o \cdot t) \quad (38)$$

where:

$$\omega_0 = \frac{1}{\sqrt{L_d \cdot C_s}} \quad (39)$$

$$Zn = \sqrt{\frac{L_d}{C_S}} \quad (40)$$

$$L_d = L_{d1} + L_{d2} \quad (41)$$

$$C_S = C_{S2} + C_{Sa2} = C_{S1} + C_{Sa1}. \quad (42)$$

The state plane of the commutation is presented in Fig. 21. As can be seen in this Figure, distance R must be higher than 2. $V_{\rm op}$ to maintain ZVS commutation. Substituting (43) in (44), the soft-commutation criterion is obtained. Equation (45) allows the determination of the soft-commutation range

$$R \geq 2 \cdot V_{op} \quad (43)$$

$$R^2 = (V_G - 2 \cdot V_{op})^2 - \left[j \cdot Zn \cdot \left(-\frac{I_{in}}{2}\right)\right]^2 \quad (44)$$

$$\left(\frac{I_{in}}{2}\right) \geq \frac{\sqrt{4 \cdot V_{op}^2 - (V_G - 2 \cdot V_{op})^2}}{Zn}. \quad (45)$$

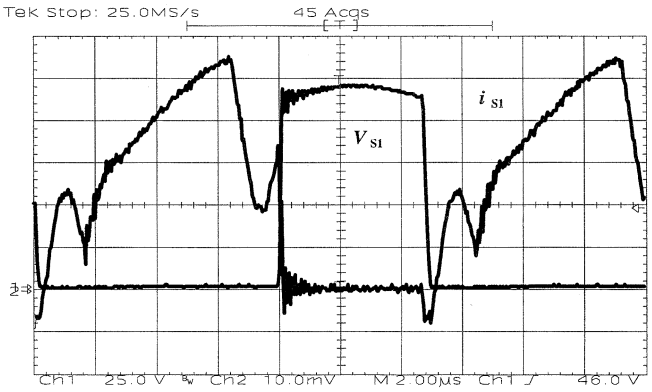

Fig. 25. Main switch voltage and current operating with maximum input voltage (25 V/1 A/2 μs/div).

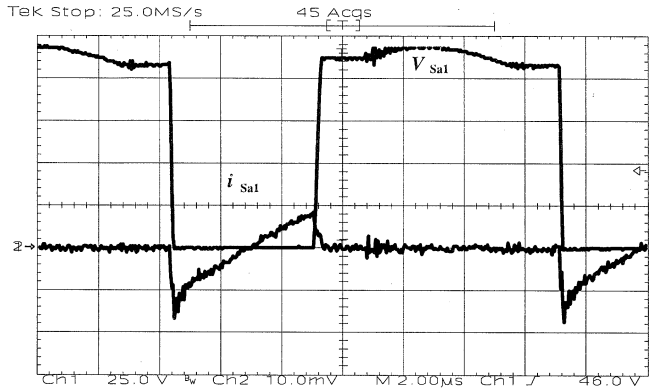

Fig. 26. Auxiliary switch voltage and current operating with maximum input voltage (25 V/2 A/2 μs/div).

7) Output Voltage Ripple: The parameterized output voltage ripple is variable with the static gain (q) and calculated by

$$\overline{\Delta V} = \frac{2 \cdot \Delta V_{Co} \cdot C_o \cdot F_s}{I_o} = \frac{(2 \cdot q - 1)^2}{4 \cdot q^2} \quad (46)$$

where

$I_{\rm o}$ average current of each output;
$C_{\rm o}$ filter capacitor;
$\Delta {\rm V}_{\rm Co}$ output voltage ripple.

D. Experimental Results

A laboratory prototype was implemented following an optimized design procedure. The details regarding the power circuit implemented are presented in Fig. 22.

The main experimental results obtained when operating with minimum input voltage (26 V) are presented in Figs. 23 and 24. The main switch current and voltage waveforms are shown in Fig. 23. Soft-commutation is obtained and the maximum switch voltage is equal to the clamping voltage.

The auxiliary switch voltage and current waveforms are presented in Fig. 24. The auxiliary switch also presents soft-commutation and the rms current and the conduction losses are very low.

The main experimental results obtained when operating with maximum input voltage (44 V) are presented in Figs. 25 and

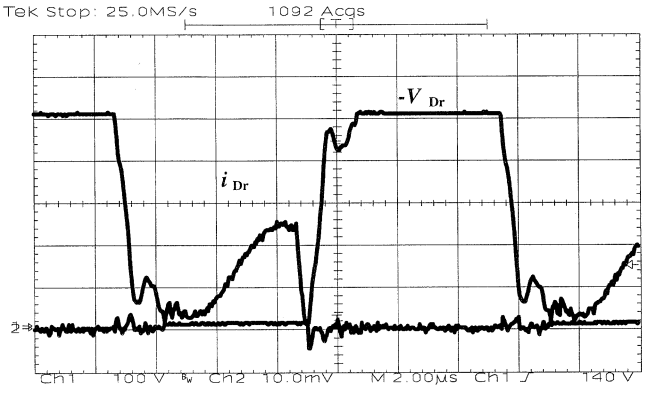

Fig. 27. Rectifier diode voltage and current (100 V/100 A/2 μs/div).

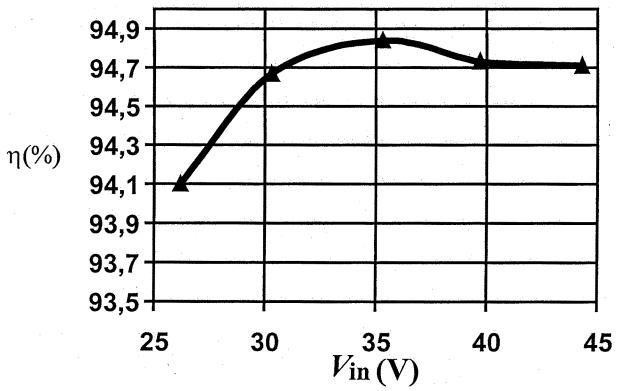

Fig. 28. Efficiency operating with nominal output power and variable input voltage.

26. The main switch current and voltage waveforms are shown in Fig. 25. The maximum switch voltage is equal to 120 V.

The auxiliary switch voltage and current waveforms are presented in Fig. 26.

The voltage and current in a high-voltage rectifier diode is shown in Fig. 27.

The efficiency curve operating with nominal output power and variable input voltage is presented in Fig. 28.

The lowest efficiency obtained with nominal output power is equal to 94.1%.

V. Conclusion

Two alternatives for the implementation of a high-efficiency isolated dc-dc converter with high-output voltage for TWTA applications were proposed and studied. Both structures present several operational characteristics suitable for high output voltage applications supplied by an unregulated input voltage.

The operational characteristics were verified by the implementation of laboratory prototypes operating with a variable input voltage (26/44 V) and with a 3.2 kV total output voltage. The lowest efficiency obtained, operating with nominal output power, is equal to 94.1% for the single-stage topology and equal to 93.4% for the two-stage topology.

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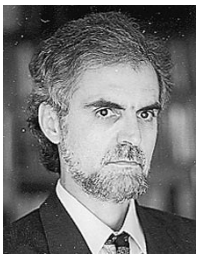

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