DC–DC Converter: Four Switches $V_{\mathrm{pk}} = V_{\mathrm{in}}/2$, Capacitive Turn-Off Snubbing, ZV Turn-On

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Abstract—A new four-switch full-bridge dc–dc converter topology is especially well-suited for power converters operating from high input voltage: it imposes only half of the input voltage across each of the four switches. The two legs of a full-bridge converter are connected in series with each other, across the dc input source, instead of the usual topology in which each leg is connected across the dc source. The topology reduces turn-off switching losses by providing capacitive snubbing of the turn-off voltage transient, and eliminates capacitor-discharge turn-on losses by providing zero-voltage turn-on. (Switching losses are especially important in converters operating at high input voltage because turn-on losses are proportional to the square of the input voltage, and turn-off losses are proportional to the input voltage). The topology is suitable for resonant and nonresonant converters. It adds one bypass capacitor and one commutating inductor to the minimum-topology full-bridge converter (that inductor is already present in many present-day converters, to provide zero-voltage turn-on, or is associated with one or two capacitors to provide resonant operation), and contains a dc-blocking capacitor in series with the output transformer, primary winding, and some nonresonant converters (that capacitor is already present in resonant power converters).

The paper gives a theoretical analysis, and experimental data on a 1.5-kW example that was built and tested: 600-Vdc input, 60-Vdc output at up to 25 A, and 50-kHz switching frequency.

The measured performance agreed well with the theoretical predictions. The measured efficiency was 93.6% at full load, and was a maximum of 95.15% at 44.8% load.

Index Terms—DC–DC converter, full-bridge converter, high input voltage.

I. INTRODUCTION

IN CONVENTIONAL full-bridge converters, the four switches must sustain the input voltage when they are "off." In applications using high values of input voltage, such as railway traction, that voltage can be larger than the safe operating voltage of power transistors that the designer would like to use, if it would be possible. A straightforward way to meet the requirements is to use transistors with sufficiently high breakdown voltage, with the disadvantages of higher cost and higher "on" resistance than would be the case if the transistors could be rated for operation at (for example) half
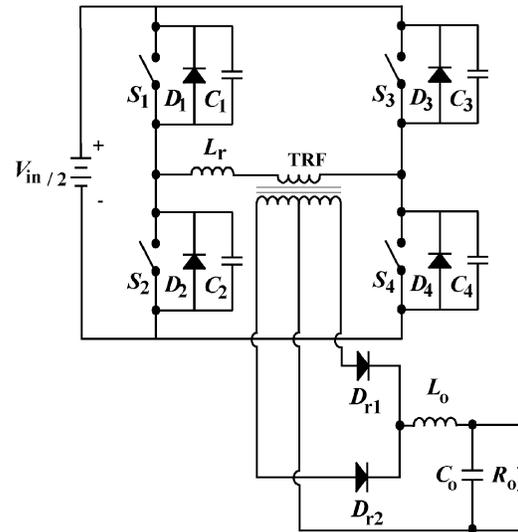
Fig. 1. Conventional full-bridge converter.

of that voltage. In a previous approach [1], each switch was realized as two transistors in series, with voltage-balancing components that would cause the two transistors to share the voltage equally. Then each transistor would sustain only half of input voltage. This approach worked well, but the equipment cost had to include the cost of eight power transistors for the full-bridge, and the voltage-balancing components.

In the new approach proposed here, shown in Fig. 6, the two legs of the full bridge (each leg containing the usual two switches in series) are connected in series across the supply voltage. The node at which the two legs are joined is held at half of the input voltage, by bypass/filter capacitors that are connected to each of the two input rails. (This adds one more bypass capacitor to the usual input bypassing.)

As in many present-day full-bridge converters, e.g., [2], this topology can be operated with

a) capacitive turn-off snubbing to reduce turn-off switching power losses;

b) resonant transitions that provide zero-voltage turn-on to eliminate turn-on switching power losses.

However, a different timing of the switch operations is used, shown in Section III.

II. GENESIS OF THE NEW FULL-BRIDGE TOPOLOGY

The proposed converter is derived from the conventional full-bridge topology presented in Fig. 1. Therefore, several operation characteristics of the full-bridge converter are also presented by the proposed structure.
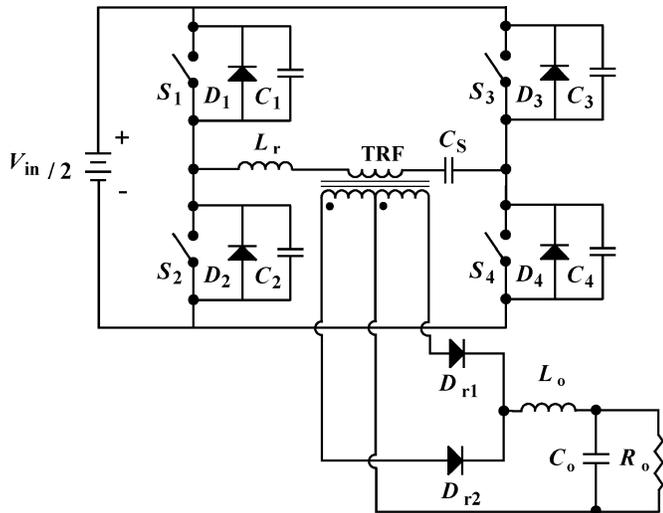
Fig. 2. Full-bridge converter with capacitor in series with transformer primary winding.
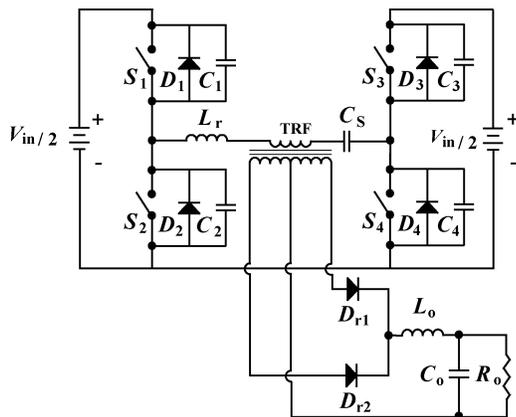

Fig. 3. Separation of the legs.

The genesis of the new converter can be presented following a sequence of modifications in the connection of the components. First, a capacitor is added in series with the transformer, as shown in Fig. 2. The full-bridge converter normally presents this capacitor. Considering two independent input voltage sources, the connection between the two legs can be eliminated as presented in Fig. 3. Then, the polarity of the voltage source and switches in the right leg are reversed, in Fig. 4. Rotating the right leg in 180° and connecting below the left leg, as shown in Fig. 5, the basic structure of the proposed converter as defined. Substituting input voltage sources by two input capacitors, the final configuration of the proposed structure is obtained, as presented in Fig. 6.

III. CIRCUIT AND PRINCIPLE OF OPERATION

A. Circuit Description

Fig. 6 shows the power-stage circuit. The upper leg comprises S_1 and S_2; the lower leg comprises S_3, and S_4. The example design that was built and tested (Section VI) used metal oxide semiconductor field effect transistor (MOSFET) switches. In each MOSFET switch, the internal substrate diode conducts inverse-polarity current and clamps the switch reverse voltage at about -1 V. (If bipolar junction transistors are used, external
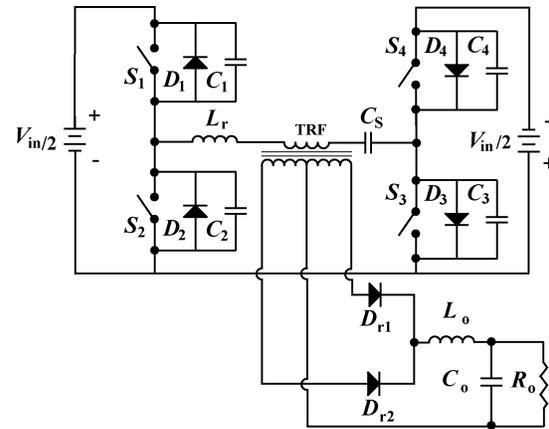

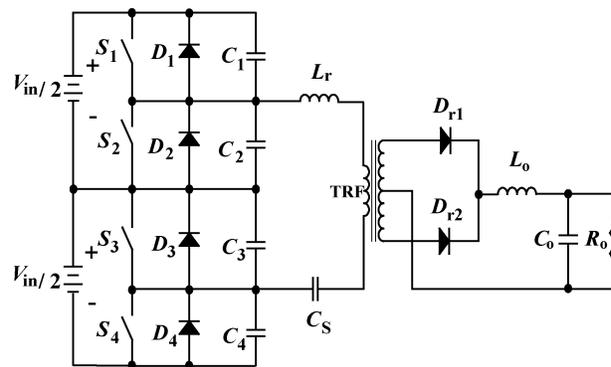Fig. 4. Reverse polarities of battery and switches in the right leg.
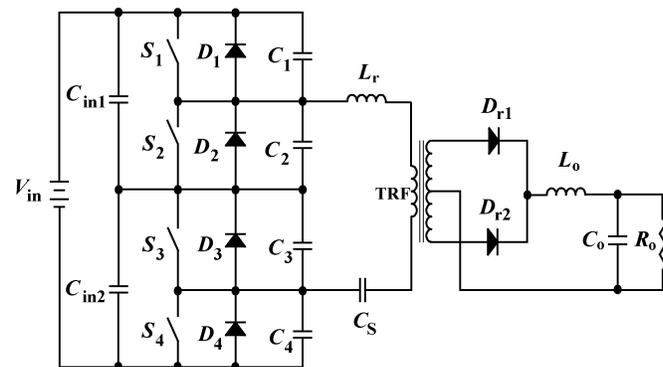

Fig. 5. Rotation of the right leg.

Fig. 6. Power circuit of the proposed converter.

anti-parallel diodes should be added.) The MOSFET internal C_{oss} capacitances are used as $C_1 - C_4$, providing capacitive turn-off snubbing. In some applications (but not in the example in Section VI), the internal capacitances can be supplemented with external capacitors that should be connected across the switches with as low wiring inductance as possible [4].

The input capacitors $C_{\text{in}1}$ and $C_{\text{in}2}$ bypass the input voltage and generate a bypassed dc mid-point voltage of $V_{\text{in}}/2$. As the switches go through their cycle of switching, to be discussed below, each switch has $V_{\text{in}}/2$ applied across it while it is "off." C_{S} is a dc-blocking capacitor that blocks the dc voltage of $V_{\text{in}}/2$ from being applied to the series combination of L_{r} and TRF. In this application, C_{S} is large enough to act as only a dc voltage source, to prevent dc current from flowing through L_{r} and TRF. If a resonant load network is used, C_{S} can be the
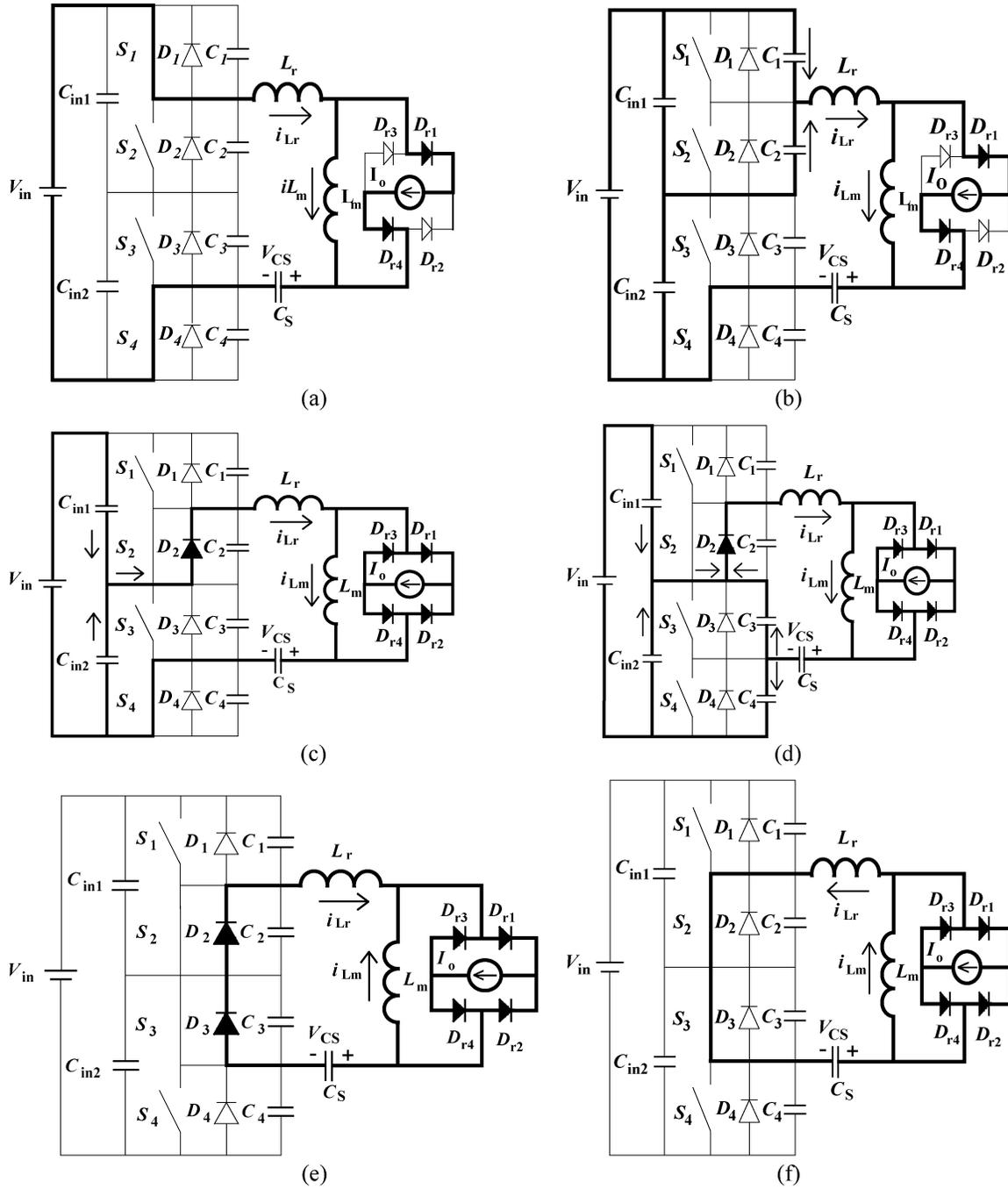
Fig. 7.   Operation stages of power converter.

series-connected resonance capacitor [5]. The stored energy in L_r charges and discharges the snubbing capacitors $C_1 - C_4$ during a conduction gap that is provided between turning-off one of a pair of switches and turning-on the other switch of the pair. That action brings the switch voltage to zero before the switch is turned-on. L_r comprises the sum of an external inductor and the internal primary-side leakage inductance of the transformer. The transformer provides galvanic isolation and voltage transformation, between the source and the load R_o. D_{R1} and D_{R2} rectify the rectangular-wave output of the transformer, and L_o and C_o filter-out the ripple in the rectified output.

B. Principle of Operation

To simplify the explanation and the analysis of circuit operation, the following assumptions are made:.

1) All components are ideal.
2) The ripple in the dc voltage across the series capacitor C_S and the input capacitors C_{in1} and C_{in2} is negligibly small.
3) A current sink I_o replaces the output filter and load.
4) The analysis is based on the circuit reflected to the primary side of the transformer, where L_m represents the mutual inductance in the transformer's T equivalent circuit and the leakage inductance is absorbed into L_r.

5) The output rectifier is replaced by four rectifier diodes.

Fig. 7 shows the resulting equivalent circuit, referred to the primary side of the transformer. The six subsections of the figure show the six successive circuit configurations during a half-period of the cycle of switching. The second half-period is the mirror-image of the first half-period, to be described shortly.

Fig. 8 shows the switch-timing sequence for the four switches, and the resulting circuit voltages and currents. The power transfer and the output/input voltage ratio are controlled by the duty ratio (D) of the switches S_1 and S_3; the switches S_2 and S_4 operate as the complements of S_1 and S_3, respectively. The six sequential circuit states are described as follows.

1) *Stage 1 [Fig. 7(a)]: Power Transfer*

During this stage, power is transferred from the input source (V_{in}) to the load through switches S_1, Dr_1, Dr_4, and S_4. The voltage stored on the series capacitor (V_{CS}) is $V_{in}/2$ and the voltage applied across L_m is ($V_{in} - V_{CS}$).

2) *Stage 2 [Fig. 7(b)]: Commutation of Switch S_1*

At the instant t_1, switch S_1 is turned off at zero voltage, capacitor C_1 begins to charge, and C_2 begins to discharge linearly with time, with a constant current. This stage finishes when $V_{C1}(t) = V_{in}/2$ and $V_{C2}(t) = 0$.

3) *Stage 3 [Fig. 7(c)]: Free-Wheeling Stage*

The voltage across C_2 becomes zero and diode D_2 begins to conduct. During this stage, the resonant inductor current (i_{Lr}) is approximately constant. The circuit operates in a free-wheeling mode, with current flowing from $+V_{in}$, through C_{in1}, D_2, and L_r, through the parallel combination of L_m and the rectifiers (reflected to the primary side), and through C_S and S_4. Because free-wheeling current flows through both polarities of the rectifier, the output voltage is zero. In this stage, switch S_2 must be gated on.

4) *Stage 4 [Fig. 7(d)]: Commutation of Switch S_4*

At the instant t_3, the switch S_4 is turned off at zero voltage and the capacitor C_4 begins to charge while the capacitor C_3 begins to discharge in a resonant way. This stage finishes when $V_{C4}(t) = V_{in}/2$ and $V_{C3}(t) = 0$.

5) *Stage 5 [Fig. 7(e)]: Discharge of Resonant Inductor Energy*

When the voltage V_{C3} becomes zero, the diode D_3 begins to conduct and the current through L_r begins to decrease linearly with a voltage $-V_{CS}$ applied to its terminals. During this stage, the switch S_3 must be gated on.

6) *Stage 6 [Fig. 7(f)]: Charge of Resonant Inductor Energy*

In Stage 6, the resonant inductor current becomes negative and switches $S_2 - S_3$ begin to conduct at zero voltage and zero current. When the current through L_r reaches the value $-I_o/n$, the free-wheeling in the output rectifier is finished and power is transferred from the series capacitor to the load.

In the discharge and charge of resonant inductor energy (stages 5 and 6), a reduction in the duty ratio occurs, because during these stages a gate signal is applied to the S_3 switch, but the free-wheeling in the output rectifiers maintains zero voltage across the power transformer.

In the waveforms of Fig. 8, note that the maximum voltages across the "off" switches are only $V_{in}/2$ because the join-point of C_{in1} and C_{in2} is at voltage $V_{in}/2$: the voltage across S_1 or S_2 is the voltage on C_{in1}, and the voltage across S_3 or S_4 is the voltage on C_{in2}, but both of those capacitor voltages are $V_{in}/2$.
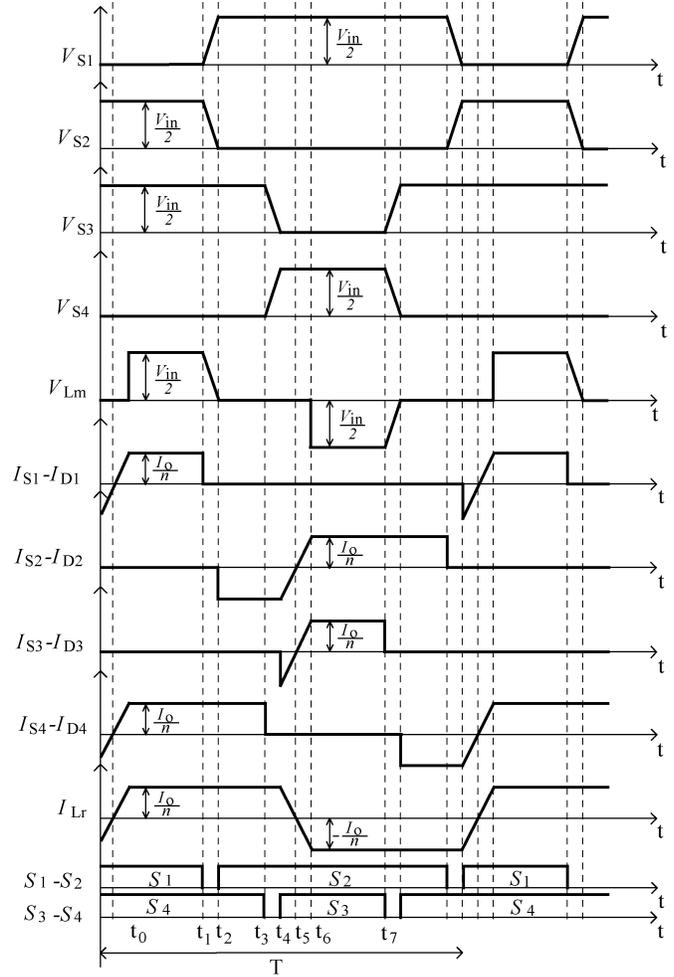

Fig. 8. Main theoretical waveforms.

The principle of operation is analyzed adopting ideal conditions, but some considerations must be done in a practical application.

The input capacitors C_{in1} and C_{in2} are charged and discharged during the free-wheeling period, which occurs in the stage 3 and in its equivalent stage at the second half-period of operation. The voltage in these capacitors can be different from $V_{in}/2$ if the switch-timing sequence of the switches has asymmetry. However, a special control circuit is not necessary, because, as verified in the practical implementation, a very large asymmetry is needed to cause a significant difference from the ideal voltage value of $V_{in}/2$.

The ideal value of the series capacitor voltage V_{CS} is also $V_{in}/2$. During the first operation stage this capacitor receives energy from the input source and after the sixth stage this energy is transferred to the load. This capacitor is designed considering a low voltage ripple (5%–10%), operating as a voltage source. But at the converter start-up, this capacitor is discharged ($V_{CS} = 0$). Thus, while the V_{CS} does not reach $V_{in}/2$, the transformer demagnetization will not occur correctly. But, as the capacitance of the series capacitor is small, the V_{CS} voltage changes quickly and in some switching cycles reaches the ideal value. Classical current protection circuits can avoid an eventual excessive switch peak current during this transition.

IV. ANALYSIS

A. Output Characteristic

At first, temporarily neglecting the reduction of duty ratio caused by the conduction gap that allows the zero-voltage turn-on, the average voltage at the load (V_o) is

$$V_o = \frac{1}{n} \cdot \left[(V_{\text{in}} - V_{\text{CS}}) \cdot \frac{D}{2} + V_{\text{CS}} \cdot \frac{D}{2} \right] \qquad (1)$$

where

V_{in} tnput voltage;
V_{CS} series capacitor voltage;
n   transformer turns ratio (N_p/N_s);
$D/2$ $(t_7 - t_4)/T$.

The voltage on the dc-blocking capacitor (V_{CS}) is

$$V_{\text{CS}} = \frac{V_{\text{in}}}{2}. \qquad (2)$$

Then, the output voltage is

$$V_o = \frac{V_{\text{in}}}{n} \cdot \frac{D}{2}. \qquad (3)$$

But the output voltage is controlled by an effective duty ratio that is smaller than the nominal duty ratio

$$D_{eff} = D - \Delta \qquad (4)$$

where Δ is the reduction of duty ratio caused by the conduction gap. That reduction can be calculated by determining the duration of Stages 5 and 6 (discussed in Section III). The current in L_r will be considered to be constant during the free-wheeling stage, and the current in L_m is neglected. Then, the current in L_r during Stages 5 and 6 is

$$iL_r = \frac{I_o}{n} - \frac{V_{\text{in}}}{2.L_r} \cdot (t_6 - t_4). \qquad (5)$$

At time t_6, $i_{\text{Lr}} = -I_o/n$

$$(t_6 - t_4) = \frac{4.L_r \cdot \frac{I_o}{n}}{V_{\text{in}}}. \qquad (6)$$

This occurs two times in the period T. Then the total reduction of duty ratio during the period is

$$\Delta = 2. \left(\frac{t_6 - t_4}{T} \right) \qquad (7)$$

$$\Delta = \frac{8.L_r.f.\frac{I_o}{n}}{V_{\text{in}}}. \qquad (8)$$

Therefore the reduction in the duty ratio is proportional to L_r and the load current. Subtracting the correction (8) from the first-approximation duty ratio in (3), we obtain, for the output voltage

$$V_o = V_{\text{in}}. \left(\frac{D}{2} - \frac{4.L_r.f \cdot \frac{I_o}{n}}{V_{\text{in}}} \right). \qquad (9)$$

However, the output voltage calculated by (9) is obtained considering ideal components. A more-accurate value of output voltage can be calculated from (10), that includes the rectifier-diode's forward-conduction threshold voltage V_F and the parasitic series resistance R_{int} through which I_o flows: the transformer, rectifier diode, filter inductor, and wiring

$$V_o = \frac{V_{\text{in}}}{n} \cdot \left(\frac{D}{2} - \frac{4.L_r.F_s.\frac{I_o}{n}}{V_{\text{in}}} \right) - R_{int}.I_o - V_f. \qquad (10)$$

B. Turn-On and Turn-Off Switching

Turn-off: The commutation process of the proposed converter is similar to the classical ZVS PWM full-bridge converter. The turn-off losses are reduced by the action of the snubber capacitors that are in parallel with the switches. When a switch is turned-off, the switch current flows through the commutation capacitor, charging this capacitor. Thus, the capacitor voltage, which is also the switch voltage, rises progressively until it reaches the V_{Cin} voltage. Therefore, the crossing of the voltage and current in the switch is reduced and the turn-off losses are minimized.

Turn-on: The converter uses zero-voltage turn-on to eliminate the turn-on switching losses.

The zero-voltage turn-on of the switches is particularly important for converters operating at high dc input voltage, because the power dissipated in switching at nonzero voltage goes as the square of the dc input voltage.

The active switches are turned on while the anti-parallel diodes are conducting, so the switches turn-on at essentially zero voltage and almost zero current. But turn-on losses occur if the turn-off snubber capacitors are not fully discharged. Switches S_1 and S_3 turn-off in the power-transfer stage (stage 1 in Section III), and the output current referred to the primary accomplishes the charge and discharge of the snubber capacitors (linearly with time). The large stored energy of the ripple-filter inductor L_o is available for this purpose, so, as a practical matter, S_2 and S_4 will always be turned-on at zero voltage.

But switches S_2 and S_4 turn-off in the free-wheeling stage (stage 3 of Section III), during which the transformer is short-circuited by the output rectifier. Thus, only the energy stored in the circuit inductance L_r (that includes the transformer primary-side leakage inductance) is available to charge and discharge the snubber capacitors, in a resonant way. The minimum current that maintains zero-voltage turn-on for S_1 or S_3 is

$$I_{\text{min}} = \frac{V_{\text{in}}}{2} \cdot \sqrt{\frac{2.C}{L_r}} \qquad (11)$$

where C is the snubber capacitor ($C = C_1 = C_2 = C_3 = C_4$).

A larger value of L_r decreases the primary-side current needed to obtain zero-voltage turn-on of S_1 and S_3, but the inductance of the resonant inductor L_r is limited by the maximum allowed reduction of duty ratio [see (8)]. Section V gives a design example that includes the effect of that reduction of duty ratio.

V. SIMPLIFIED DESIGN EXAMPLE

The input data for the design of an example converter are as follows.

     Input voltage: $V_{\text{in}} = 600$ V.
     Output Voltage: $V_o = 60$ V.
     Output power: $P_o = 1500$ W.
     Output current: $I_o = 25$ A.
     Switching frequency: $f = 50$ kHz.

A. Determination of Passive Components

1) Transformer Turns Ratio: Assuming ideal switches and diodes and considering the following.

     Nominal duty-ratio: $D = 0.8$.

Maximum duty ratio reduction: 15% of the nominal value of D:

$$\Delta = 0.15 \cdot D = 0.15 \cdot 0.8 = 0.12 \tag{12}$$

.

The transformer turns ratio is calculated from (9):

$$n = \frac{V_{\text{in}} \cdot \left(\frac{D-\Delta}{2}\right)}{V_o} = \frac{600 \text{ V.} \left(\frac{0.8-0.12}{2}\right)}{60 \text{ V}} = 3.4. \tag{13}$$

2) Resonant Inductor L_r: The resonant inductor L_r is defined by the maximum duty ratio reduction specified and is calculated from (8)

$$L_r = \frac{\Delta \cdot V_{\text{in}}}{8 \cdot f \cdot \frac{I_o}{n}} = \frac{0.12 \cdot 600 \text{ V}}{8 \cdot 50 \cdot \text{kHz} \cdot \frac{25 \text{ A}}{3.4}} = 24.5 \,\mu\text{H}. \tag{14}$$

3) Series Capacitor C_S: The series capacitor C_S must be large enough that it can be treated as a voltage source. The voltage ripple on C_S produces a small reduction of the voltage across the transformer primary winding, from the idealized value of $V_{\text{in}}/2$. Thus, the required value of C_S is calculated as a function of the maximum allowable ripple voltage. The relationship between the ripple voltage and the current in C_S is

$$i_{\text{CS}} = C_S \cdot \frac{\Delta V_{\text{CS}}}{\Delta t} \tag{15}$$

where

$$\Delta t = \frac{T}{2} = \frac{1}{2 \cdot f}$$
$$i_{\text{CS}} = \frac{I_o}{n}.$$

Then the series capacitor is calculated as

$$C_S = \frac{I_o}{2 \cdot n \cdot f \cdot \Delta V_{\text{CS}}}. \tag{16}$$

Limiting the peak ripple on the capacitor voltage to 3.5% of the dc value, yields

$$\Delta V_{\text{CS}} = 3.5\% \cdot \frac{V_{\text{in}}}{2} = 3.5\% \cdot \frac{600 \text{ V}}{2} = 10.5 \text{ V} \tag{17}$$

$$C_S \geq \frac{25 \text{ A}}{2 \cdot 3.4 \cdot 50 \cdot \text{kHz} \cdot 10.5 \text{ V}} = 7 \,\mu\text{F}. \tag{18}$$

4) Input Capacitors: The input capacitors $C_{\text{in}1}$ and $C_{\text{in}2}$ can be calculated by the same method used above for C_S. The voltage stored on the input capacitors and the voltage ripple are applied across the switches. It is reasonable to allow 5% voltage ripple in the voltages across $C_{\text{in}1}$ and $C_{\text{in}2}$. The relationship between the capacitors' ripple voltages and the currents in the capacitors is

$$i_{\text{Cin}} = C_{\text{in}} \cdot \frac{\Delta V_{\text{Cin}}}{\Delta t} \tag{19}$$

where

$$\Delta t = \frac{(1-D) \cdot T}{2} = \frac{(1-D)}{2 \cdot f}$$
$$i_{\text{Cin}} = \frac{I_o}{2 \cdot n}$$

Then the input capacitors are calculated as:

$$C_{\text{in}1} = C_{\text{in}2} \geq \frac{I_o \cdot (1-D)}{4 \cdot n \cdot f \cdot \Delta V_{\text{Cin}}}. \tag{20}$$

Allowing 5% voltage ripple, we have

$$\Delta V_{\text{Cin}} = 5\% \cdot 300 \text{ V} = 15 \text{ V}. \tag{21}$$

Then the input capacitors are

$$C_{\text{in}1} = C_{\text{in}2} = \frac{25 \text{ A} \cdot (1 - 0.8)}{4 \cdot 3.4 \cdot 50 \text{ kHz} \cdot 15 \text{ V}} = 0.5 \,\mu\text{F}. \tag{22}$$

5) Output Filter: The output filter can be calculated as for a conventional full-bridge converter. The inductance and capacitance of the filter are calculated with (23) and (24), to provide a maximum current ripple ΔI_o of 10% and a maximum voltage ripple ΔV_o of 1%

$$L_{o\min} = \frac{V_{\text{in}}}{16.f.\Delta i_o.n}$$
$$L_{o\min} = \frac{600 \text{ V}}{16 \cdot 50 \text{ kHz} \cdot 3.4 \cdot 2.5 \text{ A}} = 88.23 \,\mu\text{H} \tag{23}$$
$$C_{o\min} = \frac{\Delta I_o}{8.f.\Delta V_o}$$
$$C_{o\min} = \frac{2.5 \text{ A}}{8 \cdot 50 \text{ kHz} \cdot 0.6 \text{ V}} = 10.4 \,\mu\text{F}. \tag{24}$$

Maximum allowable series resistance of output capacitor C_o

$$R_{ser_{max}} = \frac{\Delta V_o}{\Delta I_o} = \frac{0.6 \text{ V}}{2.5 \text{ A}} = 0.24 \,\Omega. \tag{25}$$

B. Switches Voltage and Current Stresses

1) Active Switches: The maximum voltage across the "off" switches is

$$V_{S_{off}} = \frac{V_{\text{in}}}{2} = \frac{600 \text{ V}}{2} = 300 \text{ V}. \tag{26}$$

The switch rms current is needed if one wishes to calculate the conduction power dissipation in the switch, to estimate the needed cooling capability and to estimate the expected converter efficiency by knowing the sum of all of the losses. The average and rms currents through S_1 and S_3 are

$$I_{S1_{\text{avg}}} = I_{S3_{\text{avg}}} = \frac{I_o}{n} \cdot \frac{D}{2}$$
$$I_{S1_{\text{avg}}} = I_{S3_{\text{avg}}} = \frac{25 \text{ A}}{3.4} \cdot \frac{0.8}{2} = 2.94 \text{ A} \tag{27}$$
$$I_{S1_{\text{rms}}} = I_{S3_{\text{rms}}} = \frac{I_o}{n} \cdot \sqrt{\frac{D}{2}}$$
$$I_{S1_{\text{rms}}} = I_{S3_{\text{rms}}} = \frac{25 \text{ A}}{3.4} \cdot \sqrt{\frac{0.8}{2}} = 4.65 \text{ A}. \tag{28}$$

The average and rms currents through S_2 and S_4 are

$$I_{S2_{\text{avg}}} = I_{S4_{\text{avg}}} = \frac{I_o}{2.n}$$
$$I_{S2_{\text{avg}}} = I_{S4_{\text{avg}}} = \frac{25 \text{ A}}{2 \cdot 3.4} = 3.67 \text{ A} \tag{29}$$
$$I_{S2_{\text{rms}}} = I_{S4_{\text{rms}}} = \frac{I_o}{n.\sqrt{2}}$$
$$I_{S2_{\text{rms}}} = I_{S4_{\text{rms}}} = \frac{25 \text{ A}}{3.4.\sqrt{2}} = 5.2 \text{ A}. \tag{30}$$

2) Output Rectifier: For the output rectifier shown in Fig. 6, the diode reverse voltage is

$$V_{dr} = 2 \cdot \left(\frac{V_{\text{in}}}{2} \cdot \frac{1}{n}\right) = 2 \cdot \left(\frac{600 \text{ V}}{2} \cdot \frac{1}{3.4}\right) = 176.47 \text{ V}. \tag{31}$$
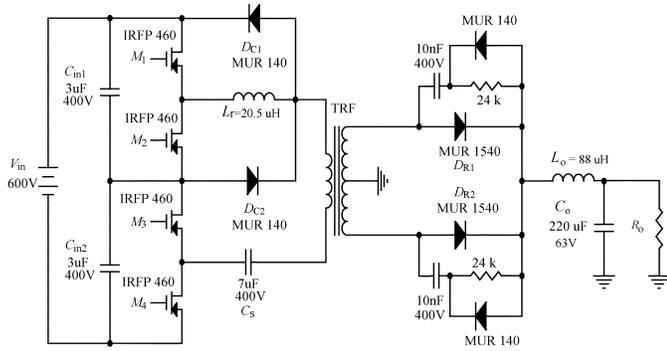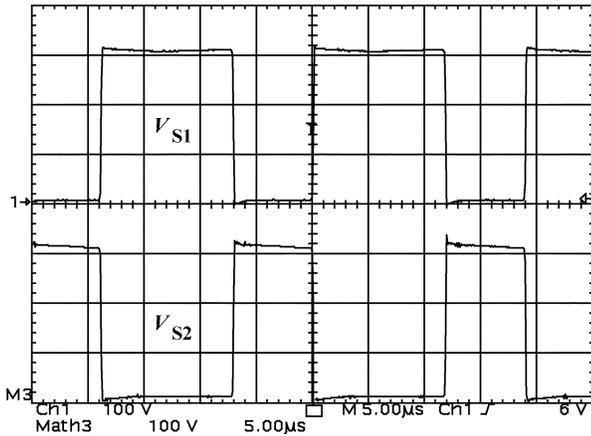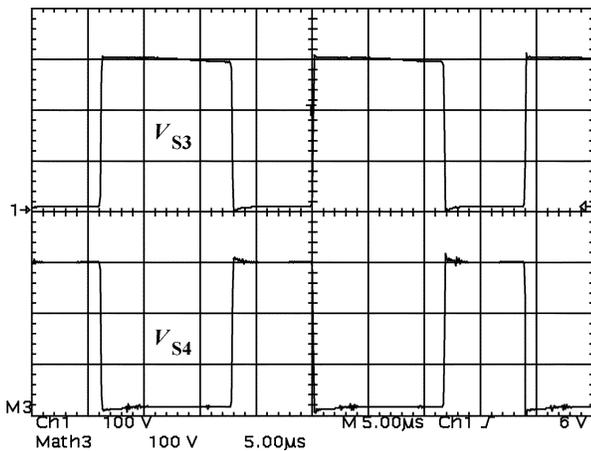
Fig. 9. Circuit diagram of the laboratory prototype.

Fig. 10. Drain-source voltages across S_1 and S_2 ($100 \, \mathrm{V/div} - 5 \, \mu\mathrm{s/div}$).

Fig. 11. Drain-source voltages across S_3 and S_4 ($100 \, \mathrm{V/div} - 5 \, \mu\mathrm{s/div}$).

The rectifier-diodes' average and rms currents are needed for the same reasons as are the switch currents. They are given by

$$I_{dr_{\mathrm{avg}}} = \frac{I_o}{2} = \frac{25 \, \mathrm{A}}{2} = 12.5 \, \mathrm{A} \tag{32}$$

$$I_{dr_{\mathrm{rms}}} = \frac{I_o}{\sqrt{2}} = \frac{25 \, \mathrm{A}}{\sqrt{2}} = 17.667 \, \mathrm{A}. \tag{33}$$

VI. EXPERIMENTAL RESULTS

To verify the practical aspects of the proposed converter, the example design of Section V was built and tested. Fig. 9 is the circuit diagram, including details about the components.
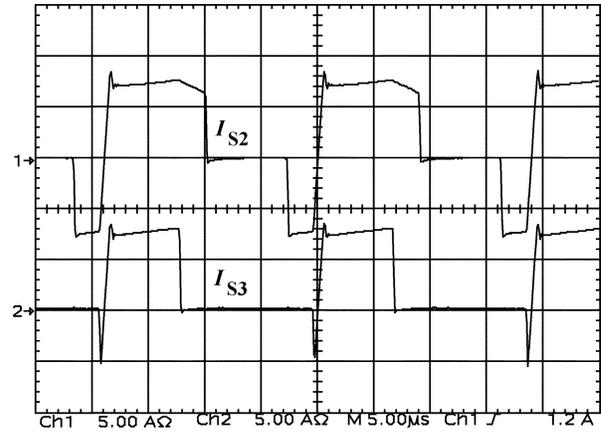
Fig. 12. Currents through S_2 and S_3 ($5 \, \mathrm{A/div} - 5 \, \mu\mathrm{s/div}$).
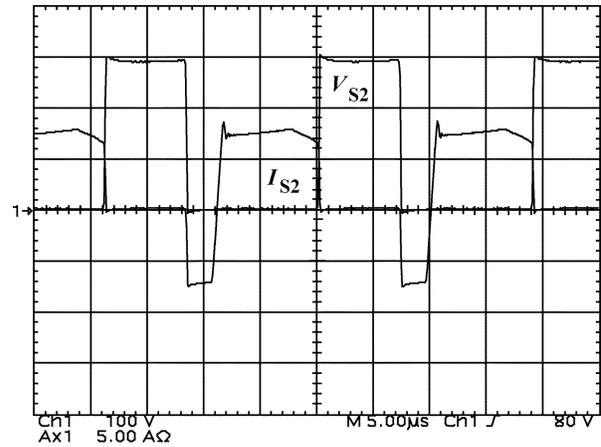
Fig. 13. Commutation of the switch S_2 ($100 \, \mathrm{V/div} - 5 \, \mathrm{A/div} - 5 \, \mu\mathrm{s/div}$).
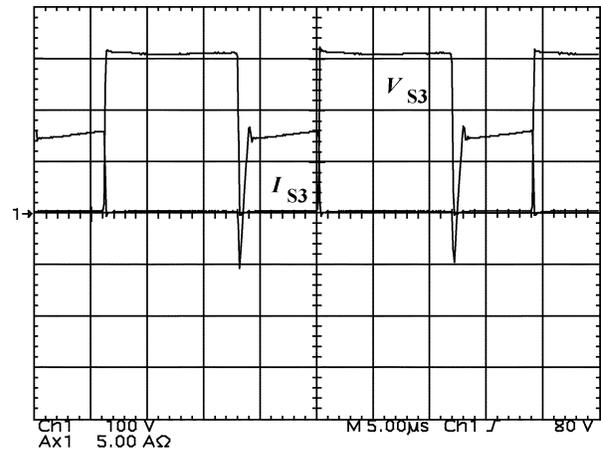
Fig. 14. Commutation of the switch S_3 ($100 \, \mathrm{V/div} - 5 \, \mathrm{A/div} - 5 \, \mu\mathrm{s/div}$).

The transformer and L_r cores were Thornton IP-12 ferrite. The effective value of L_r was 24.5 μH: an actual wound inductor of 20.5 μH, in series with the 4-μH primary-side leakage inductance of the transformer. The MOSFET body diodes were used for $D_1 - D_4$ of Fig. 6, and the MOSFET C_{oss} capacitances were used for $C_1 - C_4$ of Fig. 6.

The interaction of the reverse-recovery process of the rectifier diodes with the resonant inductance (L_r) causes reverse-voltage overshoot and ringing across the rectifier diodes. This problem
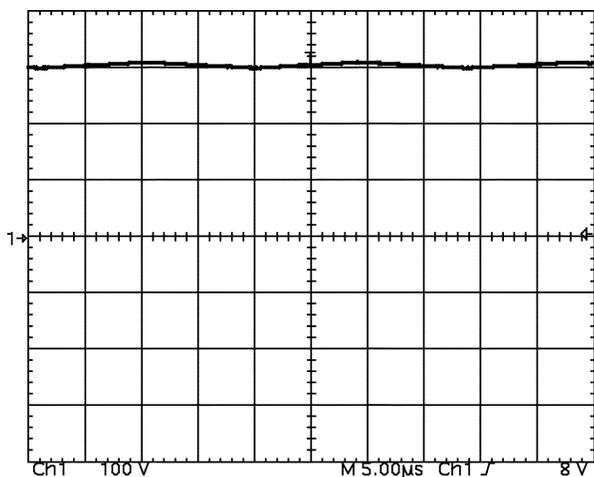
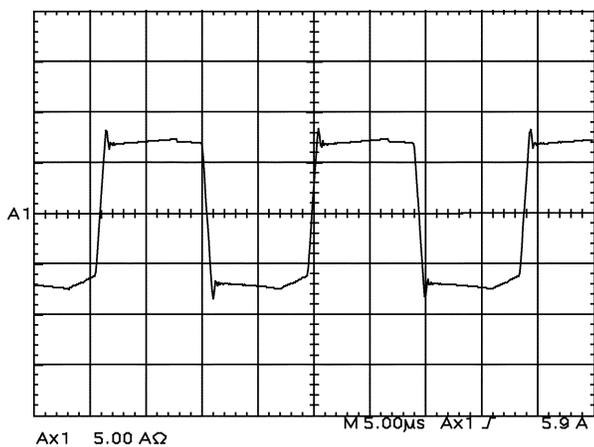Fig. 15. Voltage across the dc-blocking capacitor C_S (100 V/div − 5 μs/div).

Fig. 16. Current through the resonant inductor (5 A/div − 5 μs/div).

Fig. 17. Voltage across the primary winding of the transformer (100 V/div − 5 μs/div).
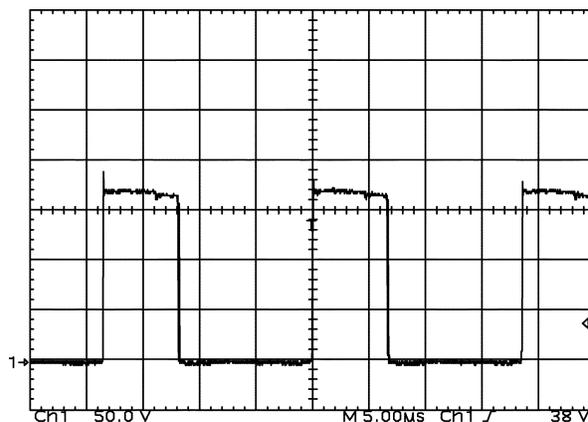
Fig. 18. Voltage across the rectifier diode (50 V/div − 5 μs/div).

can be controlled by using soft-recovery rectifiers and a clamp circuit [2], [3], comprising D_{C1} and D_{C2}, as shown in Fig. 9.

Clamping the junction of the transformer and the commutating inductor to the dc input voltage and to the half-voltage at the junction of C_{in1} and C_{in2} reduces the diode reverse-voltage overshoot in proportion to the ratio between the resonant inductance (L_r) and the leakage inductance of the transformer [2]. In addition, a RCD snubber is connected across the rectifiers, limiting the remainder of the overshoot (caused by the transformer leakage inductance) that remains after the clamping by diodes D_{C1} and D_{C2}.

As the output stage of the proposed converter is identical to the classical ZVS full-bridge converter, all techniques developed for clamping the diode voltage in the secondary side also can be used in the proposed converter. Some alternatives of three-level ZVS converters with nondissipative secondary voltage clamping are presented in [6]–[8].

Figs. 10–20 are oscilloscope waveforms of the principal voltages and currents, recorded while the converter was supplying 1.5 kW of output power (25 A at 60 Vdc), with 600-Vdc input. All of the observed waveforms agree well with the theoretical waveforms presented in Fig. 8.

Figs. 10 and 11 demonstrate the principal characteristic of this converter topology: the switch peak voltages are 300 V, half of the 600-Vdc input voltage.
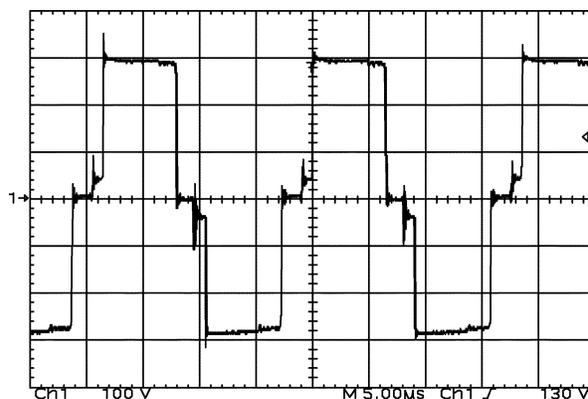
Fig. 12 shows the currents in switches S_2 and S_3, showing clearly the different conduction times of the two groups of switches.

Figs. 13 and 14 shows the current and voltage of switch S_2 and S_3, showing clearly the mechanism of the zero-voltage turn-on switching.

The voltage across the dc-blocking capacitor C_S; the dc value and the ripple are close to the expected values of 300 V and 3.5% of 300 V.

Fig. 16 shows the current through L_r; the maximum positive and negative values are close to the expected $I_o/n = (25 \text{ A})/3.4 = 7.35$ A.

The voltage across the primary winding of the transformer is presented in Fig. 17. Fig. 18 shows the voltage across the rectifier diode.

Figs. 19 and 20 show the voltage across the primary winding of the transformer and the voltage across the rectifier diode without the clamping diodes D_{C1} and D_{C2}. Those figures show clearly the benefits obtained by using the clamp circuit of [2] and [3].

Fig. 21 shows the experimental and theoretical (from (10)) dependence of output voltage on output current, with $V_{in} = 600$ Vdc and $D = 0.78$. The output voltage decreases with increasing output current because the reduction of effective duty ratio increases with increasing current in L_r, as the conduction gap increases, as predicted by (8).

The output voltage calculated by (10) is equal the measured output voltage, considering a rectifier-diode conduc-
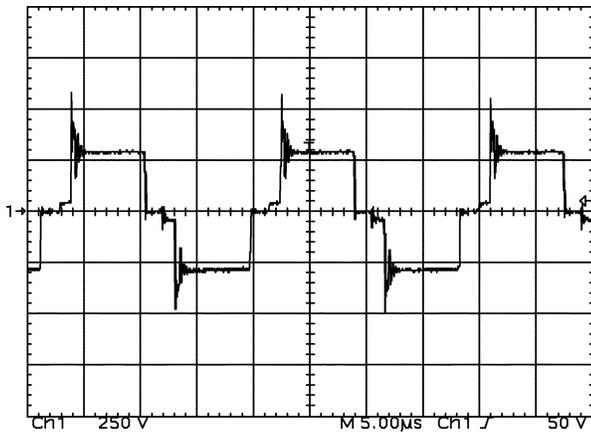
Fig. 19. Voltage across the primary winding of the transformer eliminating the claming diodes D_{C1} and D_{C2} $(250 \text{ V}/\text{div} - 5 \ \mu\text{s}/\text{div})$.
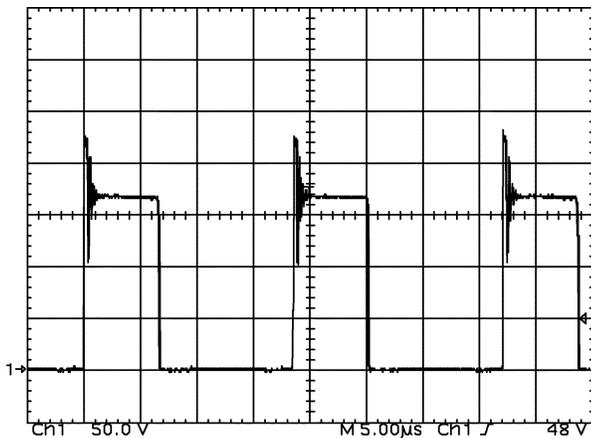

Fig. 20. Voltage across the rectifier diode eliminating the clamping diodes D_{C1} and D_{C2} $(50 \text{ V}/\text{div} - 5 \ \mu\text{s}/\text{div})$.
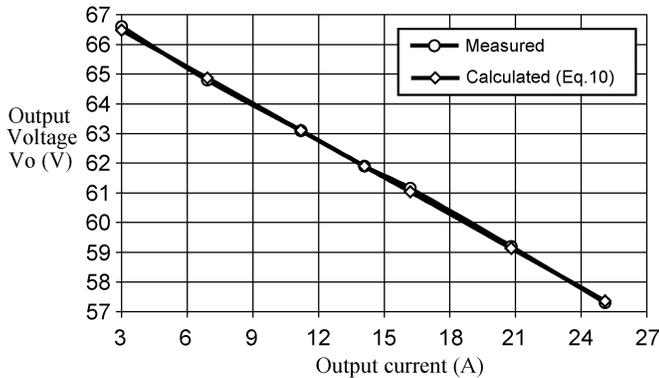

Fig. 21. Output voltage as function of output current.

tion-threshold voltage equal to $V_F = 1.1$ V and a total parasitic series resistance equal to $R_{\text{int}} = 0.06 \ \Omega$.

Fig. 22 shows the measured efficiency of the power circuit as a function of the output current. The efficiency at full load (25 A) was 93.6%; the maximum efficiency at 11.2 A (44.8% load, as also shown in Fig. 22) was 95.15%.

The efficiency was also measured operating with hard-switching, eliminating the external resonant inductor L_r. The efficiency was 2% lower than the operation with soft-commutation at nominal load.
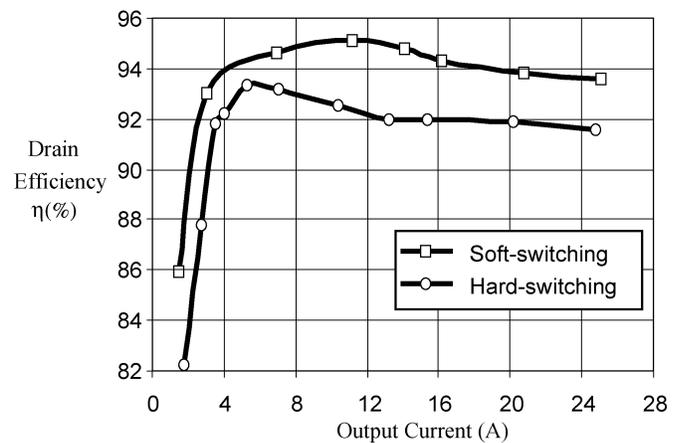

Fig. 22. Measured efficiency of the proposed converter.

The proposed converter does not operate correctly using the classical hard-switching PWM modulation of the full-bridge converter. In this case, the simultaneous turn-on and turn-off of the switches does not ensure the static and dynamic voltage sharing of the switches. Therefore, the hard-switching operation was tested using the same modulation presented in Fig. 8.

A losses comparison with the classical ZVS PWM full-bridge converter can be done considering equivalent operating conditions. Considering the same input voltage, switching frequency, output voltage and current for both converters, and a transformer turns ratio of the proposed converter equal to half of the transformer turns ratio of the full-bridge, the duty ratio of both converters will be equal. But the switch peak and rms currents will be double in the proposed converter. Thus, the difference of the conduction losses between the converters will depend mainly on the technology of the switches available for the voltage range considered. Considering the input voltage utilized in the prototype (600 V) and the use of MOSFETs, the full-bridge converter can be implemented with a 800-V MOSFET (commercial voltage range) and the proposed converter can use 400-V MOSFET. Considering MOSFET from the same manufacturer and with the same die size, the full-bridge converter can use, for example, the MOSFET IRFPE50 ($V_{\text{Dss}} = 800$ V, $R_{\text{DSon}} = 1.2 \ \Omega$) and the proposed converter can use the MOSFET IRFP350 ($V_{\text{Dss}} = 400$ V, $R_{\text{DSon}} = 0.3 \ \Omega$). The ratio between the MOSFETs conduction losses of the converters is equal to $[1.2/(0.3 * 4)] = 1$. Therefore, both converters will present the same MOSFET conduction losses.
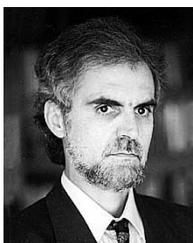
VII. CONCLUSION

This new four-switch power-circuit topology is well-suited to economical realization of full-bridge dc–dc converters to be operated from dc input voltages of up to twice the maximum voltage that is allowed to be imposed on each switch in the power circuit. The measured performance of an example 1.5-kW dc–dc converter (600-Vdc input to 60-Vdc output at up to 25 A) agreed well with theoretical predictions.

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