A Three-Phase ZVS PWM DC/DC Converter With Asymmetrical Duty Cycle for High Power Applications

Demercil de Souza Oliveira, Jr. and Ivo Barbi, *Senior Member, IEEE*

***Abstract*—This paper proposes the application of the asymmetrical duty cycle to the three-phase dc/dc pulse-width modulation isolated converter. Thus, soft commutation is achieved for a wide load range using the leakage inductance of the transformer and the intrinsic capacitance of the switches, as no additional semiconductor devices are needed. The resulting topology is characterized by an increase in the input current and output current frequency, by a factor of three compared to the full-bridge converter, which reduces the filters size. In addition, the rms current through the power components is lower, implying the improved thermal distribution of the losses. Besides, the three-phase transformer allows the reduction of the core size. In this paper, a mathematical analysis, the main waveforms, a design procedure, as well as simulation and experimental results obtained in a prototype of 6 kW are presented.**

***Index Terms*—Full-bridge converter, pulse-width modulation (PWM), soft commutation.**

I. Introduction

NOWADAYS, the main topology used in high power dc/dc conversion is the zero-voltage switching (ZVS) pulse-width modulation (PWM) full-bridge converter [1], [2]. It is characterized by four switches operating in high frequency. The soft commutation can be obtained by using phase shift modulation, which preserves the simplicity and achieves high power density.

However, for higher power levels, the components face several stresses. As possible solutions, the parallelism of components or even converters can be applied. The former choice increases the complexity of the compromise between the layout circuit and the thermal design. Besides that, one should consider that the dynamic and static current sharing problem limits its application. The other alternative causes redundancy in the control circuits as well as in the number of power components and drivers, increasing the global cost and size of the equipment.

A prominent alternative was proposed by Ziogas [3]. It uses a three-phase inverter coupled to a three-phase high frequency transformer and to a three-phase high frequency rectifier (Fig. 1). The resulting advantages are as follows:

1) increase of the input current and output current frequency, by a factor of three compared to the full-bridge converter;
2) lower rms current through power components;
3) reduction in the transformer size.

The disadvantages are:

1) control circuit complexity;
2) commutation losses.

Considering that digital signal processors (DSPs) can overcome the control aspect, several researchers have investigated techniques to achieve soft commutation. Divan [4] has proposed a circuit (Fig. 2) in which soft commutation can be achieved for a wide load range. Nevertheless, it is only viable in applications where bi-directional power flow is needed, because six additional switches are included.

Bhat [5] and Ziogas [6] applied the resonance concept in three phase dc/dc converters, as shown in Figs. 3 and 4, reaching soft commutation. However, the resulting topologies suffer high voltage and current stresses, and also a considerable increase in the volume of reactive power elements.

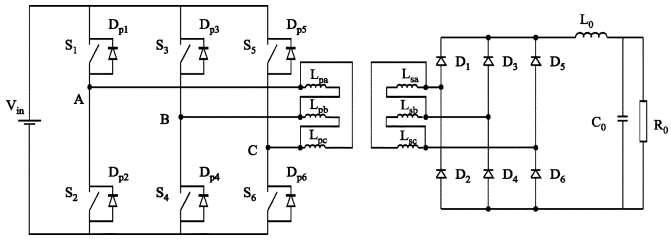

Fig. 1. Three-phase dc/dc converter [3].

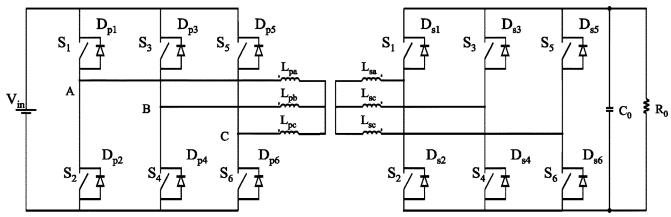

Fig. 2. Three-phase ZVS dc/dc converter [4].

II. Proposed Three-Phase ZVS PWM DC/DC Converter

This paper proposes the application of the asymmetrical duty cycle [7] to the three-phase configuration shown in Fig. 5. Thus

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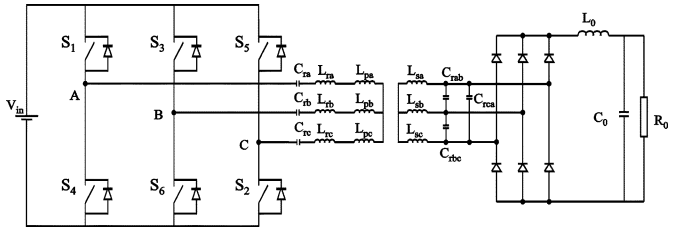

Fig. 3. Three-phase LCC resonant dc/dc converter [5].

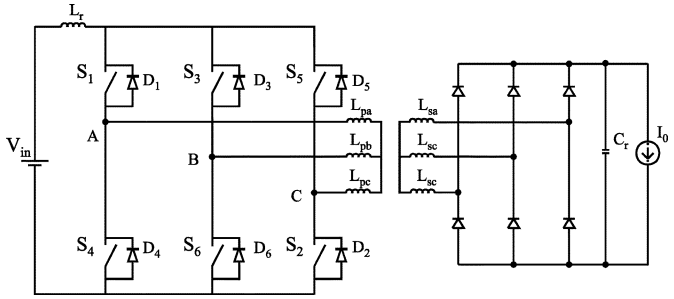

Fig. 4. Three-phase resonant dc link dc/dc converter [6].

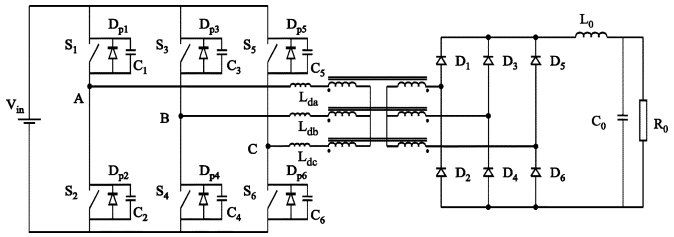

Fig. 5. ZVS dc/dc three-phase converter.

soft commutation is obtained for a wide load range using the leakage inductance of the transformer and the intrinsic capacitance of the switches, and no additional semiconductors devices are needed. Moreover, external inductors and capacitors can be added in order to improve the turning off of the main switches, as well as to control the ZVS commutation load range.

The gating signals sequence and the obtained main waveforms are shown in Fig. 6. The operation of this converter can be described in several stages, depending on the duty cycle, load current and the characteristic impedance. For simplicity, only the operation mode called maximum characteristic impedance mode (MAXCIM) is presented, once that it occurs at maximum output voltage. The MAXCIM mode is composed of three operation stages for each switch, yielding eighteen operating stages.

In order to describe the behavior of the currents and voltages in the circuit, shown in Table I, the following parameters are defined:

$$\alpha_i = \frac{I_0}{V_{\text{in}}} \text{Z}_{0\text{i}} \tag{1}$$

$$Z_{0i} = \sqrt{\frac{L_{deq}}{C}} \tag{2}$$

$$\omega_{0i} = \frac{1}{\sqrt{L_{\text{eq}} C}}. \tag{3}$$

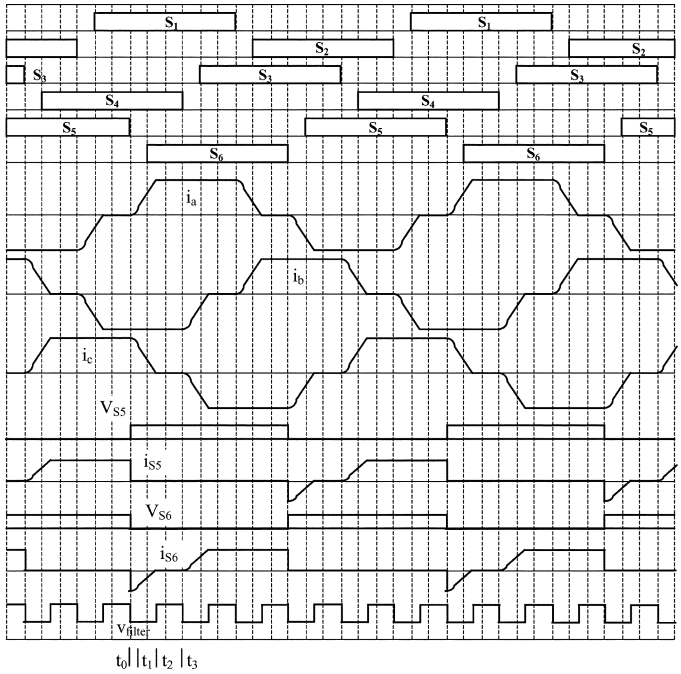

Fig. 6. Main waveforms in the MAXCIM mode.

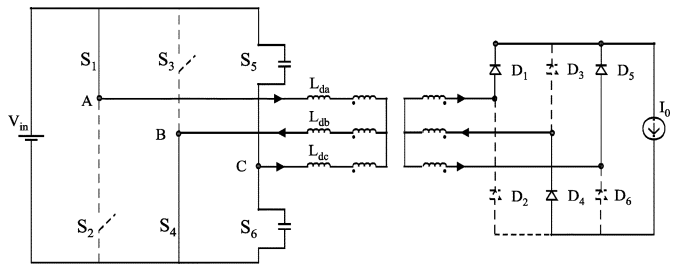

Fig. 7. First stage for switch $S_5[t_0, t_1]$.

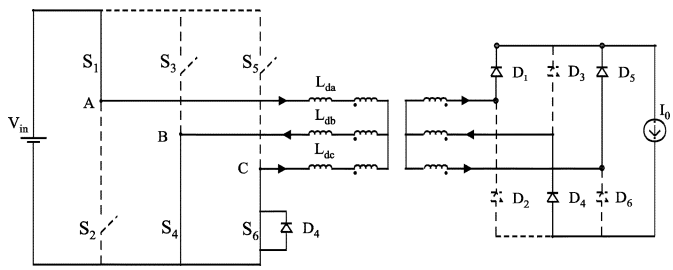

Fig. 8. Second stage for switch $S_5[t_1, t_2]$.

First Stage $[t_0, t_1]$: This stage begins when switch S_5 is turned off. It can be seen in the equivalent circuit shown in Fig. 7 that the current in phase b remains constant, while the resonance among the leakage inductances in phases a and c and the equivalent capacitance $C_5 + C_6$ occurs (see Table II).

Second Stage $[t_1, t_2]$: When the voltage over the capacitor C_5 reaches V_{in}, switch S_6 can be turned on in ZVS mode, establishing the equivalent circuit presented in Fig. 8. The current in phase b remains constant while currents in a and c change linearly.

TABLE I
CURRENTS AND VOLTAGES IN MAXCIM MODE

	FIRST STAGE	SECOND STAGE	THIRD STAGE
$\mathbf{i_a}$	$\alpha_g \frac{V_{in}}{Z_{0g}}\left(1-\cos\omega_{0g}t\right)$	$i_a(0)+\frac{V_{in}}{Z_{0g}}\omega_{0g}t$	$\alpha_g \frac{V_{in}}{Z_{0g}}$
$\mathbf{i_b}$	$\alpha_g \frac{V_{in}}{Z_{0g}}$	$\alpha_g \frac{V_{in}}{Z_{0g}}$	$\alpha_g \frac{V_{in}}{Z_{0g}}$
$\mathbf{i_c}$	$\alpha_g \frac{V_{in}}{Z_{0g}}\cos\omega_{0g}t$	$i_c(0)-\frac{V_{in}}{Z_{0g}}\omega_{0g}t$	0
$\mathbf{v_c}$	$\alpha_g V_{in}\sin\omega_{0g}t$	V_{in}	V_{in}
$\mathbf{V_{filter}}$	$V_{in}\left(1-\frac{\alpha_g}{2}\sin\omega_{0g}t\right)$	$\frac{1}{2}V_{in}$	V_{in}
$\Delta\mathbf{t}$	$\frac{1}{\omega_{0g}}\arcsin\frac{1}{\alpha_g}$	$\frac{1}{\omega_{0g}}\sqrt{\alpha_g^2-1}$	$\begin{cases} DT_s+\left(\frac{T_s}{3}-t_d\right)-\Delta t_1-\Delta t_2 \\ \frac{2}{3}T_s-DT_s-\Delta t_1-\Delta t_2-t_d \end{cases}$
Boundary Condition	$v_c(\Delta t)=V_{in}$	$i_c(\Delta t)=0$	-

TABLE II
CURRENTS AND VOLTAGES IN MINCIM AND VARCIM MODES

	i_a	i_b	i_c	Δt	V_{filter}	Boundary Condition
MINIMUM CHARACTERISTIC IMPEDANCE MODE (MINCIM)						
First Stage	$I_0-\frac{1}{3}\frac{V_{in}}{L_d}t$	$I_0-\frac{2}{3}\frac{V_{in}}{L_d}t$	$\frac{1}{3}\frac{V_{in}}{L_d}t$	$\frac{3L_dI_0}{V_{in}}$	0	$i_b(\Delta t_1)=-I_0$
Second Stage	0	I_0	I_0	$DT_s-\Delta t_1$	V_{in}	-
Third Stage	0	I_0	I_0	$\frac{T_s}{3}-DT_s$	0	-
VARIABLE CHARACTERISTIC IMPEDANCE MODE (VARCIM)						
First Stage	$\frac{V_{in}}{2L_d}t$	I_0	$I_0-\frac{V_{in}}{2L_d}t$	$DT_s-\frac{T_s}{3}$	$\frac{V_{in}}{2}$	-
Second Stage	$i_a(0)+\frac{1}{3}\frac{V_{in}}{L_d}t$	$i_b(0)-\frac{1}{3}\frac{V_{in}}{L_d}t$	$i_c(0)-\frac{2}{3}\frac{V_{in}}{L_d}t$	$\frac{3L_dI_0}{V_{in}}-(3D-1)\frac{T_s}{2}$	0	$i_a(\Delta t_2)=I_0$
Third Stage	I_0	$i_b(0)-\frac{V_{in}}{2L_d}t$	$i_c(0)-\frac{V_{in}}{2L_d}t$	$T_s\left(D-\frac{1}{3}\right)$	$\frac{1}{2}V_{in}$	-
Fourth Stage	I_0	0	I_0	$DT_s-\Delta t_2-\Delta t_3$	V_{in}	-

Third Stage $[t_2, t_3]$: From the instant when the currents in phases a and c reach I_0 and null, respectively, all voltages and currents remain constant until the next switch turns off, as the equivalent circuit shown in Fig. 9 represents this stage.

The fourth stage shown in Fig. 10 is analogous to the first one, but it starts when switch S_4 turning off occurs.

III. COMMUTATION AND OUTPUT CHARACTERISTIC ANALYSIS

In the previous section, the operating stages concerning the MAXCIM mode have been presented. However, in order to describe the output characteristic, the modes minimum characteristic impedance (MINCIM) and variable characteristic impedance (VARCIM) have been analyzed. The MAXCIM stages can be obtained by neglecting the switches capacitance.

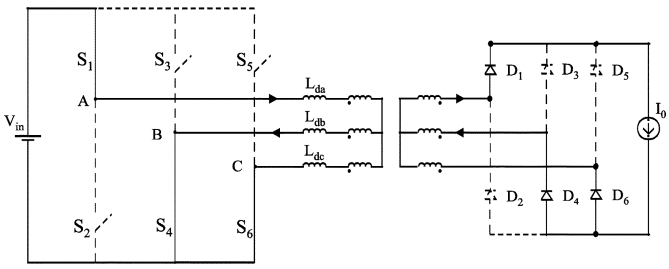

Fig. 9. Third stage for switch $S_5[t_2, t_3]$.

A. Operation in MINCIM Mode

The gating signals, the line currents and the voltage applied to the output filter, in the MINCIM mode, are presented in Fig. 14.

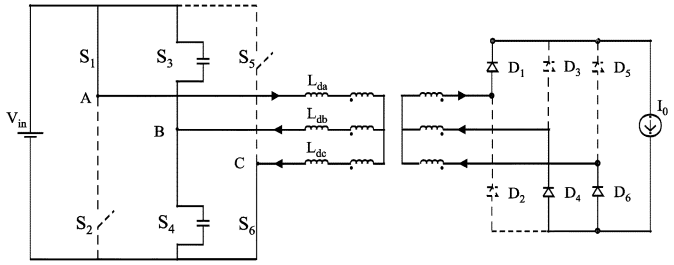

Fig. 10. First stage for switch S_4.

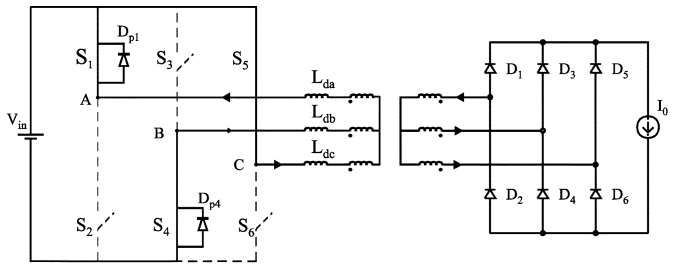

Fig. 11. First stage in the MINCIM mode $[t_0, t_1]$.

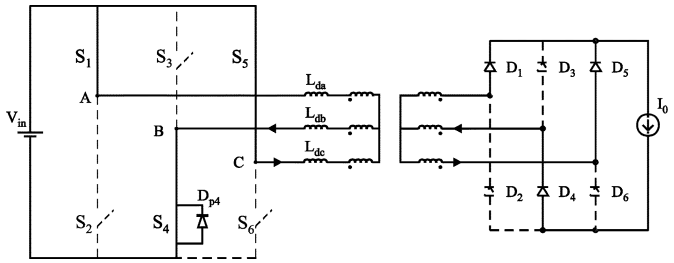

Fig. 12. Second stage in the MINCIM mode $[t_1, t_2]$.

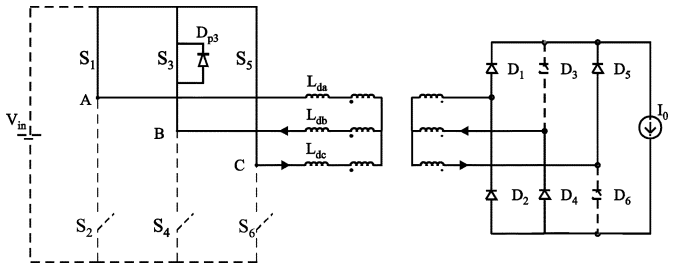

Fig. 13. Third stage in the MINCIM mode $[t_2, t_3]$.

First Stage $[t_0, t_1]$: This stage is started with the turning off of S_3, causing the current in phase b to decrease linearly, as shown in Fig. 11.

Second Stage $[t_1, t_2]$: At the moment when the linear transitions among the line currents finish, the second stage begins, as established in Fig. 12.

Third Stage $[t_2, t_3]$: The switch S_4 turning off determines the beginning of this stage (Fig. 13), in which load current freewheels by S_5 and D_{p3}, and the switch S_5 turning off is responsible for its end.

B. Operation in VARCIM Mode

The gating signals, the line currents, the voltages and currents in the main switches and the voltage applied to the output filter in the VARCIM mode are presented in Fig. 14. One can see that this stage can be considered as an intermediate operation between MAXCIM and MINCIM modes, and it occurs when a switch is turned off during a linear current transition (see Fig. 15).

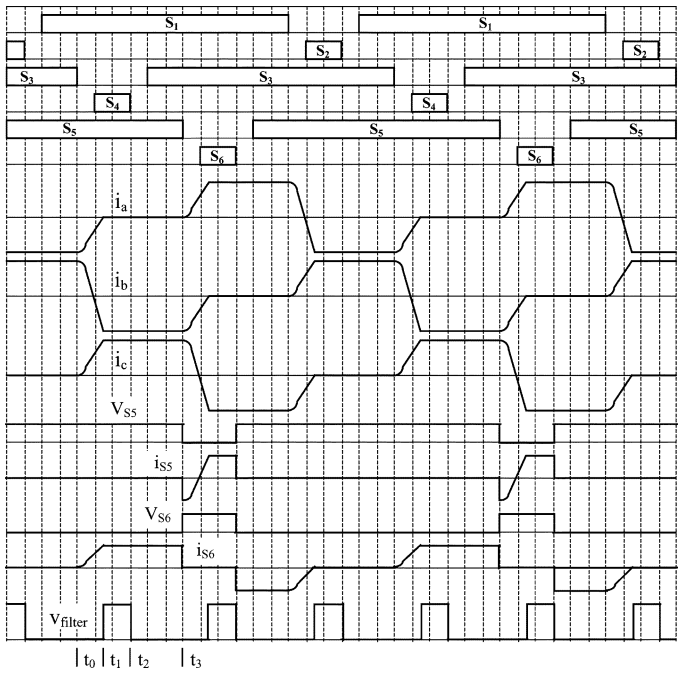

Fig. 14. Main waveforms in the MINCIM mode.

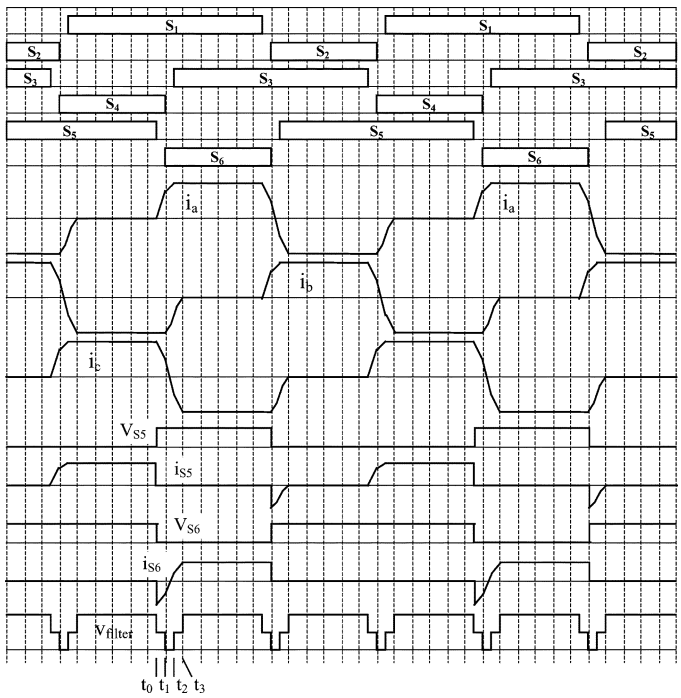

Fig. 15. Main waveforms in the VARCIM mode.

First Stage $[t_0, t_1]$: This stage is started by the turning off of switch S_5, as shown in Fig. 16, causing the transition between two line currents.

Second Stage $[t_1, t_2]$: At the moment when switch S_4 turns off, a linear transition among the line currents begins, according to the circuit shown in Fig. 17.

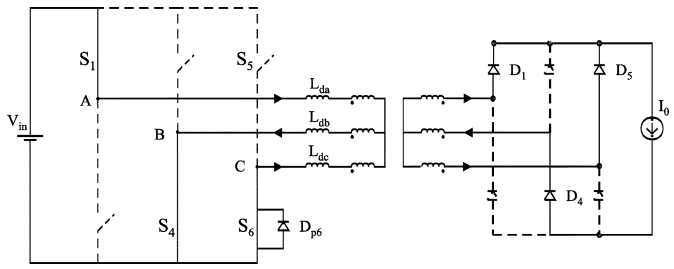

Fig. 16. First stage in VARCIM mode $[t_0, t_1]$.

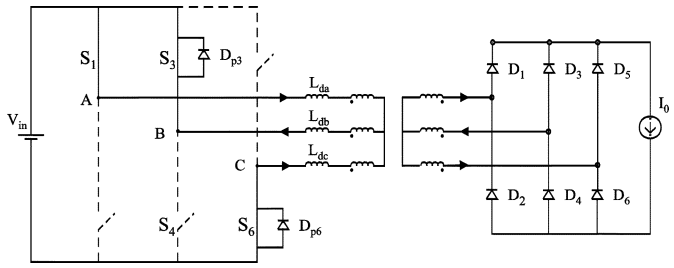

Fig. 17. Second stage in VARCIM mode $[t_1, t_2]$.

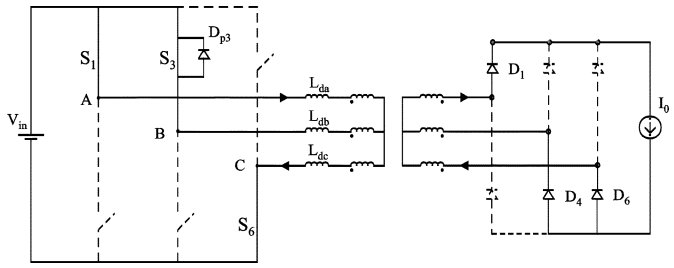

Fig. 18. Third stage in VARCIM mode $[t_2, t_3]$.

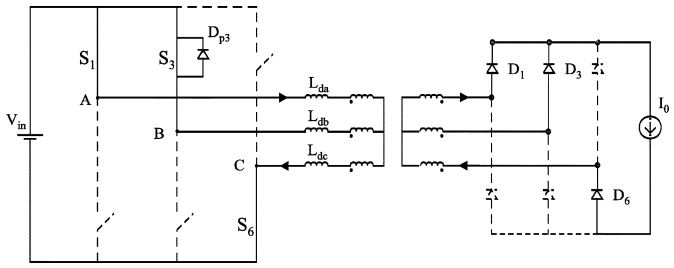

Fig. 19. Fourth stage in VARCIM mode $[t_3, t_4]$.

Third Stage $[t_2, t_3]$: When any line current reaches I_0, it remains constant, while the remaining currents continue the linear transition, as it can be seen in Fig. 18.

Fourth Stage $[t_3, t_4]$: When the currents reach I_0 and null, this stage begins. All the currents become constant until the next switch turns off (see Fig. 19).

From the stages described previously, one can obtain the expression of the static gain G as (4), where I_0' is the parameterized load current defined in (5), f_s is the switching frequency, $V_{\rm in}$ is the input voltage, L_d is the leakage inductance and I_0 is the load current referred to the primary side

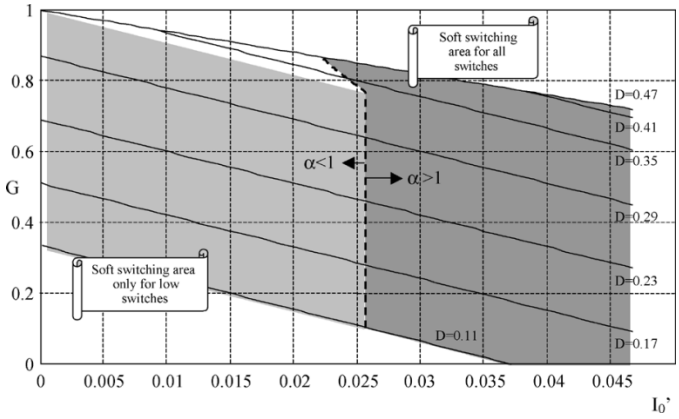

Fig. 20. Soft switching range.

$$G = \begin{cases} 3\,(D - 3\cdot I_0') & \text{if } 3I_0' < D < \frac{1}{3}\,(\text{MINCIM}) \\ \frac{1}{2} + 3\left(\frac{D}{2} - 3\cdot I_0'\right) & \text{if } \frac{1}{3} < D < \frac{1}{3} + 2I_0'\,(\text{VARCIM}) \\ 1 - 6\cdot I_0' & \text{if } D > \frac{1}{3} + 2I_0'\,(\text{MAXCIM}) \end{cases} \quad (4)$$

$$I_0' = \frac{f_s L_d I_0}{V_{\rm in}}. \quad (5)$$

Analyzing the circuit in order to obtain the soft switching condition, it results in the minimum load condition (6) and in the minimum and maximum dead times (7)

$$\alpha_i > 1 \quad (6)$$

$$\frac{1}{\omega_{0i}} \arcsin\left(\frac{1}{\alpha_i}\right) < t_d < \frac{1}{\omega_{0i}}\sqrt{\alpha_i^2 - 1} + \frac{1}{\omega_{0i}} \arcsin\left(\frac{1}{\alpha_i}\right) \quad (7)$$

where the normalized conductance, the characteristic impedance and the angular frequency are given by (8)–(10), respectively

$$\alpha_i = \frac{I_0}{V_{\rm in}} Z_{0i} \quad (8)$$

$$Z_{0i} = \sqrt{\frac{L_{deq}}{C}} \quad (9)$$

$$\omega_{0i} = \frac{1}{\sqrt{L_{\rm eq} C}}. \quad (10)$$

The equivalent leakage can be obtained by the analysis of the equivalent circuit, except in the VARCIM mode. Therefore, a linear approach has been considered, as shown in

$$L_{deq} = \begin{cases} 1.5 \cdot L_d & \text{if } 3I_0' < D < \frac{1}{3} \\ \left[\frac{0{,}5}{2I_0'} \cdot \left(D - \frac{1}{3}\right) + 1.5\right] L_d & \text{if } \frac{1}{3} < D < \frac{1}{3} + 2I_0' \\ 2 \cdot L_d & \text{if } \frac{1}{3} + 2I_0' < D \end{cases}. \quad (11)$$

From the previous expressions, the commutation range can be obtained, as depicted in Fig. 20. It can be observed that an adequate design can achieve ZVS commutation from 40% to 100% load condition, without great reduction in the effective duty cycle.

IV. Design Procedure

From the analysis of the operating stages, one can see that the minimum load condition for the achievement of ZVS commutation must be considered in the MINCIM mode, since that this mode presents the minimum equivalent leakage inductance.

The resonant inductance can be obtained by employing (12), where V_{inmax} is the maximum input voltage, $P_{0\text{min}}$ is the minimum output power to achieve soft commutation, D_{min} is the minimum duty cycle and C_{shunt} is the Thévenin equivalent capacitance over a switch

$$L_d = \frac{V_{in_{\max}}^4}{P_{0_{\min}}}(3D_{\min})^2 \cdot \frac{2C_{\text{shunt}}}{1.5}. \tag{12}$$

It must be also mentioned that the resulting soft switching characteristic, obtained by the proposed modulation technique, is very similar to that in full-bridge phase shift converter [2]. Therefore, the C_{shunt} value is not supposed to be harmful for the switches in any load condition. If no external capacitor is used, the ZVS turning on is maintained. Besides, as there is a trade off between the leakage inductance value and the efficiency, the first stage time interval must not be higher than 5% of the switching period.

The analysis of the static gain of the converter in the MAXCIM mode provides the transformer turns ratio (13). In the design of the transformer core, it must be considered that the waveform coefficient K_f is equal to 4.22 in the area product calculation, since the voltage waveform applied to the transformer winding is modified. Thus, the use of three single-phase transformers will decrease the A_p product by 23%, when compared to a Full-Bridge converter using one single-phase transformer. However, when compared to a Full-Bridge converter employing the association of three transformers, the A_p product is increased by 12%. On the other hand, it must be remembered that the use of a three-phase magnetic core, which is not analyzed in this paper, can reduce the size by about 30%. Such values are obtained [9] considering an EE core type and an efficiency equal to 94%

$$n = \frac{1}{2V_0}\left(V_{in_{\min}} + \sqrt{V_{in_{\min}}^2 - 24V_0 f_s L_d I_0}\right). \tag{13}$$

The output filter inductance is given by (14), which provides a reduction of 33% in its value, when compared to the output inductor used in the full-bridge converter

$$L_0 > \frac{V_{\text{in}}}{12nf_s\Delta I_0}. \tag{14}$$

From the nonlinear model developed in [10], the linearized model of the converter can be obtained as

$$G_{21}(s) = \frac{\Delta v_0}{\Delta d} = 3kV_{\text{in}} \times \frac{r_{SE}C \cdot s + 1}{LC\left(1+\frac{r_{SE}}{R}\right)s^2 + \left[r_{SE} + R_d\left(1+\frac{r_{SE}}{R}\right)C + \frac{L}{R}\right]s + \frac{R_d}{R} + 1} \tag{15}$$

where r_{SE} is the series resistance of the output filter capacitor and R_d is given by (16). Parameter k is unity in MINCIM mode, and equal to 0.5 in VARCIM

$$R_d = 9f_s L_d. \tag{16}$$

TABLE III
Parameters Set

L_{da}=L_{db}=L_{dc}	C_1=...=C_6	L_p	L_s	L_0	f_s
10μH	1nF	871μH	28,8μH	15μH	46kHz

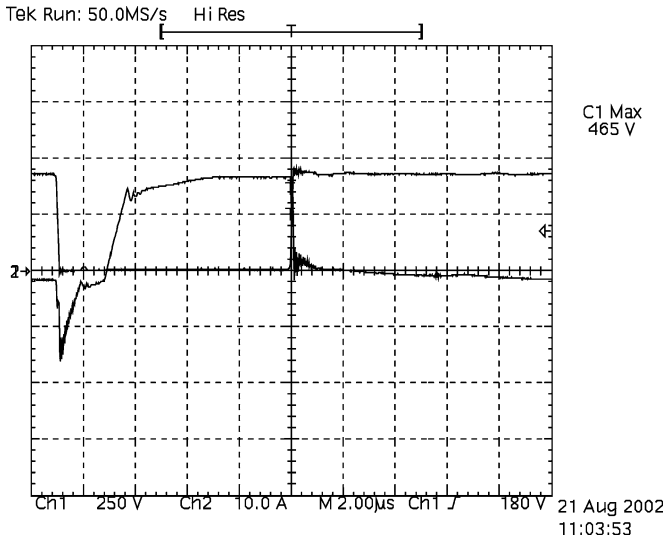

Fig. 21. Current and voltage on switch S_6 and capacitor C_6($C_1 = \ldots = C_6 = 1$ nF).

Despite the difference between the dynamical models, only a single controller can be used. The voltage mode control can be implemented with a digital signal processor as well as with Intersil's IC ISL6558.

V. Experimental Results

In order to demonstrate the theoretical assumptions, experimental tests were performed for $V_{\text{in}} = 420$ V, $V_0 = 60$ V, $P_0 = 6$ kW, as the parameters set presented in Table III is employed. The switches used in the primary side are IGBTs IRG4PC50UD and the semiconductors used in the secondary side are ultra fast diodes HFA50PA60C.

As it can be noticed in Fig. 21, an optimum turning on of the main switches has been achieved. In the turning off of the main switches (Fig. 22), the voltage increase rate is controlled by the external capacitor, reducing overshoot. Moreover, the switches turning off can be improved by increasing the parallel resonant capacitors.

Furthermore, Fig. 23 shows an optimum balance among the primary currents of the transformer. The ZVS commutation for the given parameter set is achieved from 30% to 100% of the maximum output power.

Fig. 24 shows the efficiency of the structure with and without the use of external resonant capacitors. The obtained efficiency at full load was 91.5%. The main source of losses lies in the output rectifier, since the output current always flows through two diodes simultaneously, increasing the conduction and the reverse recovery losses. The use of Schottky diodes can be considered in low voltage applications. However, a three-phase version of the Hybridge rectifier [8] can be used, reducing reverse recovery and conduction losses, because a single diode conducts

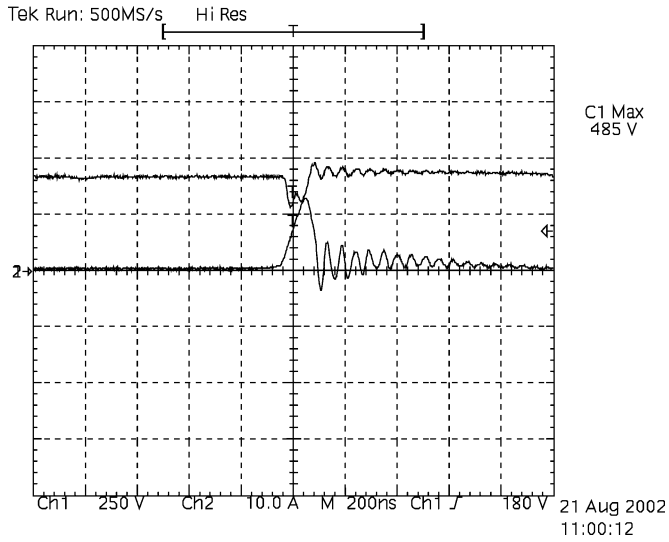

Fig. 22. Detailed view of current and voltage on switch S_6 and capacitor C_6 during turning off ($C_1 = \ldots = C_6 = 1$ nF).

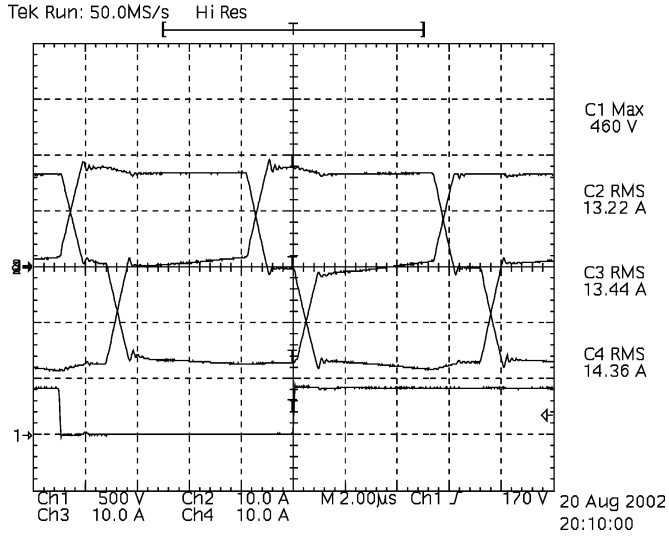

Fig. 23. Currents in the transformer primary side and voltage on switch S_6.

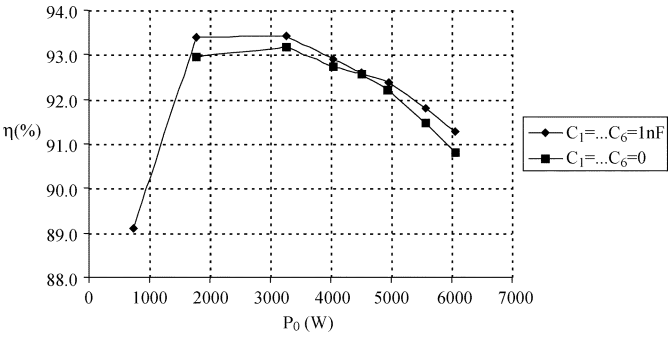

Fig. 24. Measured efficiency of the prototype for $C_1 = \ldots = C_6 = 0$ and $C_1 = \ldots = C_6 = 1$ nF.

the output load current. In addition, Schottky diodes can also be used in the Hybridge Rectifier in low voltage applications.

VI. Conclusion

This paper has presented the application of the asymmetrical duty cycle to the three-phase dc/dc converter. The resulting topology combines the advantages of the three-phase configuration with the ZVS commutation of the main switches for a wide load range. Thus, no extra power semiconductors are necessary. The load range on which ZVS commutation can be obtained, is controlled by adding few power elements (six resonant capacitors and three resonant inductors).

It was verified that the frequency of the output and input currents is six times the switching frequency in MAXCIM mode, while in the MINCIM and VARCIM modes it is three times the switching frequency, reducing the filter size. Besides, there is a reduction in the transformer size if a three-phase core is used.

The characteristics mentioned above establish that the proposed converter achieves high power density. Considering that there is an improvement in the distribution of the losses, it can be assured that this converter is suitable for power levels higher than those employed in the ZVS full-bridge phase-shift converter.

The theoretical analysis has been validated via the experimental results obtained from a laboratory prototype processing 6 kW and operating at 46 kHz.

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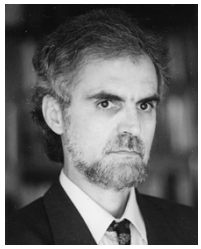

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