A Three-Phase ZVS PWM DC/DC Converter With Asymmetrical Duty Cycle Associated With a Three-Phase Version of the Hybridge Rectifier

Demercil S. Oliveira, Jr. and Ivo Barbi, *Senior Member, IEEE*

Abstract—This paper proposes the use of a three-phase version of the hybridge rectifier in the three-phase zero-voltage switch (ZVS) dc/dc converter with asymmetrical duty cycle. The use of this new rectifier improves the efficiency of the converter because only three diodes are responsible for the conduction losses in the secondary side. The current in the secondary side of the transformer is half the output current. In addition to this, all the advantages of the three-phase dc/dc converter, i.e., the increased frequency of the output and input currents, the improved distribution of the losses, as well as the soft commutation for a wide load range, are preserved. Therefore, the resulting topology is capable of achieving high efficiency and high power density at high power levels. The theoretical analysis, simulation, and experimental results obtained from a 6-kW prototype, and also a comparison of the efficiency of this converter with the full-bridge rectifier are presented.

Index Terms—Full-bridge rectifier, hybridge rectifier, zero-voltage switch (ZVS).

I. INTRODUCTION

NOWADAYS, the main topology used in high power dc/dc conversion is the zero-voltage switch (ZVS) pulse-width modulated (PWM) full bridge converter [1], [2]. It is characterized by four switches operating at high frequency. Soft commutation can be obtained by using phase shift modulation, which preserves its simplicity and provides high power density.

However, at higher power levels, the components face several stresses. As possible solutions, the parallelism of components or even converters can be applied. The former choice increases the complexity of the compromise between the circuit layout and the thermal design. Besides that, one should consider that the dynamic and static current sharing problem limits its application. The other alternative causes redundancy in the control circuits as well as in the number of power components and drivers, increasing the global cost and size of the equipment.

An interesting alternative was proposed by Ziogas in [3]. It uses a three-phase inverter coupled to a three-phase high frequency transformer and to a three-phase high frequency recti-
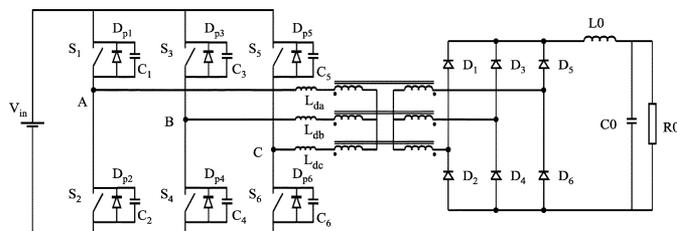
Fig. 1. Three-phase dc/dc ZVS PWM converter associated with the three-phase full-bridge rectifier.
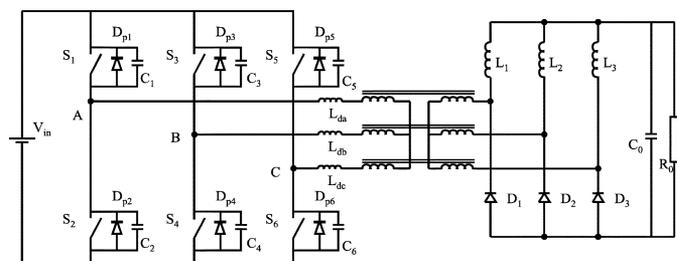

Fig. 2. Three-phase ZVS dc/dc converter associated with the hybridge rectifier.

fier. The resulting advantages consist of the increase of the input and output current frequency by a factor of three compared to the full-bridge converter, lower rms current through power components and reduction of the cores. Although it presents satisfactory advantages, soft commutation has not been achieved, which limits the switching frequency and the power density. Then, the use of asymmetrical duty cycle [4] in the three-phase dc/dc converter was proposed in [5], in order to provide ZVS commutation of all switches for a wide load range, as shown in Fig. 1. Nevertheless, analogously to the full-bridge converter, the resulting topology suffers conduction losses in the rectifier stage, since two series diodes conduct the load current. Therefore, the association of a three-phase dc/dc converter and a three-phase high efficiency rectifier seems to be an optimal arrangement to applications that demand high current levels and low output voltages.

II. PROPOSED THREE-PHASE HYBRIDGE RECTIFIER

In order to overcome the efficiency limit imposed by the full-bridge rectifier used in [5], the extension of the hybridge rectifier [6] to a three-phase version is proposed, as shown in Fig. 2. The rectifier is formed by only three diodes and three inductors, although it provides the same optimum transformer utilization as
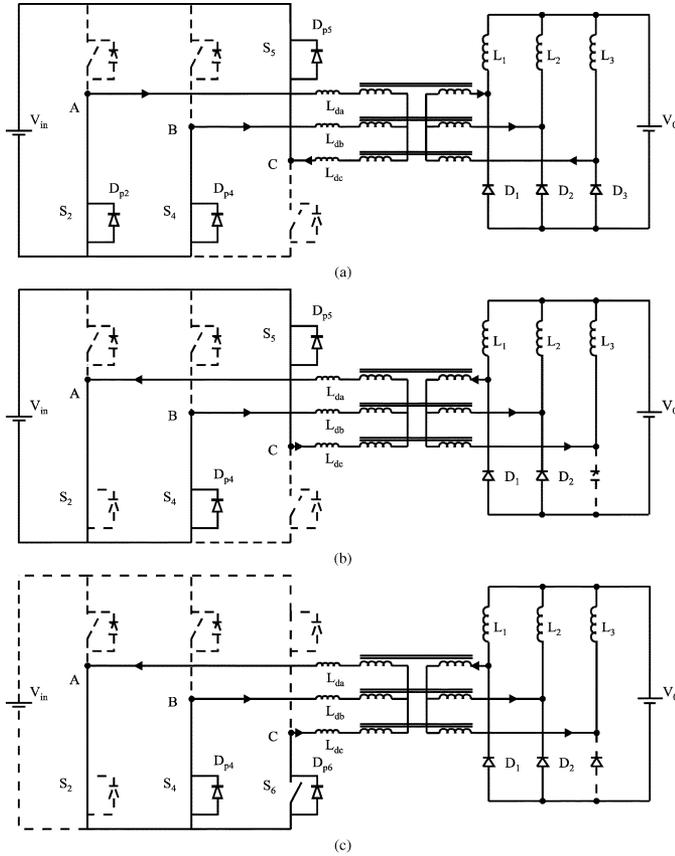
Fig. 3. Topological stages in DMIN operating mode: (a) first stage $[t_0, t_1]$, (b) second stage $[t_1, t_2]$, and (c) third stage $[t_2, t_3]$.

Fig. 4. Main waveforms of DMIN mode.

the six-diode full-bridge rectifier. However, the output inductor volume is increased and the output capacitor is decreased, if the same input current ripple is maintained.

The study of the waveforms relevant to the proposed converter reveals the existence of several operating modes, depending on the duty cycle and the output current. For example if $D < 0.33$, S_1, S_3, and S_5 are never simultaneously on, establishing DMIN mode. If $D > 0.66$, S_2, S_4, and S_6 are never simultaneously on, establishing DMAX mode. Otherwise, DMED mode occurs. Fig. 9 shows clearly the difference among the operating modes. Each operating mode has distinct stages sequences, what can be better comprehended once the static gain curve is obtained

A. Stages in DMIN Operating Mode

The topological stages concerning DMIN operating mode are shown in Fig. 3 and the corresponding waveforms are shown in Fig. 4.

> *First stage* $[t_0, t_1]$—Fig. 3(a): switch S_6 turning off causes the linear transition of all line currents. Rectifier diodes D_1, D_2, and D_3 are forward biased and the currents in the output inductors decrease linearly.
> *Second stage* $[t_1, t_2]$—Fig. 3(b): when current i_{Ldc} reaches i_{L3}, diode D_3 is blocked and energy is transferred to the load.
> *Third stage* $[t_2, t_3]$—Fig. 3(c): switch S_5 turning off ceases the energy transference and causes a freewheeling
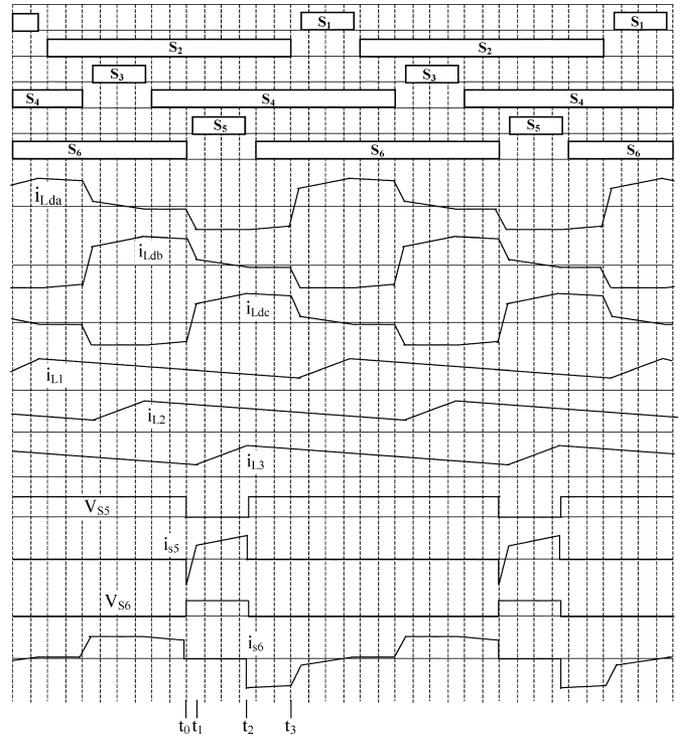
stage to begin, in which all currents and voltages remain constant, until switch S_2 turns off. The same behavior is assumed for the remaining switches.

B. Stages in DMED Operating Mode

The topological stages concerning DMED operating mode are shown in Fig. 5 and the corresponding waveforms are shown in Fig. 6.

> *First stage* $[t_0, t_1]$—Fig. 5(a): switch S_6 turning off causes the linear transition of the line currents in phases a and c. Rectifier diodes D_1 and D_3 conduct and nearly half the input voltage is transferred to the load.
> *Second stage* $[t_1, t_2]$—Fig. 5(b): when current i_{Ldc} reaches i_{L3}, diode D_3 is blocked and energy is transferred to the load.
> *Third stage* $[t_2, t_3]$—Fig. 5(c): the switch S_3 turning off causes D_2 to be forward biased, but energy continues to be transferred to the secondary side until switch S_2 is turned off. The same behavior is assumed for the remaining switches.

C. Stages in DMAX Operating Mode

The topological stages concerning DMAX operating mode are shown in Fig. 7 and the corresponding waveforms are shown in Fig. 8.

> *First stage* $[t_0, t_1]$—Fig. 7(a): switch S_6 turning off causes all rectifier diodes to be forward biased. No energy is transferred to the load and the currents decrease according to the output voltage.
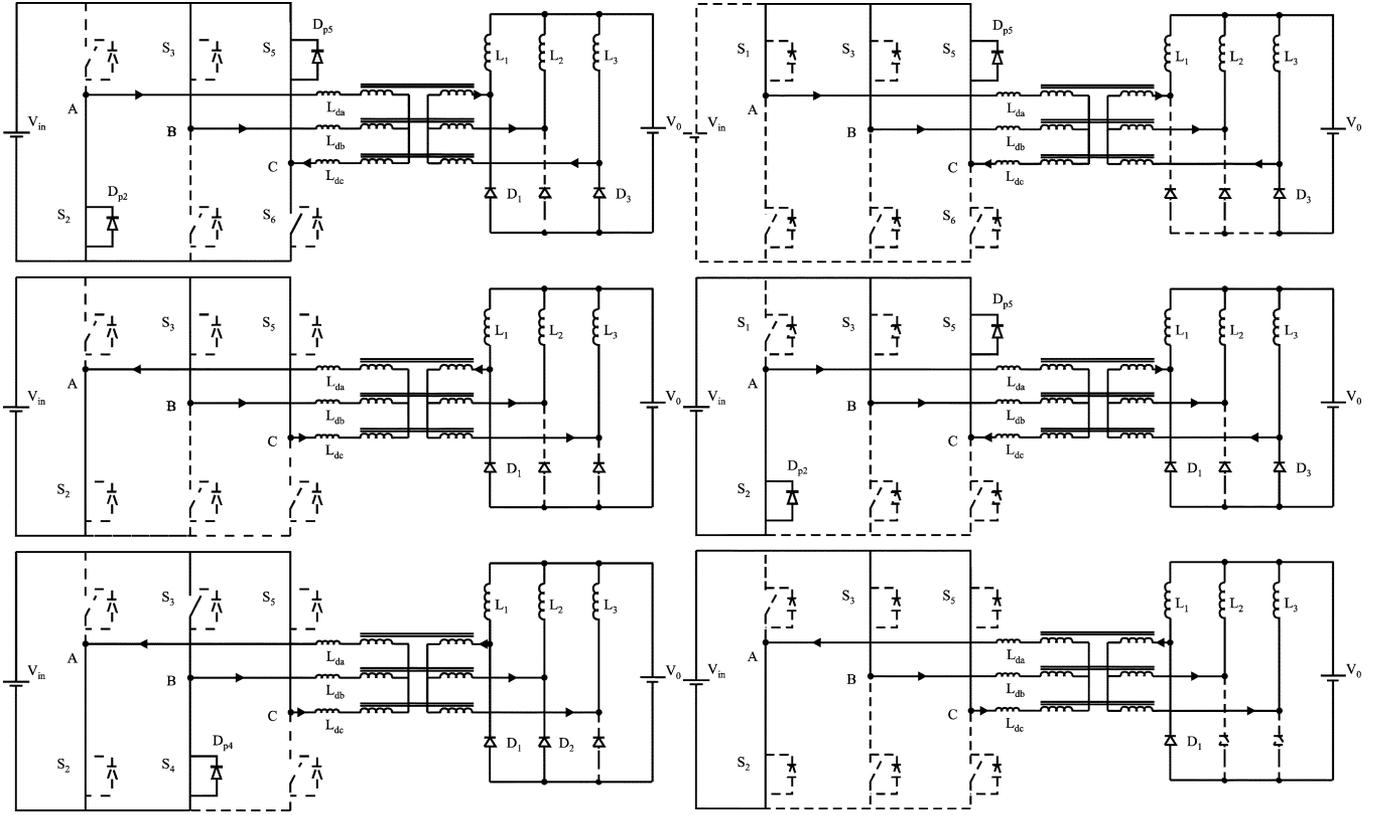
Fig. 5.   Topological stages in DMED operating mode: first stage $[t_0, t_1]$, second stage $[t_1, t_2]$, and third stage $[t_2, t_3]$.

Fig. 7.   Topological stages in DMAX operating mode: first stage $[t_0, t_1]$, second stage $[t_1, t_2]$, and third stage $[t_2, t_3]$.
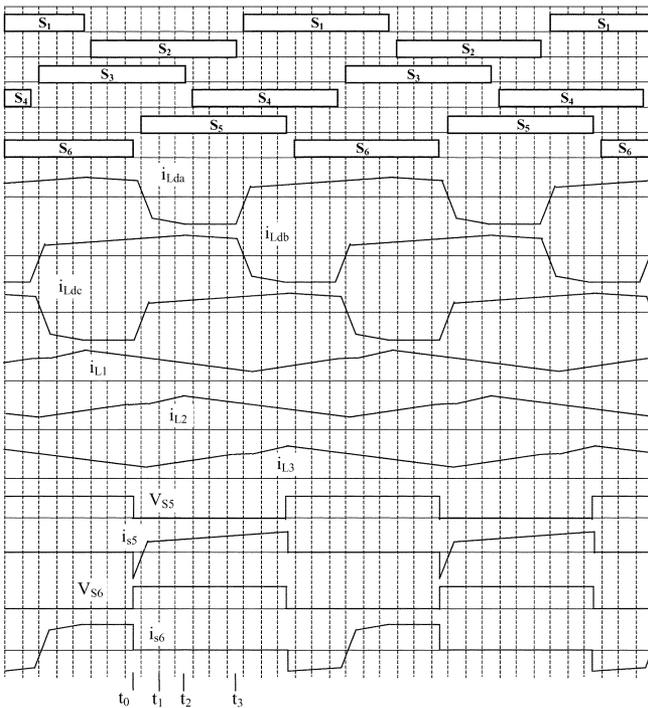

Fig. 6.   Main waveforms of DMED mode.

Second stage $[t_1, t_2]$—Fig. 7(b): when switch S_1 turns off, a linear transition between the line currents a and c begins and half the input voltage is applied to the output filter.

Third stage $[t_2, t_3]$—Fig. 7(c): when the line current in phase c reaches i_{L3}, diode D_3 is blocked and an energy transference stage begins.

According to the aforementioned operating modes, the time intervals and voltages across the output filters corresponding to each topological state can be obtained, as shown in Table I. For simplicity, the parameterized current I_0' and the inductance factor k are defined as in (1) and (2), respectively

$$I_0' = \frac{f_s L_d I_0}{V_{in}} \tag{1}$$

$$k = \frac{L_d}{L_f} \tag{2}$$

where $L_d = L_{da} = L_{db} = L_{dc}$ are the transformer leakage inductances, $L_f = L_1 = L_2 = L_3$ are the output filter inductances, V_{in} is the input voltage and T_s corresponds to the switching period, with all the parameters being referred to the secondary side of the transformer.

According to Table II, the rms currents through the secondary side semiconductors are smaller in mode DMIN. One must consider that if the converter operation is restricted to this mode only, the transformer ratio n is supposed to be halfed, (related to DMED and DMAX design), what doubles the rms primary currents and doubles the voltage across the secondary semiconductors, as shown in Table III. If the converter is designed for the operation in DMED or DMAX modes, the voltages across the secondary semiconductors are 50% greater than in Full-Bridge rectifier and 25% smaller than in a single phase of the hybridge rectifier. Another benefit obtained by the operation in DMED
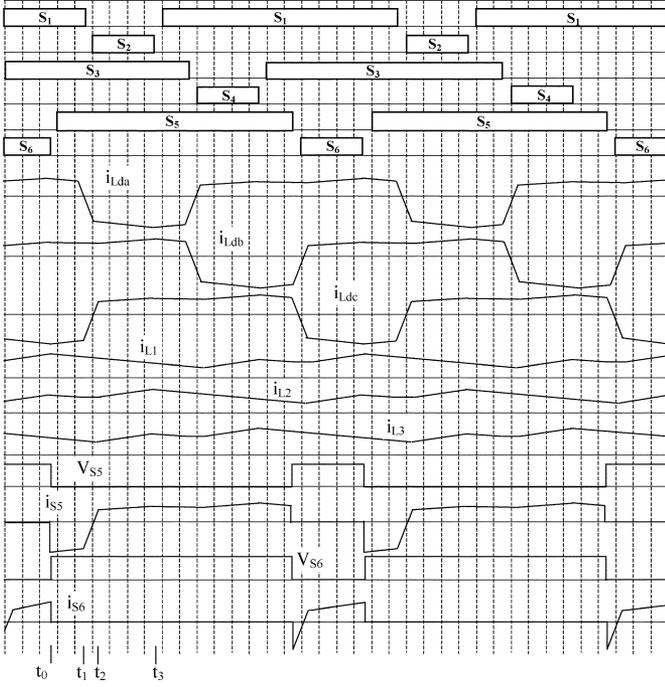
Fig. 8. Main waveforms of DMAX mode.

TABLE I
VOLTAGES ACROSS THE OUTPUT INDUCTORS AND TIME INTERVALS

	DMIN			DMED			DMAX		
	STAGE 1	STAGE 2	STAGE 3	STAGE 1	STAGE 2	STAGE 3	STAGE 1	STAGE 2	STAGE 3
V_{L1}	0	0	0	0	0	0	0	0	0
V_{L2}	0	0	0	$\frac{(V_{in}-V_0)}{3k+2}$	$\frac{(V_{in}-V_0)}{3k+1}$	0	0	$\frac{(V_{in}-2V_0)}{3k+2}$	$\frac{(V_{in}-V_0)}{3k+1}$
V_{L3}	0	$\frac{(V_{in}-V_0)}{1,5k+1}$	0	0	$\frac{(V_{in}-V_0)}{3k+1}$	$\frac{(V_{in}-V_0)}{k+1}$	0	0	$\frac{(V_{in}-V_0)}{3k+1}$
Δt	$I_0' \cdot T_s$	$T_s(D-I_0')$	$T_s\left(\frac{1}{3}-D\right)$	$2I_0' \cdot T_s$	$T_s\left(D-\frac{1}{3}-2I_0'\right)$	$T_s\left(\frac{2}{3}-D\right)$	$T_s\left(D-\frac{2}{3}\right)$	$2I_0' \cdot T_s$	$T_s(1-D-2I_0')$

TABLE II
RMS CURRENTS THROUGH SEMICONDUCTORS

	DMIN	DMED	DMAX
D_1, D_2 and D_3	$\frac{I_0}{3}\sqrt{\frac{5}{3}}$	$\frac{I_0}{\sqrt{3}}$	$\frac{I_0}{\sqrt{3}}$
S_1, S_3, S_5	$\frac{I_0}{3n}\sqrt{D}$	$\frac{I_0}{3n}\sqrt{D}$	$\frac{I_0}{3n}\sqrt{4D-2}$
S_2, S_4, S_6	$\frac{I_0}{3n}\sqrt{\frac{2}{3}-D}$	$\frac{I_0}{3n}\sqrt{2-D}$	$\frac{2I_0}{3n}\sqrt{1-D}$

TABLE III
NORMALIZED VOLTAGE ACROSS SECONDARY RECTIFIER SEMICONDUCTORS

Full-Bridge	One Phase Hybridge	Three-Phase Hybridge (DMIN)	Three-Phase Hybridge (DMED)
1	2	3	1,5

TABLE IV
CONDITIONS OF THE OPERATING MODES AND OUTPUT CHARACTERISTIC

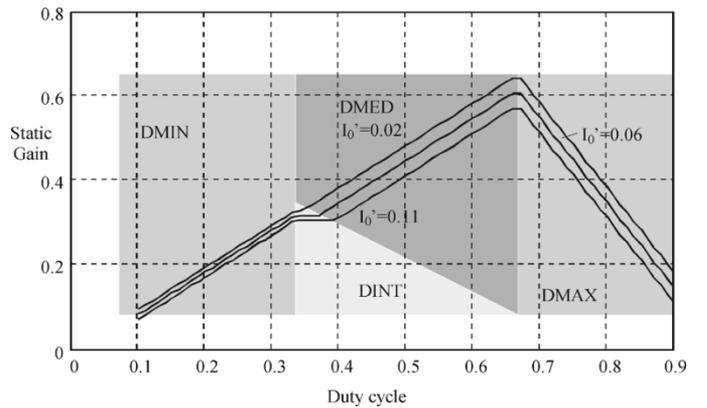|	DMIN	DMED	DMAX
Conditions	$D > I_0 \wedge D \le \frac{1}{3}$	$D > \frac{1}{3} + 2I_0' \wedge D \le \frac{2}{3}$	$D > \frac{2}{3} \wedge D \le 1 - I_0'$
Output characteristic	$G = D - I_0'$	$G = D - 3I_0$	$G = 2 - 2D - 3I_0'$
Load condition for the soft commutation of switches S_2, S_4 e S_6	0	0	$I_0' > \frac{3}{\sqrt{2}}\frac{V_{in}}{Z_0}$
Load condition for the soft commutation of switches S_1, S_3 e S_5	$I_0' > \frac{3}{\sqrt{1.5}}\frac{V_{in}}{Z_0}$	$I_0' > \frac{1.5}{\sqrt{2}}\frac{V_{in}}{Z_0}$	0

Fig. 9. Voltage gain versus duty cycle.

mode is a smaller primary current circulating through antiparallel diodes, what improves efficiency without costs in the soft commutation range. Then, the choice of the operation mode must consider the output voltage level as well as the primary and secondary losses.

III. STATIC GAIN AND SOFT COMMUTATION CONDITION

From the theoretical analysis shown in Table I, one can state the conditions for each operating mode, as well as the respective output characteristic, according to Table IV. One can see that the equations describing each operating mode do not include an interval between DMIN and DMED. During this interval, named DINT, a linear transition stage is interrupted by the turning off of a given switch, giving way to another linear transition stage with a different derivative. Since the output characteristic is constant and given by (3), the operating stages related to DINT are not presented

$$G = \frac{1}{3} - I_0'. \qquad (3)$$

The curve of the static gain versus the duty cycle can be plotted, as shown in Fig. 9. In addition to this, Table IV shows the load condition for soft commutation, where $Z_0 = \sqrt{L_d/C}$. The constant value in the numerator is present because the currents in the output inductors are one third of the output current. The constant value in the denominator represents the leakage association in each operating mode. In the modes where there is

no minimum load condition to achieve ZVS commutation, the output inductors are connected in series with the switches. An important aspect to be mentioned is the existence of a phase shift greater than 180° between modes DMED and DMAX. The control circuit is supposed to limit the operation of the converter in modes DMIN and DMED modes or only in DMAX mode.

IV. DESIGN PROCEDURE

A. Transformer Design

The transformer turns ratio can be obtained from the expression of the static gain, by employing $D_{max} = 0.66$, according to

$$n = \frac{1}{2V_0}\left(V_{in_{\min}}D_{\max} + \sqrt{V_{in_{\min}}^2 D_{\max}^2 - 12V_0 f_s L_d I_0}\right). \tag{4}$$

Considering all losses as a voltage drop in series with the load, one can obtain

$$n = \frac{1}{2(V_0 + \Delta v)}$$
$$\times \left(V_{in_{\min}}D_{\max} + \sqrt{V_{in_{\min}}^2 D_{\max}^2 - 12(V_0 + \Delta v)f_s L_d I_0}\right) \tag{5}$$

where Δv is given by

$$\Delta v = \frac{P_0(1 - \eta)}{I_0}. \tag{6}$$

B. Output Filter Design

From the output current waveform, the output inductance is given by

$$L_0 > \frac{V_{in}}{4n f_s \Delta I_L}. \tag{7}$$

Analogously, the output capacitance can be calculated from (8) and (9), where ΔI_L is the current ripple in each output inductor and ΔV_0 is the output voltage ripple

$$C_0 > \frac{\frac{\Delta I_L}{3}}{12 f_s \Delta V_0} \tag{8}$$

$$R_{SE} < \frac{\Delta V_0}{\frac{\Delta I_L}{3}}. \tag{9}$$

C. Energy Aspects of the Output Filter

The ratio between the total energy stored in the output filter inductors of the three-phase dc/dc converter associated with the three-phase full-bridge rectifier and with the three-phase hybridge rectifier is represented by

$$\frac{E_{FB}}{E_{HY}} = \frac{2k}{3}\left(\frac{2 + \frac{\Delta I_L}{I_0}}{2 + 3\frac{k\Delta I_L}{I_0}}\right)^2 \tag{10}$$

where k is the ratio between the output current ripples in the inductor of each rectifier. In Fig. 10, one can see that if the inductor current ripple is equal to 10% of the load current, the energy stored by the hybridge inductors is about 80% greater than that processed by the full-bridge inductor. On the other hand, the
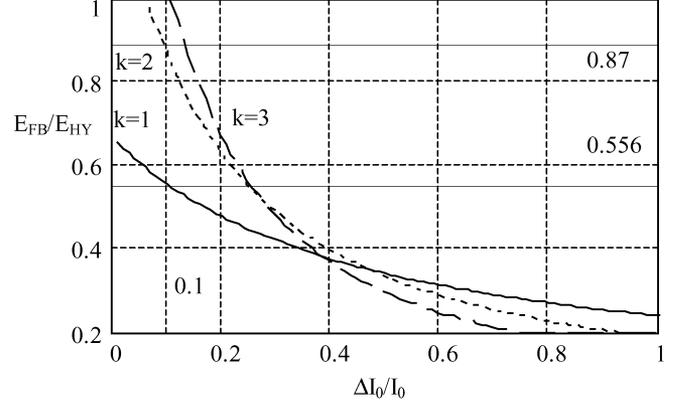

Fig. 10.   Ratio between the energy in the inductors of the full-bridge and hybridge rectifiers.

TABLE V
PROTOTYPE COMPONENTS AND PARAMETERS

$S_1 = \ldots = S_6$	IRG4PC50UD (600V/27A)	$D_1 = \ldots = D_6$	HFA50PA60C (600V/2×25A)
$L_{da} = L_{db} = L_{dc}$	EE42/21/15 N=12 (Thornton) 3x7μH	Transformer	3×EE65/33/39 N=11/3 (Thornton) ($L_{leakage} \cong 3$μH)
L_0	3×EE65/33/39 N=14 3×45μH	C_0	5×330μF/400V

output capacitance is reduced by 66%. For $k = 2$ (i.e., current ripple in the hybridge inductors is twice that of the full-bridge inductor), there is an increase of about 15% in the energy processed by the full-bridge inductor. Therefore, the current ripple choice is a trade off among the inductor volume, core losses, rms current through the semiconductors and efficiency [7], [8].

V. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, an experimental prototype was developed with the following specifications: $V_{in} = 420$ V; $V_0 = 60$ V; $P_0 = 6$ kW; $f_s = 46$ kHz. The parameters and components employed in the tests are shown in Table V.

As it can be noticed in Fig. 11, the waveforms are typically referent to DMED mode. Line currents i_{Lda}, i_{Ldb} and i_{Ldc} are unbalanced, which suggests a special adjustment in the practical implementation of the output inductors. It can also be affirmed that the remaining waveforms validate the theoretical analysis.

The following results were obtained with the converter operating in DMED mode. Fig. 12 shows the current through and voltage across switch S_6, in which ZVS commutation can be observed. Additionally, Fig. 13 presents the waveforms obtained for switch S_5, where one can see that all of the switches commutate in ZVS mode.

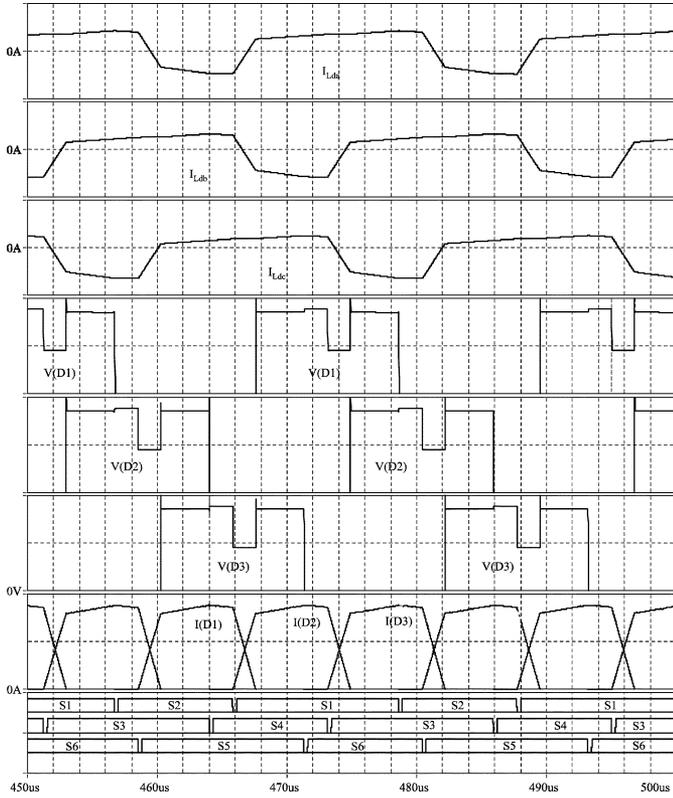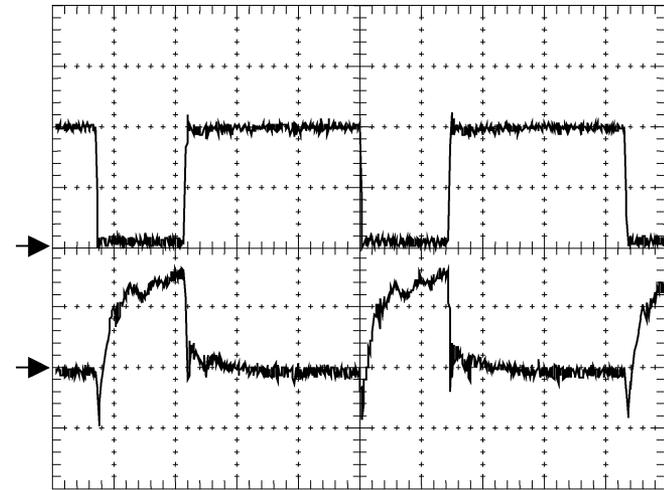Fig. 11. Main waveforms of the circuit in mode DMED obtained via simulation.

Fig. 12. Voltage and current of switch S_6. (Voltage—200 V/div; current—10 A/div; time—5 μs/div).

Fig. 14 shows line currents i_{Lda}, i_{Ldb} and i_{Ldc}. The waveforms demonstrate a satisfactory equilibrium among the line currents. In Fig. 15, one can see the currents through output inductors L_1, L_2 and L_3. A difference equal to 15% of the output current between currents i_{L1} and i_{L3} was measured, although it is considered to be acceptable.

Fig. 16 shows that the use of a three-phase version of the hybridge rectifier improves the efficiency of the three-phase ZVS dc/dc converter with asymmetrical duty cycle in about 2%, when compared to the three-phase full-bridge rectifier. The same components specifications were used in both topologies, except for
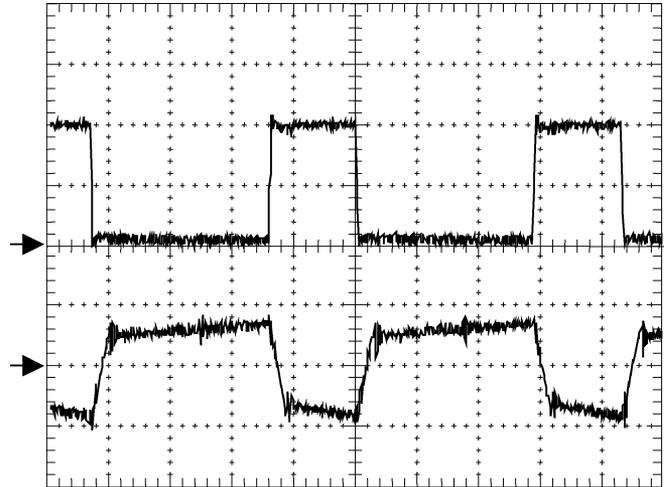

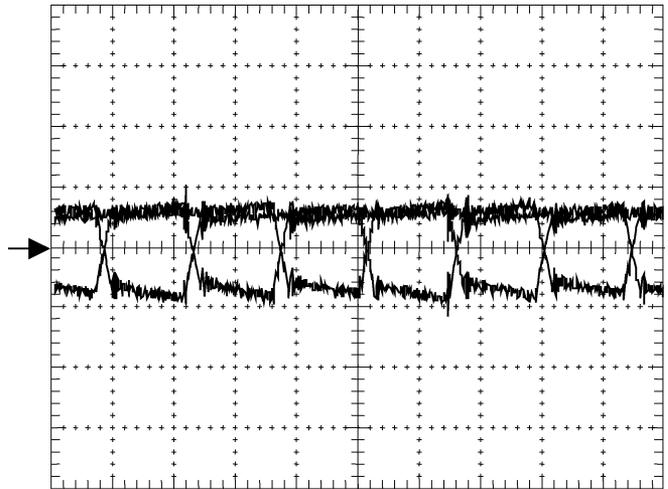Fig. 13. Voltage across switch S_5 and current I_{Ldc}. (Voltage—200 V/div; current—10 A/div; time—5 μs/div).

Fig. 14. Line currents i_{Lda}, i_{Ldb} and i_{Ldc}. (Current—10 A/div; time—5 μs/div).
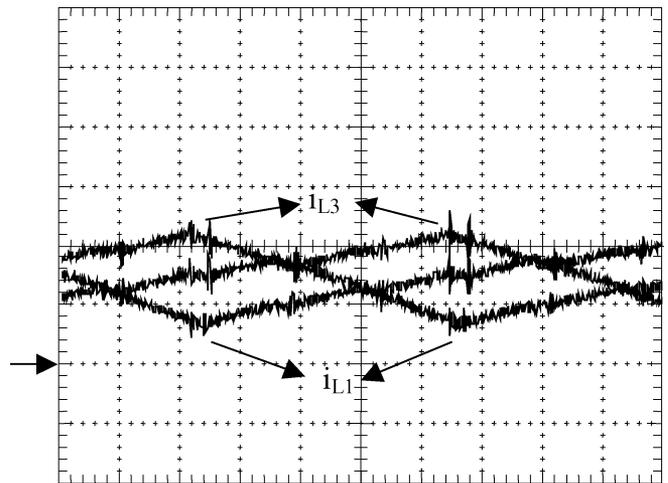

Fig. 15. Currents through output inductors L_1, L_2 and L_3. (Current—20 A/div; time—5 μs/div).

the single output inductor (15 μH) and number of secondary turns (n=2) of the full bridge converter.
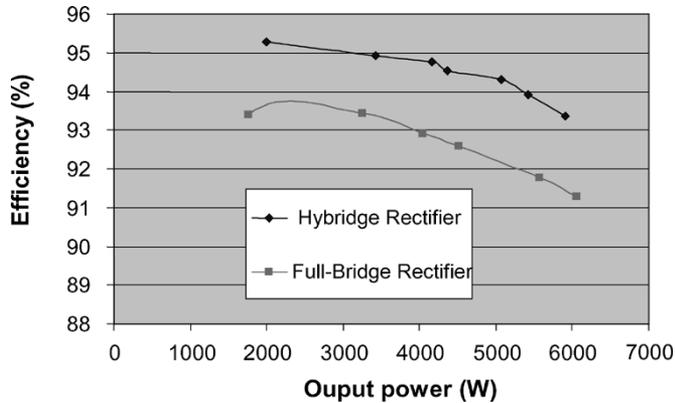
Fig. 16.   Efficiency curve regarding the hybridge and full-bridge rectifiers.

VI. CONCLUSION

From the theoretical and experimental results presented in this paper on the use of the three-phase version of the hybridge rectifier in the three-phase ZVS-PWM dc/dc converter, the authors draw the following conclusions.

1) The efficiency of the developed prototype, operating at 6 kW and 46 kHz, has increased from 91%, using the three-phase full-bridge rectifier, to 93%, using the hybridge rectifier. Despite the increase of the output inductors' volume, the efficiency improvement provides an overall reduction of the converter volume.

2) The operation principle and theoretical analysis have been confirmed by experimentation.

It is the authors' opinion that the proposed converter is suitable for high efficiency and high power density dc/dc conversion applications, particularly in telecommunication facilities.

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Demercil S. Oliveira, Jr. was born in Santos, São Paulo, Brazil, in 1974. He received the B.Sc. and M.Sc. degrees in electrical engineering from the Federal University of Uberlândia, Uberlândia, Brazil, in 1999 and 2001, respectively, and the Ph.D. degree from the Federal University of Santa Catarina, Florianopolis, Brazil, in 2004.

Currently, he is a Researcher in the Group of Power Processing and Control, Federal University of Ceará, Ceará, Brazil. His interest areas include dc/dc conversion, soft commutation, and renewable energy applications.

Ivo Barbi (M'78-SM'90) was born in Gaspar, Santa Catarina, Brazil, in 1949. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina, Florianopolis, Brazil, in 1973 and 1976, respectively, and the Dr.Ing. degree from the Institut National Polytechnique de Toulouse, France, in 1979.

He founded the Brazilian Power Electronics Society, the Power Electronics Institute of the Federal University of Santa Catarina, and created the Brazilian Power Electronics Society. Currently, he is a Professor with the Power Electronics Institute, Federal University of Santa Catarina.

Dr. Barbi has been an Associate Editor in the Power Converters Area of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS since 1992.