Harmonic Voltage Reduction Using a Series Active Filter Under Different Load Conditions

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***Abstract*—This paper proposes a series active filter using a simple control technique. The series active filter is applied as a controlled voltage source contrary to its common usage as variable impedance. It reduces the terminal harmonic voltages, supplying linear or even nonlinear loads with a good quality voltage waveform. The operation principle, control strategy, and theoretical analysis of the active filter are presented. These aspects were proven by the results of numerical simulations. Experimental results of the series active filter demonstrated its good performance under different load conditions.**

***Index Terms*—Harmonic distortion, power filter, series active filter, voltage control.**

I. Introduction

In RECENT decades, the growing and widespread use of electronic equipment by different segments of society is perceptible. This equipment presents itself as nonlinear impedances to its supplying electrical systems and generates harmonic currents with well-known adverse effects, such as low power factor, electromagnetic interference, voltage distortions, etc. These disturbances have required researchers and power electronics engineers to present solutions to minimize or eliminate them [1], [2].

Therefore, the quality of the electrical system, nowadays, is an important matter and, within this context, voltage distortion is the focus of this paper. Thus, if a sinusoidal or good quality voltage waveform must be available at a certain point in the electrical system to supply generic or critical loads, consumers, or to comply with standards and technical recommendations, a voltage filtering system is required (Fig. 1). Passive filtering is a possible solution, but presents several drawbacks. Another possibility would be an ac/dc/ac system, which produces sinusoidal voltages. However, it needs more than one stage of conversion and implies higher costs. Another option is the use of active filters, conceptually established in the 1970s [3]. A series active filter is the appropriate choice to improve voltage waveforms.

Unfortunately, few papers on series active filters have been published in comparison with the number of publications on, for instance, shunt filters. Among these works, one topology, proposed by [4], describes the use of a series filter requiring a power source (usually a dc link) that is supplied by a shunt filter (or an auxiliary source). Still regarding series active filters, a second and third work proposed its use in harmonic current reduction or compensation [5], [6] while a fourth one, combined it with a passive element resulting in a hybrid voltage filter [7]. Different from the concept used in [5], [6] the hybrid filter acts as a controlled voltage source to correct the voltage available to the loads. According to [7], the main problem of the hybrid filter is determining its reference signals (currents and voltages).

This paper proposes a series active filter to reduce harmonic voltages without using an auxiliary source for the dc bus line and it is applied as controlled voltage source contrary to its common use as variable impedance [6]. Equations were developed to determine, in a simple manner, the parameters and components of the active filter. In addition, the control strategy used for the active filter is simple [8], [9].

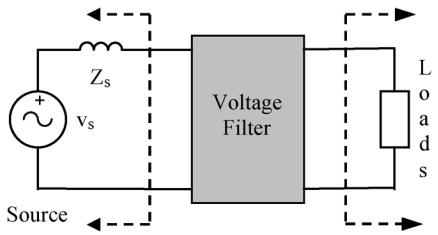

Fig. 1. Voltage filtering system.

II. Configuration of the Series Active Filter and Proposed Control Strategy

The control strategy for the series active filter uses average voltage mode control. It is illustrated in Fig. 2. The series active filter is controlled by monitoring the input voltage $v_s(t)$. From this voltage, by means of function $E(s)$, two signals are obtained: its fundamental component $v_{s1}(t)$ and signal $v_{\rm hr}(t)$, which contains the harmonics to be compensated.

The function $E(s)$ shown in Fig. 2, comprises a tuned-circuit band-pass filter [10], an inverter and an adder. The band-pass filter has a center frequency equals to 60 Hz ($f_{\rm center} = 60$ Hz). Its output signal, $-v_{s1}(t)$, after passing through the inverter yields the fundamental component $v_{s1}(t)$. The input voltage, $v_s(t)$, added to the band-pass filter output signal, $-v_{s1}(t)$, produces the distorted voltage $v_{\rm hr}(t)$.

It is necessary to maintain a constant average voltage (V_d) at the dc bus line of the inverter, therefore, the losses of the inverter and capacitor C_d must be compensated. Voltage $v_d(t)$ is controlled by compensator $H_1(s)$. Its output signal multiplies the sinusoidal signal $(v_{s1}(t))$, which is in phase with and proportional to the fundamental component of the input voltage $v_s(t)$. This results in a sinusoidal signal responsible for the compensation of the above mentioned losses. The sinusoidal signal

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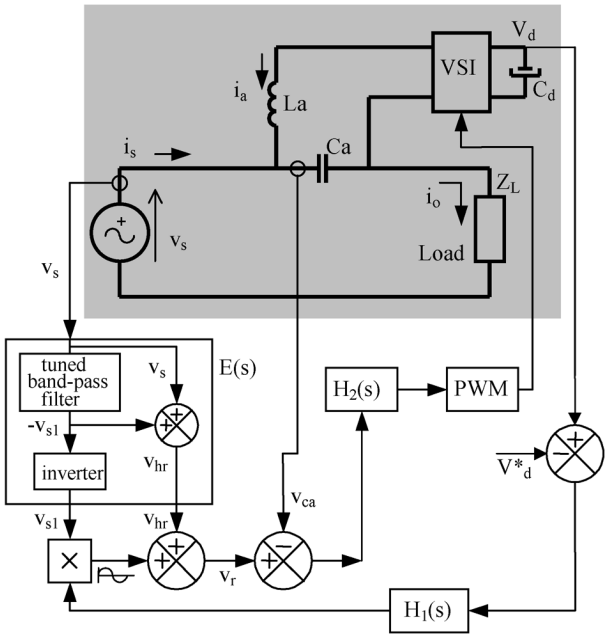

Fig. 2. Harmonic voltage compensator and its control strategy block diagram.

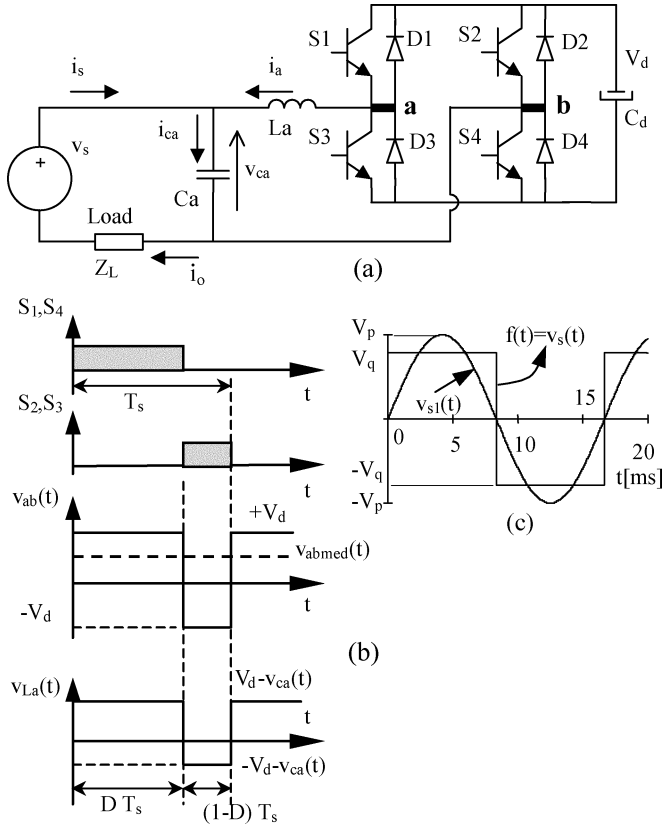

Fig. 3. (a) Series active filter. (b) Waveforms for a switching period. (c) Source voltage waveform.

is added to voltage $v_{\rm hr}(t)$, which contains the information regarding the harmonic content of the input voltage $v_s(t)$. This operation produces a reference voltage, in other words, signal $v_r(t)$ which is to be produced in C_a. This signal and the signal sampled from capacitor C_a are compared to one another and are fed to compensator $H_2(\rm s)$. The compensator commands the inverter, hence, closing the control loop. The output signal of $H_2(\rm s)$ is compared to a triangular waveform, producing, consequently, command signals for the inverter's switches.

Fig. 2 presents a shaded area and from it Fig. 3(a) is derived. Fig. 3(a) shows the voltage source $v_s(t)$, the load with impedance Z_L and the series active filter. All components of the series active filter are clearly drawn, i.e., capacitors C_a and C_d, inductor L_a, switches S_1–S_4 and diodes D_1–D_4. Fig. 3(b) shows the signals applied to the switches, the voltage $v_{ab}(t)$ between terminals $\mathbf{a}$ and $\mathbf{b}$, and the voltage $v_{La}(t)$ across the inductor L_a. Fig. 3(c) presents the input voltage $v_s(t)$, $[f(t) = v_s(t)]$, and its fundamental component $v_{s1}(t)$.

During operation, the inverter's switches are commanded in a complementary manner. During the interval DT_s, switches S_1 and S_4 are on and S_2 and S_3 are off. During the interval $(1 - D)T_s$, this situation is inverted. This characterizes a two-level modulation of the voltage between terminals $\mathbf{a}$ and $\mathbf{b}$.

III. Theoretical Analysis—Main Equations

Voltage $v_{ab}(t)$ varies between $-V_d$ and $+V_d$, as shown in Fig. 3(b). The average value of this voltage $v_{abmed}(t)$, within a switching period, $T_s = 1/f_s$ is defined by (1). It should be observed that (1)–(14) are related to Fig. 3

$$V_{abmed}(t)=\frac{1}{T_s}\left[\int_0^{DTs} V_d dt+\int_0^{(1-D)Ts} -V_d dt\right]=V_d(2D-1). \tag{1}$$

It is determined that during a switching period, T_s, the dc bus line voltage remains constant with an average value of V_d. Duty cycle D is associated with switches S_1 and S_4 and its complement, $(1 - D)$, is associated with S_2 and S_3. The value of interval Δt is defined by

$$\Delta t = DT_s. \tag{2}$$

Voltage $v_o(t)$ across the load must be sinusoidal and a square waveform, $f(t)$, as presented in Fig. 3(c), is used as input voltage $v_s(t)$. Signal $v_s(t)$ has a maximum amplitude equal to V_q, a period of $T = 1/60$ s, $\omega = 2\pi/T$ and making $V_p = (4/\pi)V_q$, $v_s(t)$ can be written as

$$\begin{aligned} v_s(t) &= V_p \sin(\omega t) + V_p\left[\sum_{n=2}^{m}\frac{1}{2n-1}\sin\left[(2n-1)\omega t\right]\right] \\ &= v_1(t) + v_h(t). \end{aligned} \tag{3}$$

A. Duty Cycle D, Current Ripple Δi_a and Inductor L_a

Voltage $v_{ca}(t)$ across capacitor C_a, which contains the harmonics to be filtered, is defined by

$$v_{ca}(t) = \frac{4V_q}{\pi}\left[\sum_{u=2}^{v}\frac{1}{2u-1}\sin\left[(2u-1)\omega_c t\right]\right]. \tag{4}$$

Between terminals a and b, shown in Fig. 3(a), a high frequency waveform is present, composed of a carrier signal and a modulating signal, that is, voltage $v_{ab}(t)$. This voltage is similar to voltage $v_{ca}(t)$. Therefore, voltage $v_{ab}(t)$ is defined by

$$v_{ab}(t) = \frac{4V_q}{\pi}\left[\sum_{n=2}^{m}\frac{1}{2n-1}\sin\left[(2n-1)\omega_a t\right]\right]. \quad (5)$$

Assuming that the switching frequency, f_s, is by far greater than the frequency of the highest order harmonic, in (5), and combining (1), (2), and (5) results in a duty cycle $D(t)$ as

$$D(t) = 0.5\left[1 + \frac{4V_q}{\pi V_d}\left[\sum_{n=2}^{m}\frac{1}{2n-1}\sin\left[(2n-1)\omega_a t\right]\right]\right]. \quad (6)$$

Assuming $V_q = V_d$, as more harmonic components are taken into consideration, the excursion of $D(t)$ tends, in some regions, towards the limit values of 1.0 and 0. In this manner, a voltage modulation index, M_v, is defined as

$$M_v = \frac{V_q}{V_d}. \quad (7)$$

During the conduction interval of S_1 and S_4 of the circuit in Fig. 3(a), the following is obtained:

$$L_a\frac{\Delta i_a(t)}{\Delta t} = V_d - v_{ca}(t). \quad (8)$$

Equations (2), (6), and (4) are substituted into (8) resulting, after some algebra, in

$$\frac{L_a\Delta i_a(t)}{0.5T_s} = \left(\left(1 + \frac{4V_q}{\pi V_d}\left(\sum_{n=2}^{m}\alpha_n\sin(\gamma_n\omega_a t)\right)\right) \times \left(V_d - \frac{4V_q}{\pi}\left(\sum_{u=2}^{v}\alpha_u\sin(\gamma_u\omega_c t)\right)\right)\right)$$
$$\alpha_n = \frac{1}{2n-1} \quad \gamma_n = 2n-1$$
$$\alpha_u = \frac{1}{2u-1} \quad \gamma_u = 2u-1. \quad (9)$$

Factors A and B are designated

$$A = \frac{(4V_q)^2}{\pi^2 V_d}\left(\sum_{n=2}^{m}\alpha_n\sin(\gamma_n\omega_a t)\right)$$
$$B = \left(\sum_{u=2}^{v}\alpha_u\sin(\gamma_u\omega_c t)\right). \quad (10)$$

After multiplying the terms of expression (9) and using (10), the following is obtained:

$$\frac{L_a\Delta i_a(t)}{0.5T_s} = \left(\left(V_d + \frac{4V_q}{\pi}\left(\sum_{n=2}^{m}\alpha_n\sin(\gamma_n\omega_a t)\right) - \frac{4V_q}{\pi}\left(\sum_{u=2}^{v}\alpha_u\sin(\gamma_u\omega_c t)\right) - AB\right)\right). \quad (11)$$

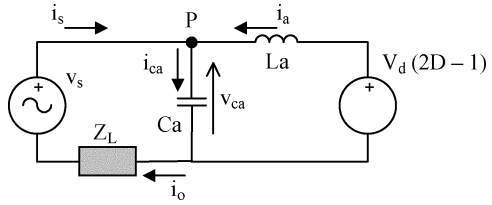

Fig. 4. Equivalent circuit model to the VSI.

The second and third terms at the right side of (11) cancel each other when the series active filter operates properly. Then (11) can be rewritten as

$$\frac{L_a\Delta i_a(t)}{V_d T_s} = \left[0.5 - 2\left(\frac{2V_q}{\pi V_d}\right)^2\left(\sum_{n=2}^{m}\alpha_n\sin(\gamma_n\omega_a t)\right) \times \left(\sum_{u=2}^{v}\alpha_u\sin(\gamma_u\omega_c t)\right)\right]. \quad (12)$$

Equation (7) is replaced into (12) yielding (13), $\overline{\Delta i_a(t)}$, that has denominated the parametric variation of the ripple current through inductor L_a

$$\overline{\Delta i_a(t)} = \left[0.5 - 2\left(\frac{2}{\pi}M_v\right)^2\left(\sum_{n=2}^{m}\alpha_n\sin(\gamma_n\omega_a t)\right) \times \left(\sum_{u=2}^{v}\alpha_u\sin(\gamma_u\omega_c t)\right)\right]$$
$$\overline{\Delta i_a(t)} = \frac{L_a\Delta i_a(t)}{V_d T_s}. \quad (13)$$

The maximum value of (13) is equal to 0.5. Therefore, the value of L_a can be determined by

$$L_a = \frac{0.5V_d}{f_s\Delta i_{a\max}}. \quad (14)$$

B. Transfer Function $\Delta V_{ca}(s)/\Delta D(s)$

The circuit of the converter, considering its average values, at the commutation frequency, has a large signal model as shown in Fig. 4. From this circuit a set of equations can be obtained.

The transfer function, $\Delta V_{ca}(s)/\Delta D(s)$, can be obtained by introducing minimal disturbances in the duty cycle, D, in other words, disturbances with amplitudes equal to ΔD. It is determined that load Z_L is a load with a current source characteristic. As a consequence, the alterations in $i_a(t)$, due to the disturbance in D, will effect current $i_{ca}(t)$, which, in turn, will modify voltage $v_{ca}(t)$. Therefore, introducing this disturbance in the set of equations obtained from the circuit of Fig. 4 and after a few algebraic manipulations (15) is obtained

$$Ga(s) = \frac{\Delta V_{ca}(s)}{\Delta D(s)} = \frac{2V_d}{1 + s^2 L_a C_a}. \quad (15)$$

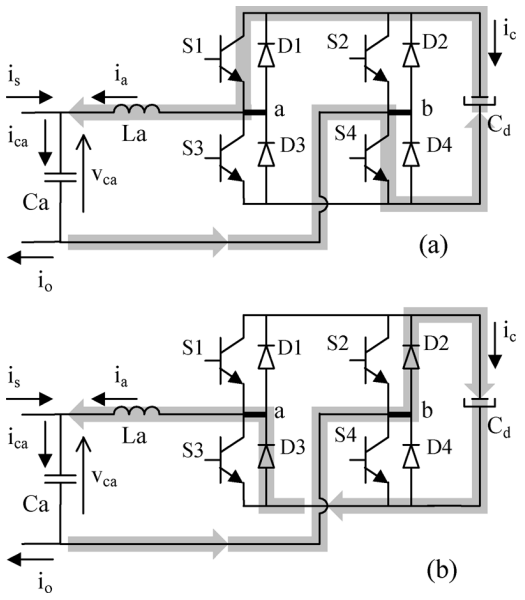

Fig. 5. Active filter operating stages for a switching period.

C. Transfer Function $\Delta V_d(s)/\Delta V_{ca}(s)$

The average voltage V_d at the dc bus line of the inverter must remain constant and this situation demands the use of a controller. In order to select a controller, the variation of the dc bus voltage $v_d(t)$ as a function of the voltage $v_{ca}(t)$ variation, across capacitor C_a, must be known. To obtain this transfer function, the circuits of Fig. 5 containing the operation stages of the active filter during a commutation period, T_s, should be used.

During the interval $D.T_s$, switches S_1 and S_4 are on and conduct the current flowing through capacitor C_d, and during the interval $(1-D).T_s$, switches S_1 and S_4 are off and the current flows through diodes D_2 and D_3. Analyzing this circuit mathematically and after solving its equations, the transfer function $\Delta V_d(s)/\Delta V_{ca}(s)$ is defined as

$$Gd(s) = \frac{\Delta V_d(s)}{\Delta V_{ca}(s)} = \frac{(2D-1)}{s^2 L_a C_d + (2D-1)^2}. \tag{16}$$

D. Coupling Capacitor C_a

The value of inductor L_a is determined according to the variation of the current ripple, which flows through it during a commutation period [see (14)]. Taken into account the L_a inductor value, capacitor C_a can be calculated by defining a resonance or a crossover frequency to the L_aC_a filter. This frequency should be settled between the frequency of the higher order harmonic to be eliminated and 1/4 of the switching frequency. In order to reduce or cancel all odd harmonics a voltage $v_{ca}(t)$ should be produced over capacitor C_a that is given, in another way, by

$$v_{ca}(t) = \begin{cases} V_q - \frac{4}{\pi} V_q \sin(\omega_1 t), & 0 \le t < T/2 \\ -V_q - \frac{4}{\pi} V_q \sin(\omega_1 t), & T/2 \le t < T \end{cases}. \tag{17}$$

Expression (18) will be produced after calculating the root-mean-square (RMS) of (17)

$$v_{caRMS} = \frac{V_q}{\pi}\sqrt{(\pi^2 - 8)}. \tag{18}$$

Additionally, (17) could be rewritten as shown in

$$v_{ca}(t) = \frac{4}{\pi}\frac{V_q}{3}\sin(3\omega_1 t) + \frac{4}{\pi}\frac{V_q}{5}\sin(5\omega_1 t) + \frac{4}{\pi}\frac{V_q}{7}\sin(7\omega_1 t) + \cdots \tag{19}$$

Applying this voltage to the capacitor C_a, reactance X_{ca} is found and it is represented by (20), where $\omega_1 = 2\pi/T$, $T =$ 1/60 s and $(m-1)$ is the number of harmonics considered in (19)

$$X_{ca} = \sqrt{\frac{\sum_{n=2}^{m}\left(\frac{1}{2n-1}\right)^2}{(m-1)(\omega_1 C_a)^2}}. \tag{20}$$

Now, using expression (21) the RMS value of the I_{caRMS} current, circulating through capacitor C_a, can be found. It is an additional parameter that can be used when specifying capacitor C_a

$$v_{caRMS} = X_{ca} I_{caRMS}. \tag{21}$$

E. Capacitor C_d

Another component to be specified is the capacitor C_d. To accomplish this task, it is supposed that the circuit, depicted in Fig. 3(a), has a linear load with impedance Z_L. After analyzing that circuit an expression to the dc bus line voltage is as a function of the capacitor C_d. Expression (22), shown at the bottom of the page, represents the behavior of the voltage $v_d(t)$ where constants and coefficients are defined as follows:

$$\begin{aligned} &C = \cos u \quad C2 = \cos 2u \quad S = \sin u \quad S2 = \sin 2u \\ &c_1 = \sqrt{2}\frac{2V_q}{\omega C_d} I_1 \quad c_2 = \frac{8}{\pi}\sqrt{2}\frac{V_q}{\omega C_d} I_1 \quad c_3 = 8\frac{C_a}{\pi}\frac{V_q^2}{C_d} \\ &c_4 = 8\frac{C_a}{\pi^2}\frac{V_q^2}{C_d} \quad c_5 = \frac{L_a}{C_d} I_1^2 \quad c_6 = 4L_a\frac{C_a}{\pi}\frac{V_q}{C_d}\omega\sqrt{2} I_1 \\ &c_7 = 8L_a\frac{C_a^2}{\pi^2}\frac{V_q^2}{C_d}\omega^2 \quad u = \omega t \end{aligned}.$$

$$v_d(t) = \sqrt{c_1(1-C) - c_2(-0.5CS + 0.5u) + c_3 S + (c_4 + c_5 - c_7)(C2 - 1) - c_6 S2 + V_d^2} \tag{22}$$

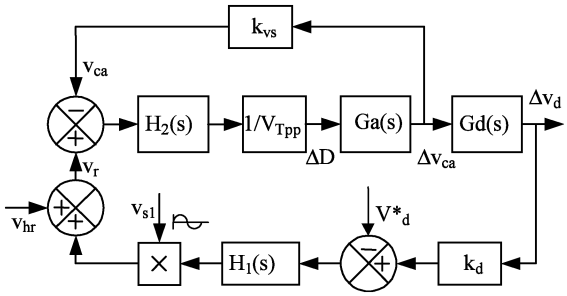

Fig. 6. Control structure of the series active filter.

The voltage $v_d(t)$ aspect and values depend on several parameters, as capacitor C_d, for instance. Thus for a given value of C_d, a certain variation of the voltage $v_d(t)$ will be observed. In this way, the capacitor C_d is established always in accordance with the design limits of the dc bus voltage variation $v_d(t)$.

IV. Project and Numerical Simulation Results

A. Current and Voltage Loop Control

From Fig. 2 the control structure to the series active filter is derived and it is presented in Fig. 6. It illustrates the employment of an inner voltage loop ($v_{ca}(t)$ voltage control) within the outer voltage loop ($v_d(t)$ voltage control) in the closed-loop regulation of the VSI converter.

It is noticed that both transfer functions ($Ga(s) = \Delta V_{ca}(s)/\Delta D(s)$ and $Gd(s) = \Delta V_d(s)/\Delta V_{ca}(s)$) act like second-order low-pass filters. The transfer function $\Delta V_d(s)/\Delta V_{ca}(s)$ depends on the values of D and D varies from 0 to 1. When $0< D <0.5$, it implies that ΔV_d variations are opposite to the ΔV_{ca} variations. If the VSI converter is closed-loop regulated using only the outer voltage loop, and considering $0< D <0.5$, the system will be unstable. But this does not occur because the $v_d(t)$ voltage control includes the $v_{ca}(t)$ voltage loop control.

B. Active Filter Design

An example of the project is described as follows, in which the main components of the active filter are determined, with VSI, which is used in the numerical simulations. The filter is projected to compensate for loads up to 1250 W and has the following specifications: $V_{sp} = 311$ V, $f = 60$ Hz, $V_d = 250$ V, $f_s = 20$ kHz, $\Delta i_{amax} = 25\%\ I_{sp}$ and $C_a = 4.7\ \mu$F. The peak value of the current source is

$$I_{sp} = \frac{2P_o}{V_{sp}} = \frac{2 \times 1250}{311} = 8.04 \text{ A}.$$

The ripple current is calculated as a function of the mains' peak current, in other words: $\Delta_{iamax} = 25\%\ I_{sp} = 0.25 \times 8.04 = 2.01$ A. Inductance L_a is calculated according to (14)

$$L_a = \frac{V_d\overline{\Delta i_a}}{f_s \Delta i_{a\max}} = \frac{250 \times 0.5}{2.01 \times 20000} = 3.11 \text{ mH}.$$

The transfer function is calculated using (15)

$$\frac{\Delta V_{ca}(s)}{\Delta D(s)} = \frac{2V_d}{1 + s^2 L_a C_a} = \frac{500}{1 + s^2 14.62 \times 10^{-9}}.$$

The transfer function of the chosen compensator (PID type) is given by

$$H_2(s) = \frac{V_o(s)}{V_i(s)} = \frac{(1 + sR_2C_2)(1 + sR_3C_1)}{sC_1(R_{ip} + R_2)\left(1 + sC_2\frac{R_{ip}R_2}{R_{ip}+R_2}\right)}. \quad (23)$$

The zeros of this compensator are placed at the resonance frequency determined by L_a and C_a. Its poles are positioned at 0 Hz and 10 kHz. With this data, the components of the circuit are determined and their values are: $C_1 = 1.016 \times 10^{-9}$ F, $C_2 = 4.48 \times 10^{-9}$ F, $R_{ip} = 1.24 \times 10^3\ \Omega$, $R_2 = 2.7 \times 10^3\ \Omega$ and $R_3 = 119.0 \times 10^3\ \Omega$. Substituting these values in (23), the compensator's transfer function will have the following numerical value:

$$H_2(s) = \frac{V_o(s)}{V_i(s)} = \frac{(1 + s120.96\times10^{-6})(1 + s120.90\times10^{-6})}{s28.69\times10^{-6}(1 + s5.311\times10^{-6})}.$$

The open-loop transfer function is presented in (24) as follows. Gain K_{vs}, with which the voltages will be sampled, is equal to 0.0128465

$$\begin{aligned} FTLAv(s) &= \frac{K_{vs}}{V_{Tpp}} Ga(s) H_2(s) \\ &= \frac{0.00128465 \times 500}{1 + s^2 14.62 \times 10^{-9}} \\ &\quad \cdot \frac{(1 + s120.96 \times 10^{-6})(1 + s120.90 \times 10^{-6})}{s28.69 \times 10^{-6}(1 + s5.311 \times 10^{-6})}. \end{aligned} \quad (24)$$

Using the procedure above, the compensator transfer function of $H_1(s)$ is calculated. $H_1(s)$ is a PI type controller and expression (25) presents its transfer function

$$H_1(s) = \frac{V_o(s)}{V_i(s)} = \frac{R_2}{R_1}\frac{(1 + sR_2C_1)}{sR_2C_1} = \frac{(1 + s1.0 \times 1.0^{-3})}{s8.2 \times 1.0^{-3}}. \quad (25)$$

C. Numerical Simulation Results

A series active filter was prepared and simulated. Its power stage diagram is presented in Fig. 7 where S_1 to S_4 are ideal switches with a conducting resistance of 0.3 Ω. Elements E1 and E2 are voltage transducers. They read the reference and the controlled voltage signals.

A R-L type load, with $R = 37\ \Omega$ and $L = 50$ mH, was connected to the active filter at the Vo terminal (Fig. 7). The active filter can be tested with other types of loads. Fig. 8 presents a simulation results related to the R–L load. The distorted voltage $v_s(t)$ and its fundamental component $v_{s1}(t)$ at the ac mains port and also the conditioning voltage $v_{ca}(t)$ are shown in Fig. 8(a). The latter cancels the distortions of the input voltage, yielding a sinusoidal signal $v_o(t)$ over the R–L load. The current $i_o(t)$

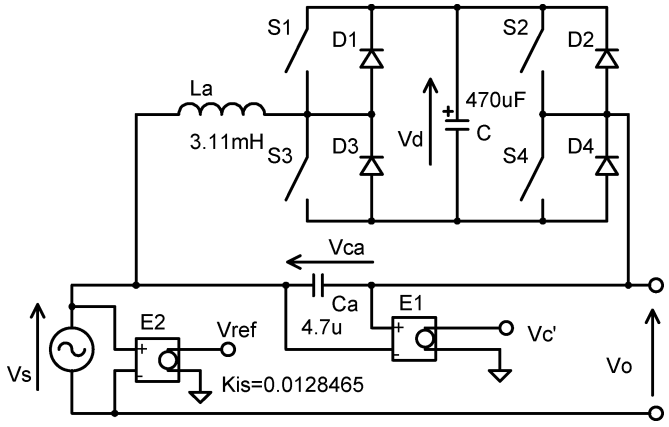

Fig. 7. Simulated power stage circuit.

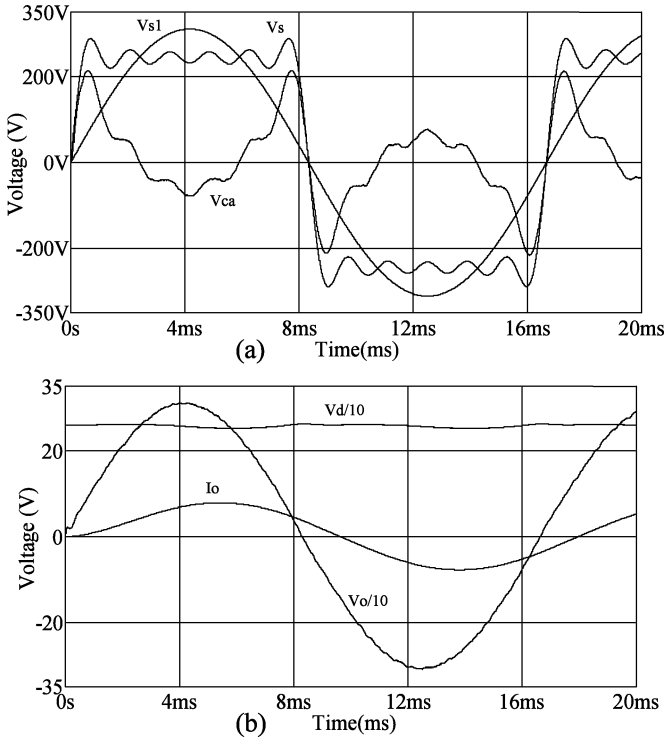

Fig. 8. (a) Input voltages $v_s(t)$, $v_{s1}(t)$ and the harmonic voltage $v_{ca}(t)$. (b) The output and dc bus voltages ($v_o(t)$ and $v_d(t)$), the output current $i_o(t)$.

is displaced around 30° from the voltage $v_o(t)$. The simulation results confirm the ability of the series active filter to generate all required harmonic voltages to cancel the ac mains harmonics content.

V. Experimental Results

In order to verify the principle of operation and control strategy, a 1250-W series active filter has been implemented. Its switching frequency is about 20 kHz. The power stage diagram of the prototype is similar to that shown in Fig. 7. Its parameters and components specifications are the following: $v_s = 220$ Vrms; $v_d = 220$ V; $L_a = 3.17$ mH; $C_a = 4.7$ μF; $C_d = 470$ μF; switches: S_1, S_2, S_3, and S_4 (IGBT module SKM50GB063D). The series active filter control strategy was implemented using discrete electronic components. The

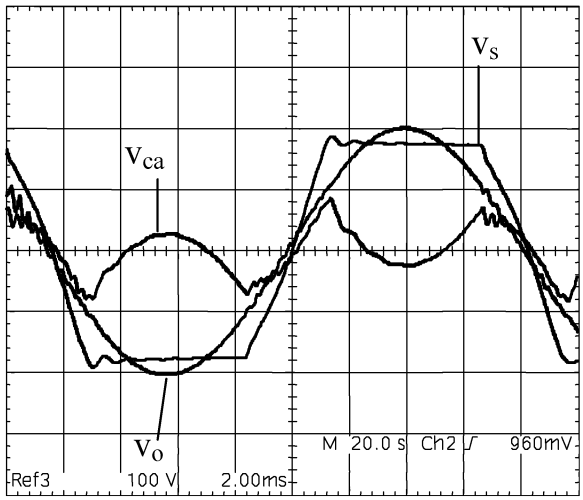

Fig. 9. Input, output and capacitor C_a voltages: $v_s(t)$, $v_o(t)$ and $v_{ca}(t)$ (100 V/div., 2 ms/div.).

compensators calculated in Section IV were used to the experimental prototype.

Fig. 9 presents the experimental result obtained from an active filter connected between the source and a R–L load ($Ro = 30\ \Omega$, $Lo = 50$ mH). Input voltage $v_s(t)$ was obtained from a voltage inverter, which produced a very distorted signal at its output. Input voltage $v_s(t)$ is shown in Fig. 9. In the same figure, output voltage $v_o(t)$ and voltage $v_{ca}(t)$, produced by coupling capacitor C_a, are also shown. The latter is responsible for reducing the harmonics present in the input voltage $v_s(t)$. The input voltage $v_s(t)$ and the output voltage $v_o(t)$ remained in phase. The filter did not introduce phase shifts between these voltages.

Analyzing the graphical aspect of the output voltage $v_o(t)$ (Fig. 9), it can be said that this voltage is substantially better than the input voltage $v_s(t)$. The harmonic content of these voltages was analyzed in quantitative terms. The result of this analysis is presented in Fig. 10.

Fig. 10(a) presents the harmonic spectrum of the input voltage $v_s(t)$. Notice that this voltage presents a large total harmonic distortion ($\mathrm{THD} = 23.36\%$). On the other hand, the total harmonic distortion of the output voltage, $v_o(t)$, presented in Fig. 10(b), compared to the input voltage $v_s(t)$, is much less ($\mathrm{THD} = 0.86\%$). This situation illustrates the performance of the proposed series active filter.

The input and output voltages ($v_s(t)$ and $v_o(t)$) and the output current, $i_o(t)$, are presented in Fig. 11. The output current, $i_o(t)$, is phase shifted approximately 30° in relation to the input voltage (R–L load type). Fig. 12 shows the input, output, and dc bus line voltages ($v_s(t)$, $v_o(t)$, and $v_d(t)$). A constant average voltage V_d is maintained at the dc bus line of the inverter. The voltage $v_d(t)$ has a ripple part designated $v_{d(ca)}(t)$. The graphical aspect of that voltage is different from that predicted by (22). But its amplitude remains around the limits given by (22) for the chosen capacitor C_d.

A load variation was tested. Initially a R–L load with $Ro = 40\ \Omega$ and $Lo = 50$ mH is settled. The series active filter is turned on and while it was operating the Ro value was, suddenly, changed to a new value, i.e., $Ro = 30\ \Omega$. Results of this test can

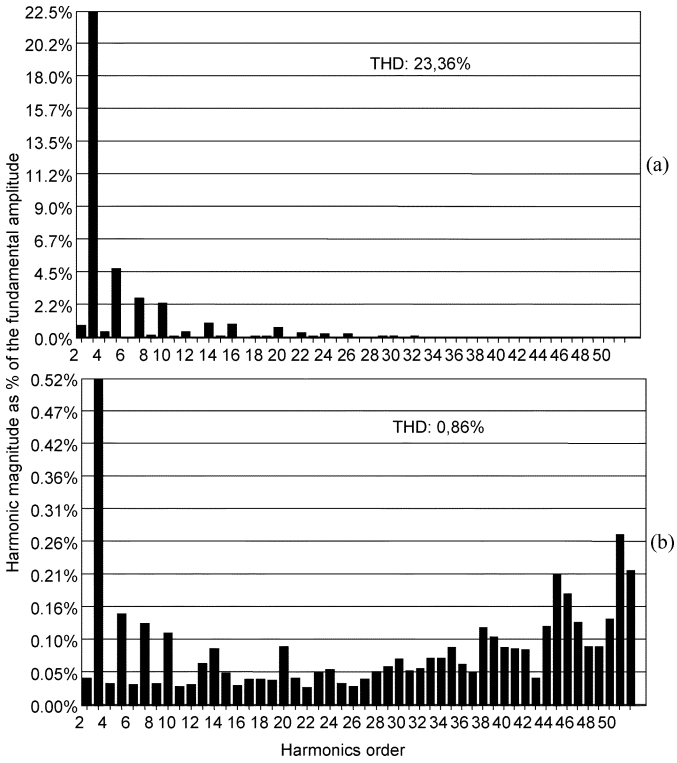

Fig. 10. Input $(v_s(t))$ and output $(v_o(t))$ voltages harmonic content.

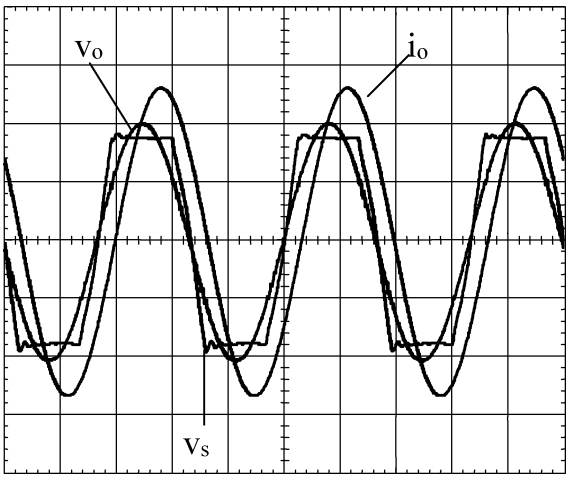

Fig. 11. Input $(v_s(t))$ and output $(v_o(t))$ voltages (100 V/div., 5 ms/div.) and the output current $i_o(t)$ (2 A/div., 5 ms/div.).

be observed in Fig. 13. It shows the input and output voltages $(v_s(t), v_o(t))$ and output current, $i_o(t)$. The load variation did not disturb the output voltage $v_o(t)$ and a few cycles were sufficient to reach the steady-state to the output current $i_o(t)$. Under steady-state operation, Fig. 14 shows the output, inductor and capacitor currents $(i_o(t), i_{La}(t)$, and $i_{Ca}(t))$. One can see in Fig. 14 the graphical aspects of those currents. The inductor and output currents are very close to each other. Then, during a time period of the fundamental component, it can be said that almost all the output current circulates through the inverter structure

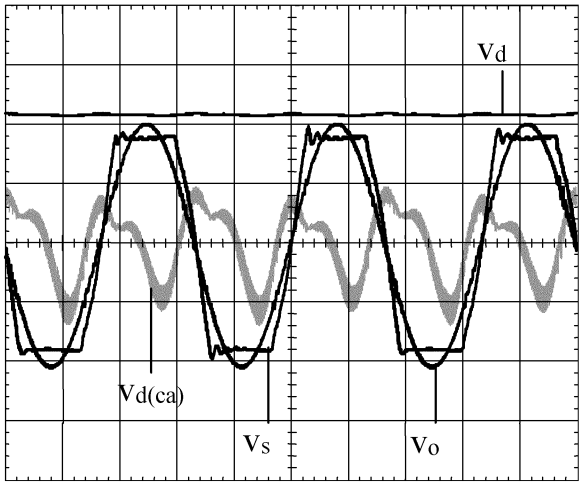

Fig. 12. Input, output and capacitor C_d voltages: $v_s(t)$, $v_o(t)$ and $v_d(t)$ (100 V/div., 5 ms/div.). The ripple voltage $v_{d(ca)}(t)$ (2 V/div., 5 ms/div.).

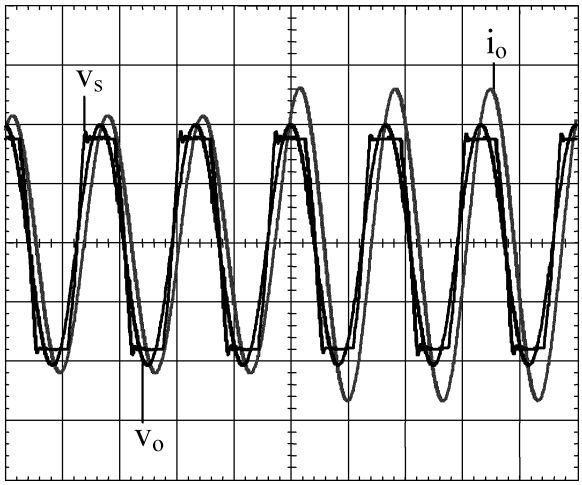

Fig. 13. The input $(v_s(t))$ and output $(v_o(t))$ voltages (100 V/div., 10 ms/div.) and the output current $i_o(t)$ (2 A/div., 10 ms/div.).

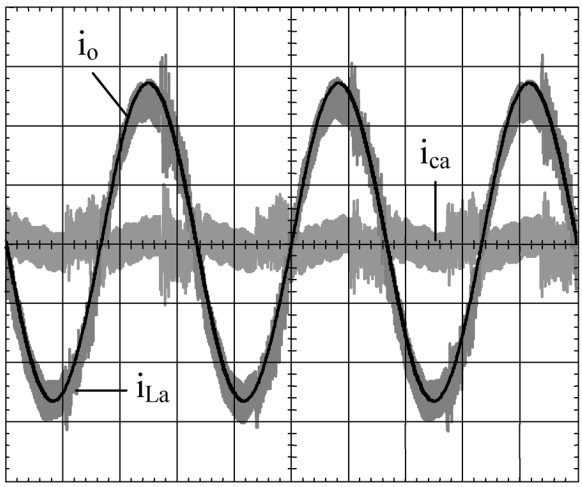

Fig. 14. Output, inductor L_a and capacitor C_a currents: $i_o(t)$, $i_{La}(t)$ and $i_{Ca}(t)$ (2 A/div., 5 ms/div.).

(VSI). Across capacitor C_a flow the currents necessary to produce the canceling voltage $v_{ca}(t)$.

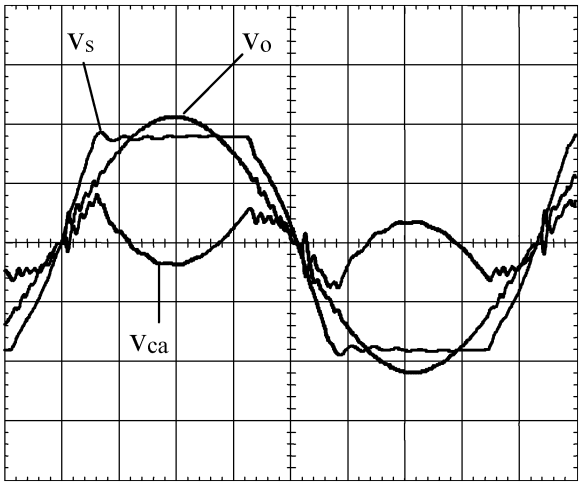

Fig. 15. Input, output, and capacitor C_a voltages: $v_s(t)$, $v_o(t)$ and $v_{\rm ca}(t)$ (100 V/div., 2 ms/div.).

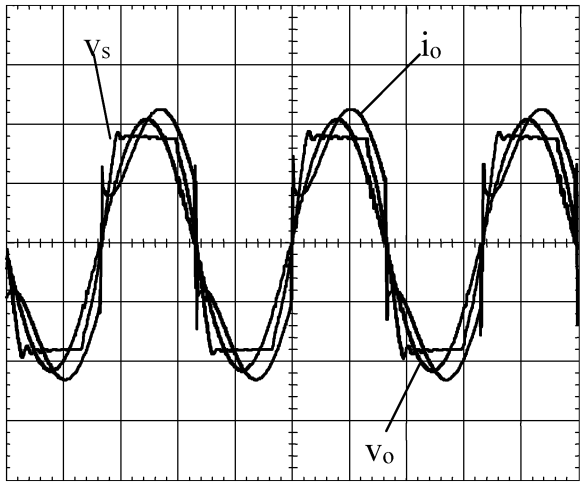

Fig. 17. Input $(v_s(t))$ and output $(v_o(t))$ voltages (100 V/div., 5 ms/div.) and the output current $i_o(t)$ (2 A/div., 5 ms/div.).

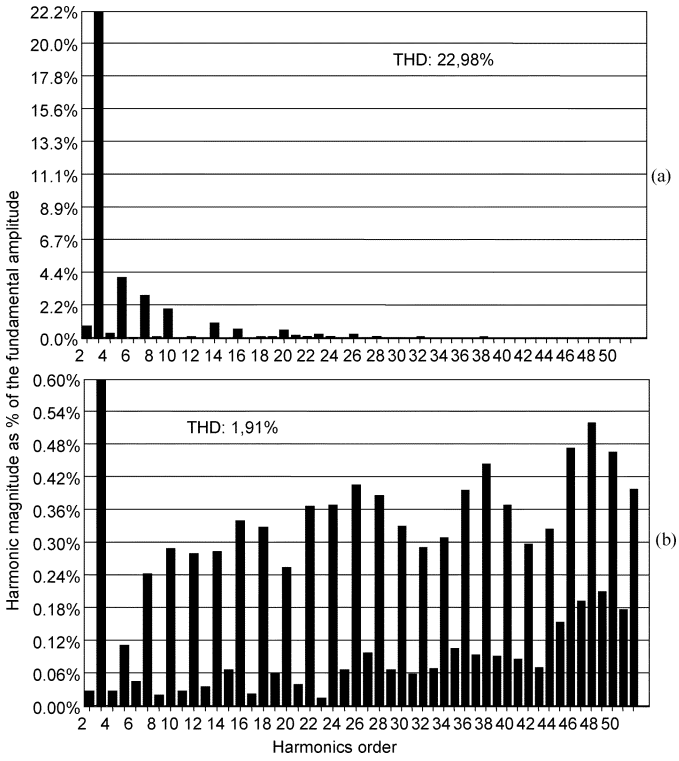

Fig. 16. Input $(vs(t))$ and output $(vo(t))$ voltages harmonic contents.

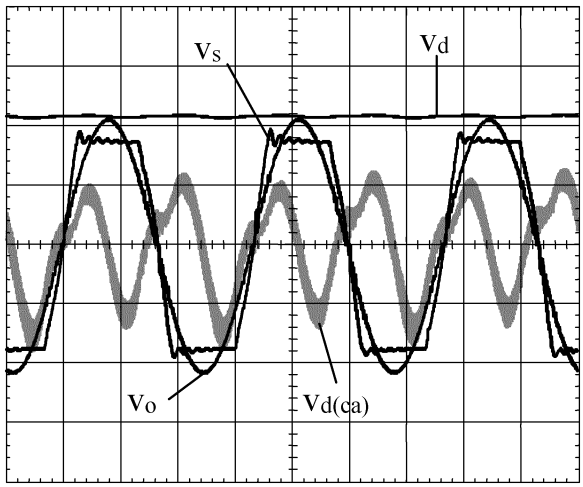

Fig. 18. Input, output, and capacitor C_d voltages: $v_s(t)$, $v_o(t)$ and $v_d(t)$ (100 V/div., 5 ms/div.). The ripple voltage $v_{dca}(t)$ (2 V/div., 5 ms/div.).

A nonlinear load replaced the R-L load used in the previous experiment. The nonlinear load is a full wave rectifier supplying a R-L load ($Ro = 30\ \Omega$ and $Lo = 50$ mH). The distorted input and the load voltages—$v_s(t)$ and $v_o(t)$—are presented in Fig. 15. Also, the conditioning voltage $v_{ca}(t)$ is shown. It reduces the input voltage distortions providing a better waveform to the load.

A quantitative analysis was accomplished using the input $v_s(t)$ and output $v_o(t)$ voltages (Fig. 15) and its result is presented in Fig. 16. According to Fig. 16(a), the input voltage $v_s(t)$ presents a large total harmonic distortion (THD= 22.98%). But the total harmonic distortion of the output voltage, $v_o(t)$, [Fig. 16(b)] compared to the input voltage, is much less (THD= 1.91%). Once more, this shows a good and an appropriate action of the series active filter.

The input and output voltages ($v_s(t)$ and $v_o(t)$) and the output current, $i_o(t)$, are presented in Fig. 17. The output current, $i_o(t)$, is not phase shifted in relation to the input voltage $v_s(t)$ but it is nonlinear. The input, output and dc bus line voltages ($v_s(t)$, $v_o(t)$ and $v_d(t)$) are shown in Fig. 18. A constant average voltage V_d is maintained at the dc bus side of the inverter. The ripple voltage, $v_{d(ca)}(t)$, is also presented. Its graphical aspect is different from that predicted by expression (22). But its amplitude remains around the limits given by (22) for the chosen capacitor C_d. Thus for both experiments the expression (22) gives a good direction to choose the capacitor C_d.

Also a load change was tested with the nonlinear load. The R–L load supplied by the full wave rectifier was modified. The series active filter was turned on with $Ro = 40\ \Omega$ and $Lo = 50$ mH. After a time period Ro was abruptly decreased to a new value: $Ro = 30\ \Omega$. Results of this test can be viewed in Fig. 19. It shows the input and output voltages ($v_s(t)$ and $v_o(t)$) and output current, $i_o(t)$. The output voltage $v_o(t)$ was not disturbed

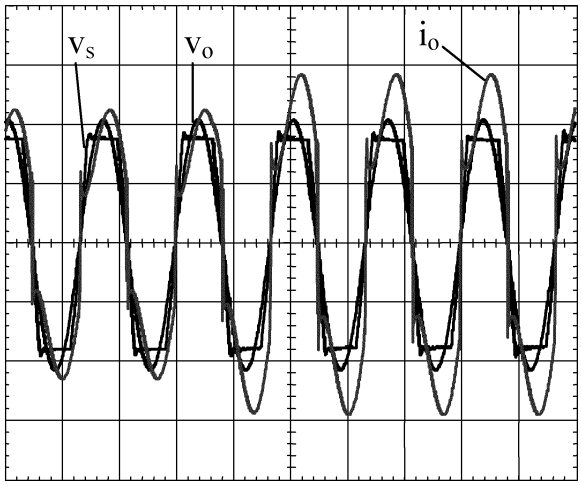

Fig. 19. Input ($v_s(t)$) and output ($v_o(t)$) voltages (100 V/div., 10 ms/div.) and the output current $i_o(t)$ (2 A/div., 10 ms/div.).

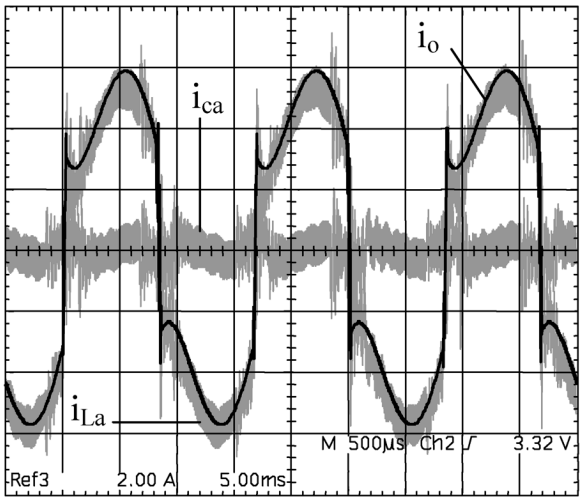

Fig. 20. Output, inductor, L_a and capacitor C_a currents: $i_o(t)$, $i_{La}(t)$ and $i_{Ca}(t)$ (2 A/div., 5 ms/div.).

by the Ro variation and a few cycles were enough to reach the steady-state to the output current $i_o(t)$. The output, inductor and capacitor currents ($i_o(t)$, $i_{La}(t)$, and $i_{Ca}(t)$), under steady-state operation of the series active filter, are shown in Fig. 20. In this figure, the graphical aspect of those currents can be observed. The inductor current, $i_{La}(t)$, follows the output current, $i_o(t)$. As stated before, it can be inferred that almost all the output current circulates through the VSI structure. Across capacitor C_a circulate the currents necessary to yield the conditioning voltage $v_{ca}(t)$.

VI. Conclusion

The proposed series active filter acting as harmonic voltage compensator, its operating principle and its control strategy, were presented. Also, a set of its relevant equations were described. A sinusoidal waveform, from a distorted voltage source, was delivered to the load after being processed by the filter. The filter topology as well as its control strategy is simple and efficient. Experimental results were obtained and validate the theoretical analysis.

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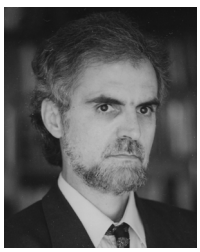

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