A Three-Phase Current-Fed Push–Pull DC–DC Converter

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***Abstract*—In this paper, a new three-phase current-fed push–pull dc–dc converter is proposed. This converter uses a high-frequency three-phase transformer that provides galvanic isolation between the power source and the load. The three active switches are connected to the same reference, which simplifies the gate drive circuitry. Reduction of the input current ripple and the output voltage ripple is achieved by means of an inductor and a capacitor, whose volumes are smaller than in equivalent single-phase topologies. The three-phase dc–dc conversion also helps in loss distribution, allowing the use of lower cost switches. These characteristics make this converter suitable for applications where low-voltage power sources are used and the associated currents are high, such as in fuel cells, photovoltaic arrays, and batteries. The theoretical analysis, a simplified design example, and the experimental results for a 1-kW prototype will be presented for two operation regions. The prototype was designed for a switching frequency of 40 kHz, an input voltage of 120 V, and an output voltage of 400 V.**

***Index Terms*—DC–DC power conversion, HF transformers, multiphase, ripple reduction.**

I. Introduction

THE ELECTRIC power generation, transmission, and distribution employ three-phase systems for economic reasons. The three-phase systems allow higher power density, the use of less material, and higher efficiency than equivalent single-phase systems. In addition, the three-phase systems present constant average power over the time as a result of the phase angle differences. The same advantages encourage the use of three-phase rectifiers and inverters.

Many industrial applications require high-power dc–dc conversion. These applications include distributed generation, uninterruptable power supplies, and transportation. The conventional isolated dc–dc converters use single-phase transformers, which are often big and heavy, and single-phase rectifiers.

Aiming at benefiting from three-phase systems advantages, some work have been done to use dc–dc converters that use a three-phase high-frequency transformer and a three-phase rectifier. These changes contribute to lower volume, weight, and cost of the overall system.

Three-phase dc–dc converters have presented good performance when high-frequency isolation is desired, high components stresses are faced, and the reduction of the filters is required [1]. Some different topologies [2], [3] as well as soft-commutation techniques [2], [4]–[6] were presented.

In recent years, work has been done to apply three-phase dc–dc conversion to fuel cell energy processing [7]–[10] and batteries in automotive devices [11], which exemplify the potential of these converters in applications where the source voltage is low.

This paper proposes a three-phase current-fed dc–dc push–pull converter inspired by the conventional single-phase counterpart. In the proposed converter, the isolation between the power source and the load is provided by a high-frequency three-phase transformer, the losses are better distributed than in a single-phase topology, and the chopping frequencies of the input current and output voltage are three times higher than the switching frequency, which reduces the size requirements for the filter. As in the converter of [12], the active switches are connected to the same reference, which simplifies the gate drive circuits, and presents boost characteristics for a unity transformer turns ratio, but only uses one input inductor.

Potentially, the proposed three-phase dc–dc converter is a good candidate to be widely used in fuel cell and photovoltaic applications.

II. Proposed Three-Phase DC–DC Converter

A. Circuit Description

The circuit of the three-phase current-fed push–pull dc–dc converter is presented in Fig. 1. In this converter, the input boost inductor is placed in series with the power source and connected to the central point (neutral) of the primary side of the wye-wye three-phase transformer. The secondary is connected to a three-phase diode bridge with a capacitive filter, which is in parallel with the load.

B. Modulation

The number of switches simultaneously ON is determined by duty cycle D, which is defined by the time that one switch is ON divided by one switching period. Table I shows the three duty cycle intervals that will be referred to as operation regions R1, R2, and R3.

In region R1, no switches are simultaneously ON, which means that this is a forbidden region of operation since a path for the demagnetization of the inductor does not exist when the only switch that is ON turns off. For this reason, only regions R2 and R3 will be discussed in detail in the following sections for continuous conduction mode (CCM) and discontinuous conduction mode (DCM) operation.

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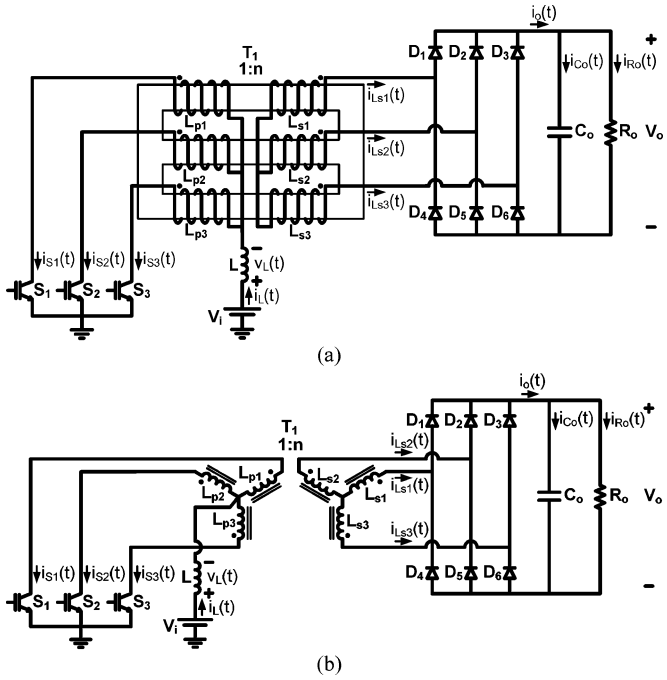

Fig. 1. Circuit of the proposed three-phase current-fed push–pull dc–dc converter. (a) Physical construction of the transformer. (b) Schematic symbol of the transformer.

TABLE I
OPERATION REGIONS

Region	Duty cycle	Switches simultaneously on
R1	0 < D < 1/3	None
R2	1/3 ≤ D ≤ 2/3	Up to two
R3	2/3 < D < 1	Up to three

III. THEORETICAL ANALYSIS

A. CCM Operation in Region R2

In region R2 and considering CCM operation, the proposed converter has six topological stages per switching period that can be described as follows.

Before the first stage, S_3 is already conducting.

1) First stage (t_0, t_1)—Starts when switch S_1 is turned on. Inductor L is magnetized with energy from power source V_i and current $i_L(t)$ increases linearly. The load receives energy from the source through diodes D_2, D_4, and D_6. This topological stage is shown in Fig. 2(a).
2) Second stage (t_1, t_2)—Starts when switch S_3 is turned off. Inductor L is demagnetized and current $i_L(t)$ decreases linearly. The load receives energy from the source and the inductor through diodes D_2, D_3, and D_4. This topological stage is shown in Fig. 2(b).

The third and fifth topological stages are similar to the first stage and the fourth and sixth topological stages are similar to the second stage. The only difference is that other switches are ON. All the topological stages can be seen in Fig. 2. After the sixth stage, the switching period is complete and another period starts with the first stage.

The main theoretical waveforms for CCM operation in region R2 are shown in Fig. 3. The currents and time intervals indicated in Fig. 3 can be expressed as shown in Table II.

Equation (1) is the average voltage across the inductor

$$\frac{3}{T_s}\left[\int_0^{\Delta t_1}\left(V_i-\frac{V_o}{3n}\right)dt+\int_0^{\Delta t_2}\left(V_i-\frac{2V_o}{3n}\right)dt\right]=0. \tag{1}$$

Solving (1) leads to the voltage gain for CCM operation in region R2

$$\frac{V_o}{V_i}=n\frac{1}{1-D}. \tag{2}$$

The inductor current ripple can be expressed for the first stage as (3) and upon substituting Δt_1 and (2) into (3) yields (4)

$$\Delta I_L=\frac{(V_i-(V_o/3n))}{L}\Delta t_1 \tag{3}$$

$$L=\left(\frac{2-3D}{1-D}\right)\left(D-\frac{1}{3}\right)\frac{V_i}{3f_s\Delta I_L}. \tag{4}$$

Equation (4) can be used to calculate the input inductance for this mode of operation.

B. DCM Operation in Region R2

In region R2 and considering DCM operation, the proposed converter has nine topological stages per switching period that can be described as follows.

Before the first stage, S_3 is ON but its current is zero.

1) First stage (t_0, t_1)—Starts when switch S_1 is turned on. Inductor L is magnetized with energy from power source V_i and current $i_L(t)$ increases linearly from zero. The load receives energy from the source through diodes D_2, D_4, and D_6. This topological stage is shown in Fig. 4(a).
2) Second stage (t_1, t_2)—Starts when switch S_3 is turned off. Inductor L is demagnetized and current $i_L(t)$ decreases linearly until zero. The load receives energy from the source and the inductor through diodes D_2, D_3, and D_4. This topological stage is shown in Fig. 4(b).
3) Third stage (t_2, t_3)—Starts when current $i_L(t)$ equals zero. The diodes of the rectifier bridge are OFF and the output capacitor delivers energy to the load. This topological stage is shown in Fig. 4(c).

The fourth and seventh topological stages are similar to the first stage; the fifth and eighth topological stages are similar to the second stage; the sixth and ninth stages are similar to the third stage. The only difference is that other switches are ON. All the topological stages can be seen in Fig. 4. After the ninth stage, the switching period is complete and a new period starts with the first stage.

The main theoretical waveforms for DCM operation in region R2 are shown in Fig. 5. The currents and time intervals can be described as presented in Table III. The DCM voltage gain, which is dependent on the duty cycle and the output current, will be presented Section III-E.

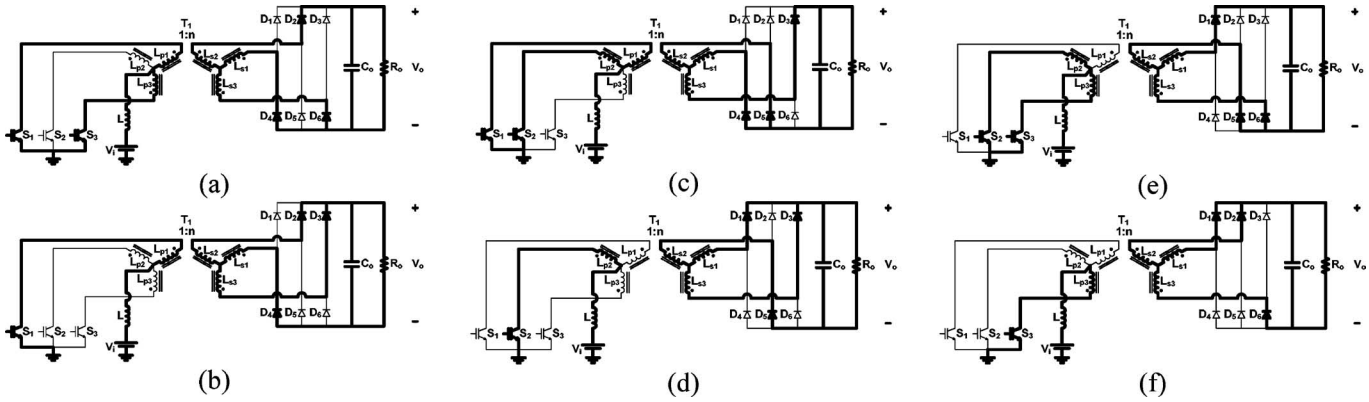

Fig. 2. Topological stages for CCM operation in region R2. (a) First stage (t_0, t_1). (b) Second stage (t_1, t_2). (c) Third stage (t_2, t_3). (d) Fourth stage (t_3, t_4). (e) Fifth stage (t_4, t_5). (f) Sixth stage (t_5, t_6).

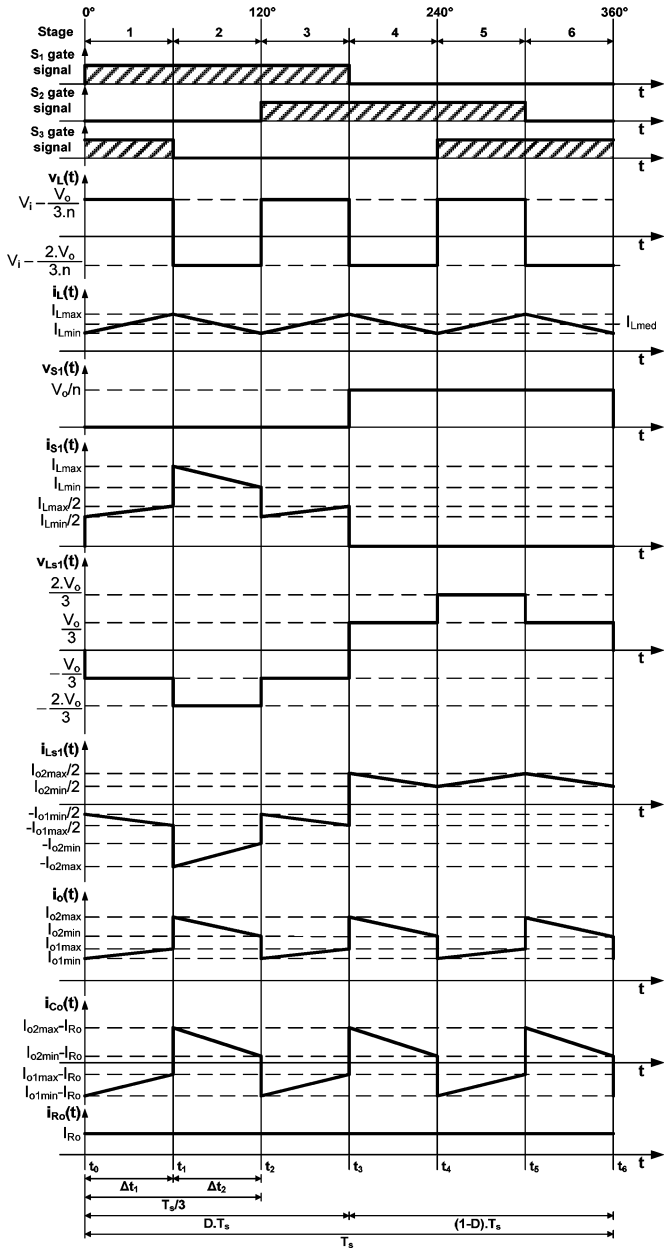

Fig. 3. Main theoretical waveforms for CCM operation in region R2.

TABLE II
EQUATIONS FOR THE CURRENTS AND TIME INTERVALS OF FIG. 3

Currents		Time Intervals
$I_{o1\min} = \frac{I_{L\min}}{3 \cdot n}$	$I_{o1\max} = \frac{I_{L\max}}{3 \cdot n}$	$\Delta t_1 = \left(D - \frac{1}{3}\right) \cdot T_s$
$I_{o2\min} = \frac{2 \cdot I_{L\min}}{3 \cdot n}$	$I_{o2\max} = \frac{2 \cdot I_{L\max}}{3 \cdot n}$	$\Delta t_2 = \left(\frac{2}{3} - D\right) \cdot T_s$

C. CCM Operation in Region R3

In region R3 and considering CCM operation, the proposed converter has six topological stages per switching period that can be described as follows.

Before the first stage, S_2 and S_3 are already conducting.

1) First stage (t_0, t_1)—Starts when switch S_1 is turned on. Inductor L is magnetized with energy from power source V_i and current $i_L(t)$ increases linearly. The diodes of the rectifier bridge are OFF and the output capacitor delivers energy to the load. This topological stage is shown in Fig. 6(a).
2) Second stage (t_1, t_2)—Starts when switch S_2 is turned off. Inductor L is demagnetized and current $i_L(t)$ decreases linearly. The load receives energy from the source and the inductor through diodes D_2, D_4, and D_6. This topological stage is shown in Fig. 6(b).

The third and fifth topological stages are similar to the first stage and the fourth and sixth topological stages are similar to the second stage. The only difference is that other switches are ON. All the topological stages can be seen in Fig. 6. After the sixth stage, the switching period is complete and a new period starts with the first stage.

The main theoretical waveforms for CCM operation in region R3 are presented in Fig. 7. The currents and time intervals indicated in Fig. 7 can be expressed as shown in Table IV.

Equation (5) is the average voltage across the inductor

$$\frac{3}{T_s}\left[\int_0^{\Delta t_1} V_i\, dt + \int_0^{\Delta t_2} \left(V_i - \frac{V_o}{3n}\right) dt\right] = 0. \qquad (5)$$

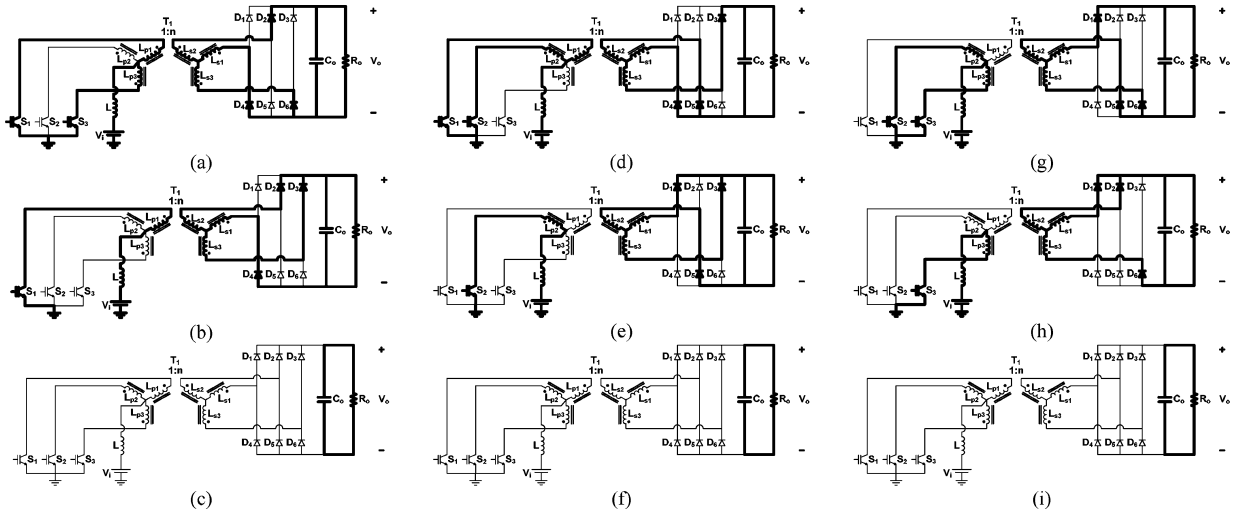

Fig. 4. Topological stages for DCM operation in region R2. (a) First stage (t_0, t_1). (b) Second stage (t_1, t_2). (c) Third stage (t_2, t_3). (d) Fourth stage (t_3, t_4). (e) Fifth stage (t_4, t_5). (f) Sixth stage (t_5, t_6). (g) Seventh stage (t_6, t_7). (h) Eighth stage (t_7, t_8). (i) Ninth stage (t_8, t_9).

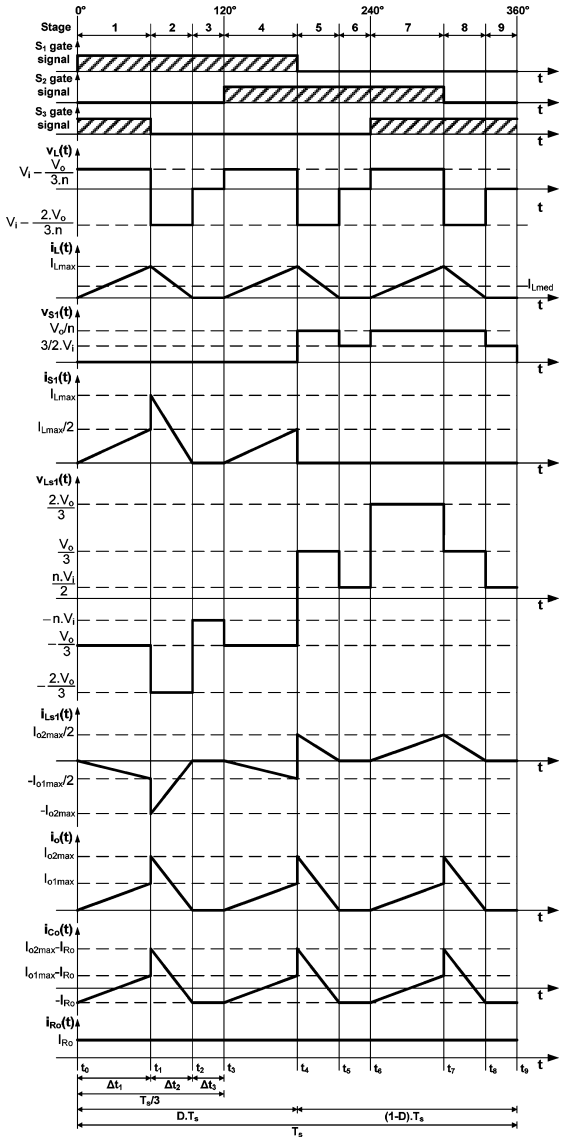

Fig. 5. Main theoretical waveforms for DCM operation in region R2.

TABLE III
EQUATIONS FOR THE CURRENTS AND TIME INTERVALS OF FIG. 5

Currents	Time Intervals
$I_{o1\max} = \frac{I_{L\max}}{3 \cdot n}$	$\Delta t_1 = \left(D - \frac{1}{3}\right) \cdot T_s$
$I_{o2\max} = \frac{2 \cdot I_{L\max}}{3 \cdot n}$	$\Delta t_2 = \left[\left(V_i - \frac{V_o}{3 \cdot n}\right) \Big/ \left(\frac{2 \cdot V_o}{3 \cdot n} - V_i\right)\right] \cdot \Delta t_1$
	$\Delta t_3 = \frac{T_s}{3} - \Delta t_1 - \Delta t_2$

Solving (5) leads to the voltage gain for CCM operation in region R3

$$\frac{V_o}{V_i} = n \frac{1}{1 - D}. \tag{6}$$

The inductor current ripple of the first stage can be expressed as (7) and upon substituting Δt_1 into (7) yields (8)

$$\Delta I_L = \frac{V_i}{L} \Delta t_1 \tag{7}$$

$$L = \left(D - \frac{2}{3}\right) \frac{V_i}{f_s \Delta I_L}. \tag{8}$$

Equation (8) can be used to calculate the input inductance for this mode of operation.

D. DCM Operation in Region R3

In region R3 and considering DCM operation, the proposed converter has nine topological stages per switching period that can be described as follows.

Before the first stage, S_2 and S_3 are ON but their current is zero.

1) First stage (t_0, t_1)—Starts when switch S_1 is turned on. Inductor L is magnetized with energy from power source V_i and current $i_L(t)$ increases linearly from zero. The diodes of the rectifier bridge are OFF and the output capacitor

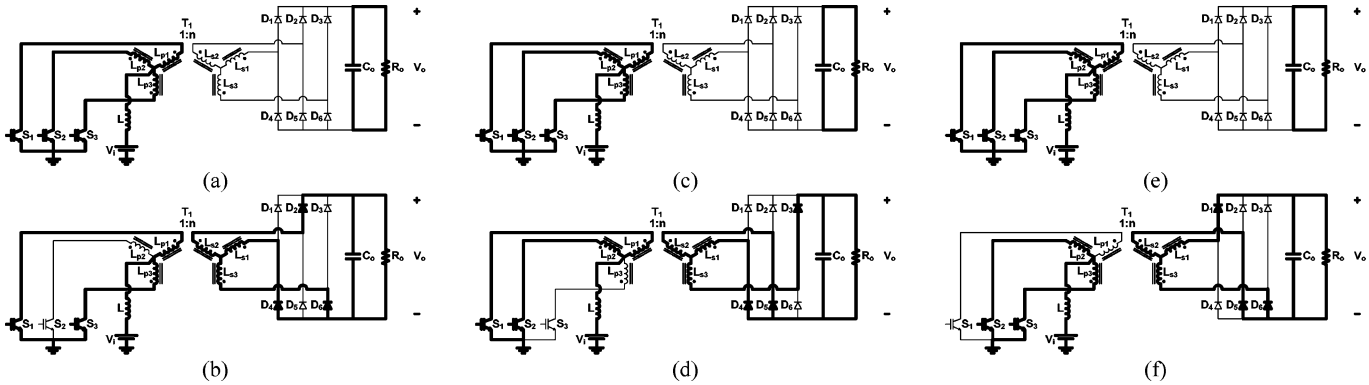

Fig. 6. Topological stages for CCM operation in region R3. (a) First stage (t_0, t_1). (b) Second stage (t_1, t_2). (c) Third stage (t_2, t_3). (d) Fourth stage (t_3, t_4). (e) Fifth stage (t_4, t_5). (f) Sixth stage (t_5, t_6).

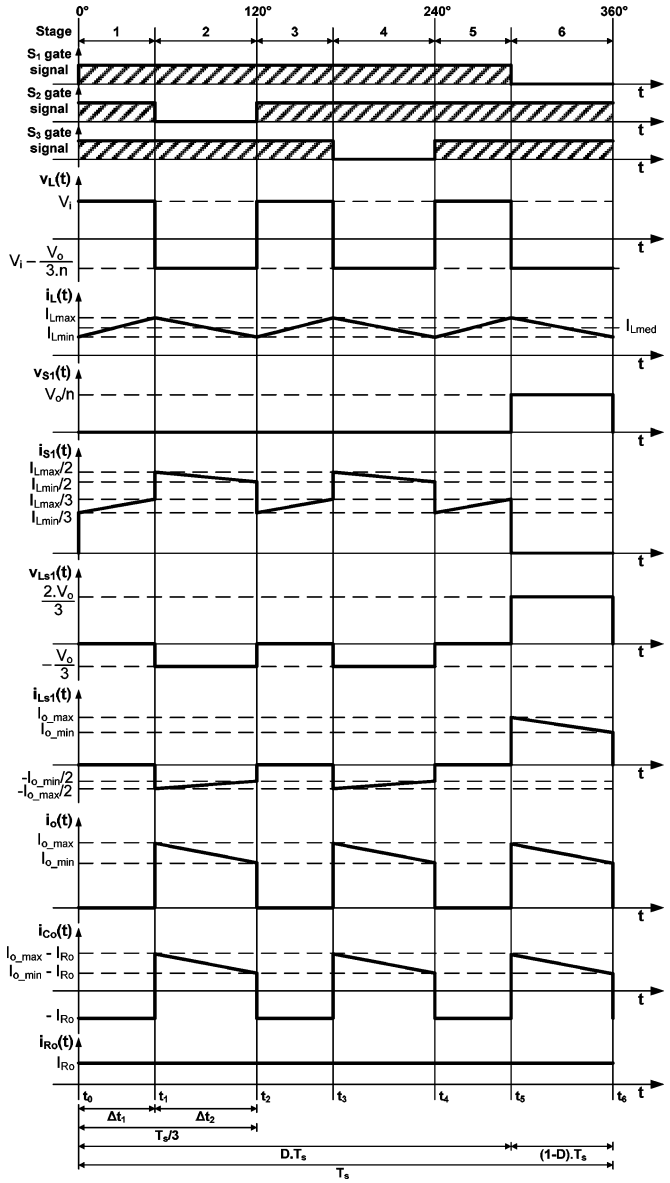

Fig. 7. Main theoretical waveforms for CCM operation in region R3.

TABLE IV
EQUATIONS FOR THE CURRENTS AND TIME INTERVALS OF FIG. 7

Currents	Time Intervals
$I_{o\_\min} = \frac{I_{L\min}}{3 \cdot n}$	$\Delta t_1 = \left(D - \frac{2}{3}\right) \cdot T_s$
$I_{o\_\max} = \frac{I_{L\max}}{3 \cdot n}$	$\Delta t_2 = (1 - D) \cdot T_s$

delivers energy to the load. This topological stage is shown in Fig. 8(a).

2) Second stage (t_1, t_2)—Starts when switch S_2 is turned off. Inductor L is demagnetized and current $i_L(t)$ decreases linearly to zero. The load receives energy from the source and the inductor through diodes D_2, D_4, and D_6. This topological stage is shown in Fig. 8(b).
3) Third stage (t_2, t_3)—Starts when current $i_L(t)$ equals zero. The diodes of the rectifier bridge are OFF and the output capacitor delivers energy to the load. This topological stage is shown in Fig. 8(c).

The fourth and seventh topological stages are similar to the first stage; the fifth and eighth topological stages are similar to the second stage; the sixth and ninth stages are similar to the third stage. The only difference is that other switches are ON. All the topological stages can be seen in Fig. 8. After the ninth stage, the switching period is complete and a new period starts with the first stage.

The main theoretical waveforms for DCM operation in region R3 are shown in Fig. 9, whose currents and time intervals can be described as presented in Table V. The voltage gain for DCM operation in region R3 will also be presented in the next section.

E. Output Characteristic

Using the voltage gain equations of the converter in each of the four operational modes already presented and the equations describing the limits between them (Table VI), the output

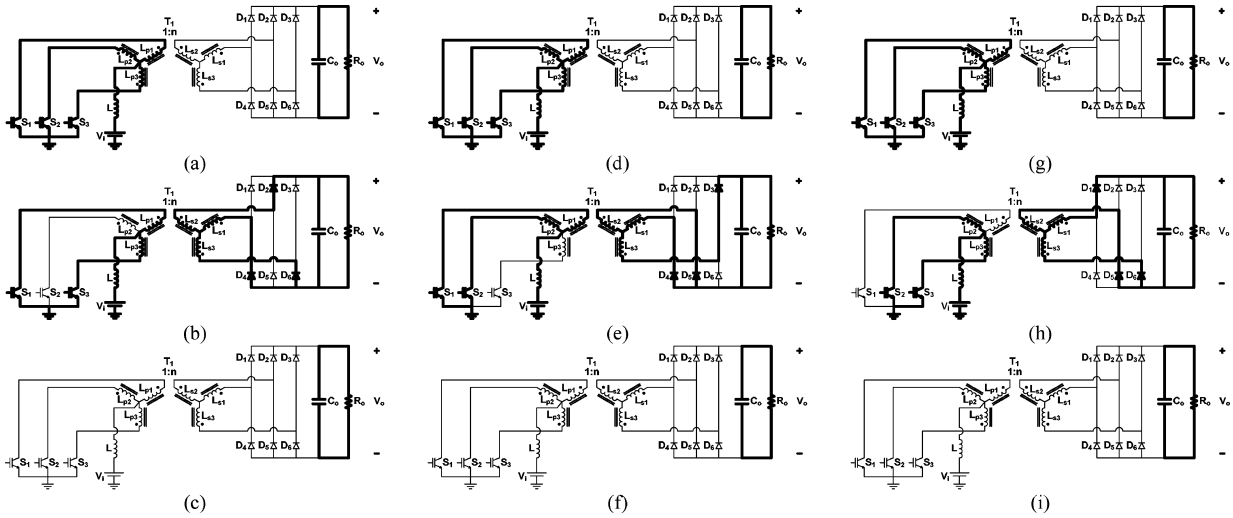

Fig. 8. Topological stages for DCM operation in region R3. (a) First stage (t_0, t_1). (b) Second stage (t_1, t_2). (c) Third stage (t_2, t_3). (d) Fourth stage (t_3, t_4). (e) Fifth stage (t_4, t_5). (f) Sixth stage (t_5, t_6). (g) Seventh stage (t_6, t_7). (h) Eighth stage (t_7, t_8). (i) Ninth stage (t_8, t_9).

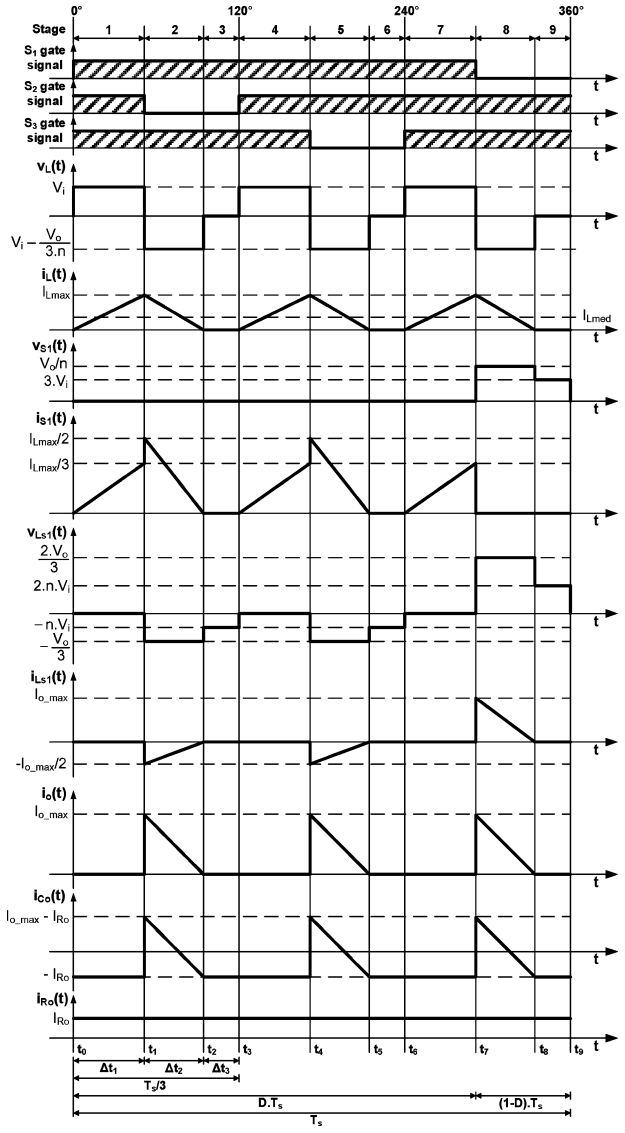

Fig. 9. Main theoretical waveforms for DCM operation in region R3.

TABLE V
EQUATIONS FOR THE CURRENTS AND TIME INTERVALS OF FIG. 9

Currents	Time Intervals
$I_{o\_max} = \frac{I_{Lmax}}{3 \cdot n}$	$\Delta t_1 = \left(D - \frac{2}{3}\right) \cdot T_s$
	$\Delta t_2 = \left[V_i \Big/ \left(\frac{V_o}{3 \cdot n} - V_i\right)\right] \cdot \Delta t_1$
	$\Delta t_3 = \frac{T_s}{3} - \Delta t_1 - \Delta t_2$

TABLE VI
EQUATIONS USED TO PLOT THE OUTPUT CHARACTERISTIC

	Region R2	Region R3
CCM voltage gain	$\frac{q}{n} = \frac{1}{1-D}$	$\frac{q}{n} = \frac{1}{1-D}$
DCM voltage gain	$\frac{q}{n} = 3 \cdot \frac{\overline{I_o} + (3 \cdot D - 1)^2}{2 \cdot \overline{I_o} + (3 \cdot D - 1)^2}$	$\frac{q}{n} = 3 \cdot \left[\frac{(3 \cdot D - 2)^2}{\overline{I_o}} + 1\right]$
Limit between CCM and DCM operation	$\overline{I_{oL}} = \frac{-2 \cdot (q/n)^2 + 9 \cdot (q/n) - 9}{(q/n)^2}$	$\overline{I_{oL}} = \frac{3 \cdot (q/n) - 9}{(q/n)^2}$

characteristic (the voltage gain divided by the turns ratio q/n versus normalized output current $\overline{I_o}$) can be plotted, as shown in Fig. 10.

The horizontal axis in Fig. 10 ($\overline{I_o}$) is normalized as a function of the average output current I_o and circuit parameters, the transformer turns ratio n, the inductance L, the switching frequency f_s, and the input voltage V_i, so that it becomes dimensionless. The general plot of Fig. 10 can be used for different design parameters, since the normalization is known.

Fig. 10 shows the three different regions of operation: R1, R2, and R3. Region R1 is forbidden and regions R2 and R3 have the voltage gain increased by increasing the duty cycle D. For a given design in CCM, with specified n, L, f_s, and V_i, the reduction of the average output current I_o makes the ripple

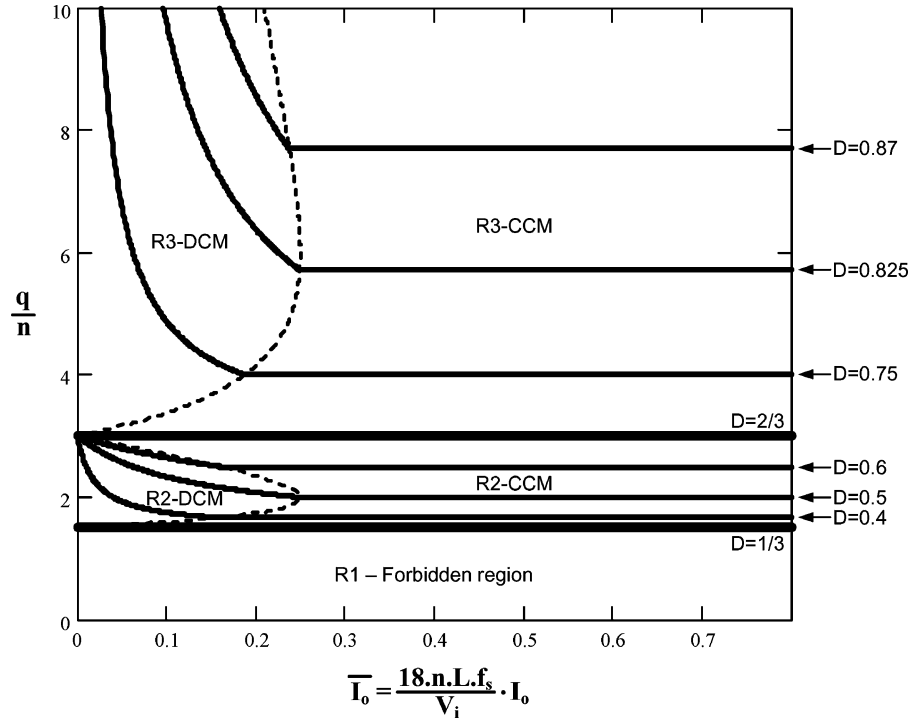

Fig. 10. Output characteristic of the proposed converter.

increase, and the converter point of operation move to the left of the plot in the direction of the DCM.

In addition, Fig. 10 shows an interesting characteristic of the converter: the ripple tends to zero when the duty cycle equals one-third or two-thirds. When the converter operates with these duty cycle values, it does not enter DCM, even for low current values. This result will be discussed again during the section on the experimental results.

IV. Design Example

A. Specifications

After the theoretical analysis, some design specifications were defined with the objective of simulating the converter and implementing a prototype. These specifications are:

$P_o = 1$ kW	output power;
$V_i = 120$ V	input voltage;
$V_o = 400$ V	output voltage;
$f_s = 40$ kHz	switching frequency;
$\eta = 85\%$	expected efficiency;
$\Delta I_L = 0.1 I_L$	input current ripple (10% of the inductor current I_L).

B. Duty Cycle

In this design, the duty cycle was chosen as 0.8 to assure operation in region R3, which was identified as the worst case.

C. Turns Ratio of the Transformer

The turns ratio of the transformer is defined as the number of turns of a secondary winding divided by the number of turns of a primary winding and was determined as

$$n = q\,(1 - D) = \frac{400\ \text{V}}{120\ \text{V}}\,(1 - 0.8) = \frac{2}{3} = 0.667. \quad (9)$$

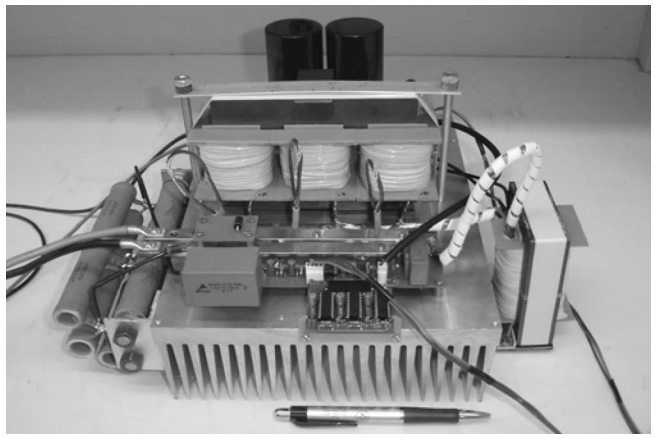

Fig. 11. Picture of the prototype.

D. Boost Inductance

The boost inductance is calculated as determined for operation in region R3

$$L = \frac{V_i}{\Delta I_L f_s}\left(D - \frac{2}{3}\right) = \frac{120\ \text{V}}{0.1\,[1\ \text{kW}/(0.85 \times 120\ \text{V})]\,40\ \text{kHz}} \times \left(0.8 - \frac{2}{3}\right) = 408\ \mu\text{H}. \quad (10)$$

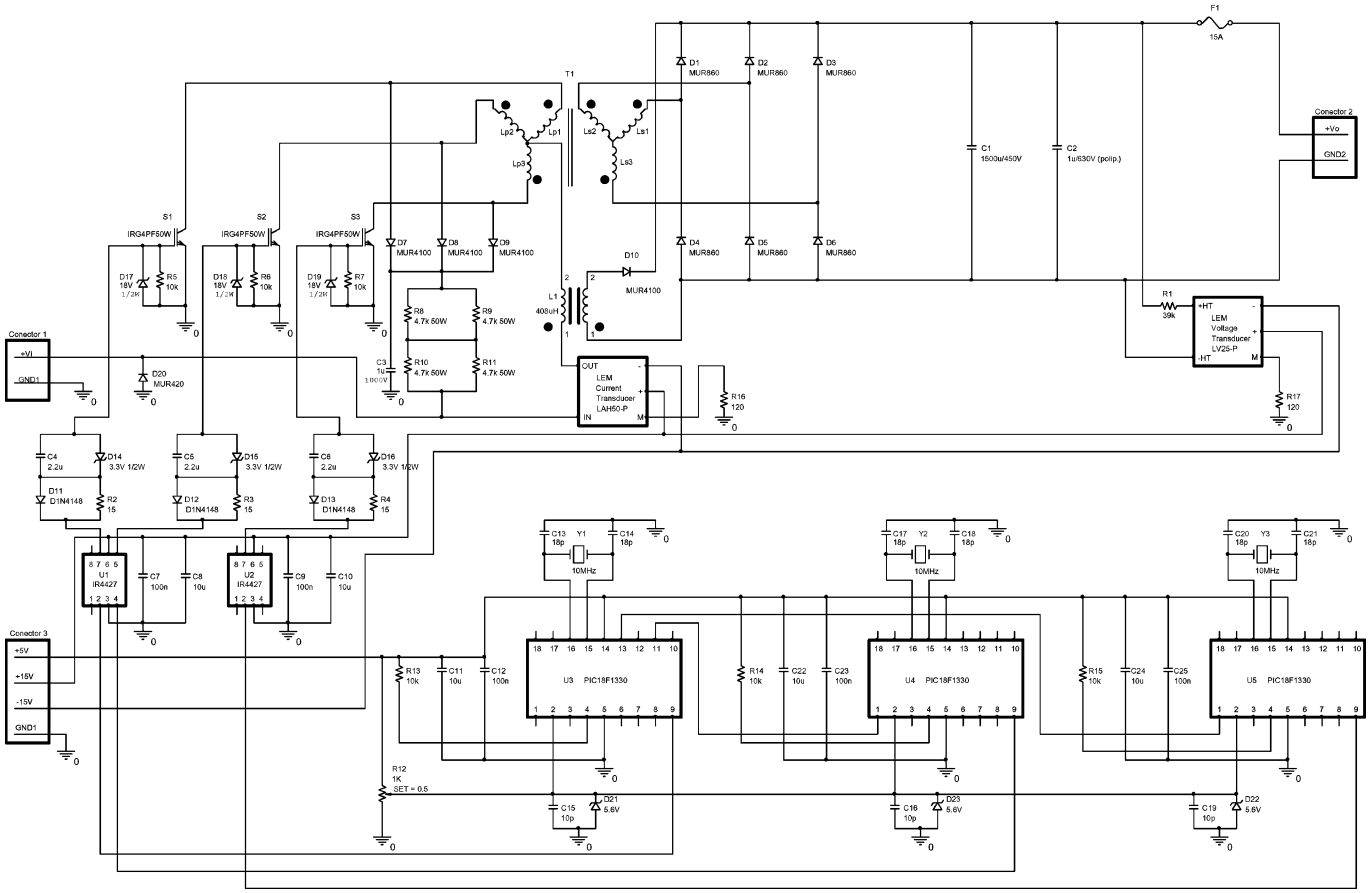

Fig. 12. Schematic of the implemented circuit.

E. RMS Value of the Current Through the Output Capacitor

The rms value of the current through the output capacitor can be calculated for operation in region R3 as

$$I_{Corms} = I_o\sqrt{\frac{2-3D}{3D-3}} = \frac{1\text{ kW}}{400\text{ V}}\sqrt{\frac{2-(3\times 0.8)}{(3\times 0.8)-3}} = 2.04\text{ A}. \tag{11}$$

A 1500-μF/450-V capacitor was used to fulfill the requirements.

V. Prototype Implementation and Experimental Results

A. Prototype Description

A prototype of the proposed three-phase current-fed push–pull dc–dc converter was implemented in order to validate the theoretical analysis. A picture of the prototype can be seen in Fig. 11 and the implemented circuit in Fig. 12.

The main specifications and components of the prototype are shown in Table VII.

The gate drive signals were generated by three PIC18F1330 microcontrollers.

The imperfections in the coupling of the windings and the leakage flux of a real transformer are always associated with a leakage inductance. This inductance stores energy in each cycle of operation and this energy must be dissipated or reused properly, otherwise it can cause overvoltage and failure of the insulated gate bipolar transistors (IGBTs) when they are turned off.

For protecting the IGBTs against overvoltage caused by the transformer leakage inductance, a passive voltage clamp circuit was used. In spite of being needed for protection, this circuit dissipates energy and reduces the efficiency of the converter. The construction of the transformer is important since the lower the leakage inductance is, the less dissipative voltage clamper can be used.

TABLE VII
Main Specifications and Components of the Prototype

Description	Quantity	Values
Output Power (P_o)	-	1 kW
Input Voltage (V_i)	-	120 V
Output Voltage (V_o)	-	400 V
Switching Frequency (f_s)	-	40 kHz
High-Frequency Three-Phase Transformer (T_1)	1	N_s/N_p=12/18
Input Inductor (L)	1	408 µH
Output Capacitor (C_o)	1	1500 µF
IGBTs (S_1, S_2, S_3)	3	IRG4PF50W
Diodes (D_1, D_2, D_3, D_4, D_5, D_6)	6	MUR860
IGBT Drivers	2	IR4427
Microcontrollers	3	PIC18F1330

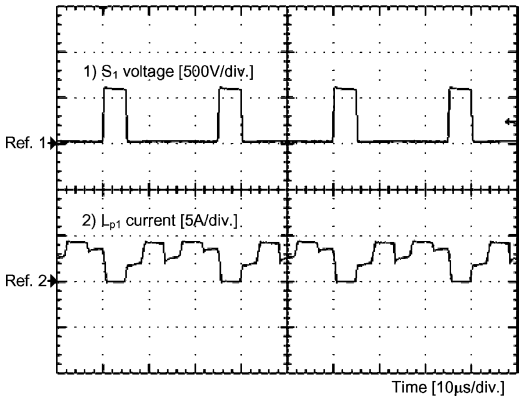

Fig. 13. Voltage across S_1 and current through $L_{\mathrm{p}1}$ for $D = 0.8$.

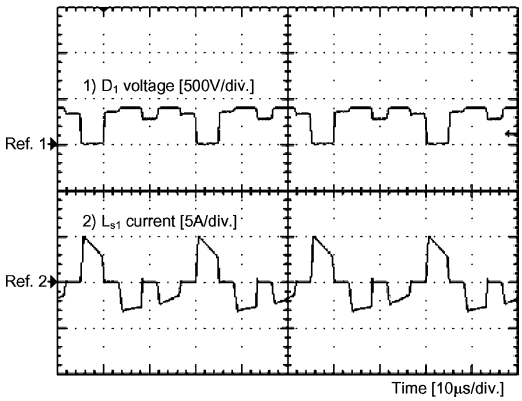

Fig. 14. Voltage across D_1 and current through $L_{\mathrm{s}1}$ for $D = 0.8$.

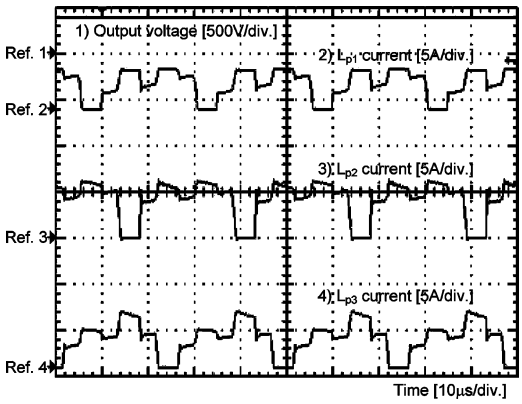

Fig. 15. Output voltage and currents through $L_{\mathrm{p}1}, L_{\mathrm{p}2}$, and $L_{\mathrm{p}3}$ for $D = 0.8$.

B. Experimental Results

First, the waveforms for the rated conditions (R3) specified for the design example are presented. Fig. 13 shows the voltage across switch S_1 and the current through primary winding $L_{\mathrm{p}1}$. The voltage value when S_1 is OFF is equal to the output voltage referred to the primary side, as expected. The waveform of the current is also as expected. The voltage across diode D_1 of the rectifier bridge and the current through secondary winding $L_{\mathrm{s}1}$ can be seen in Fig. 14. Fig. 15 shows the currents of each primary phase (currents through $\mathrm{L}_{\mathrm{p}1}$, $\mathrm{L}_{\mathrm{p}2}$, and $\mathrm{L}_{\mathrm{p}3}$) and the output voltage. The input voltage and input current for the given design conditions are presented in Fig. 16.

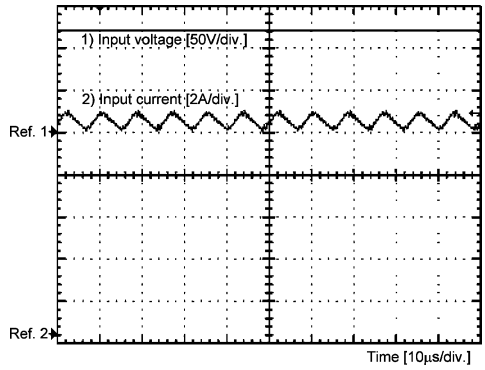

Fig. 16. Input voltage and input current for $D = 0.8$.

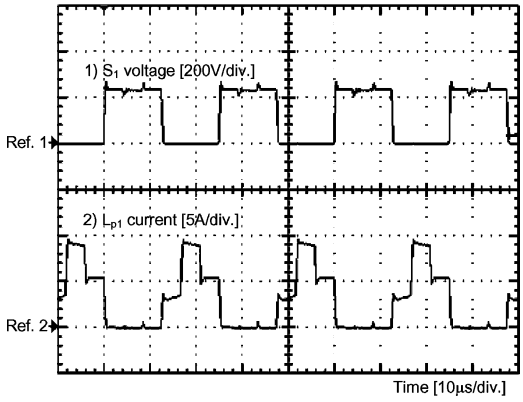

Fig. 17. Voltage across S_1 and current through $L_{\mathrm{p}1}$ for $D = 0.5$.

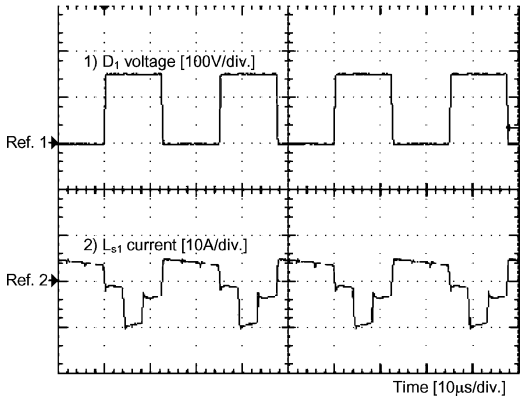

Fig. 18. Voltage across D_1 and current through $L_{\mathrm{s}1}$ for $D = 0.5$.

Two other operating conditions were also verified. Figs. 17–20 show the condition where the input voltage was maintained but the output voltage was reduced by adjusting the duty cycle to 0.5 so that the converter was operated in region R2. These experimental waveforms for R2 are also in accordance with the theoretical analysis.

The last experimental waveform, shown in Fig. 21, illustrates the comment made in the output characteristic section: when using a duty cycle of two-thirds, the input current ripple is zero. The other duty cycle value that results in zero

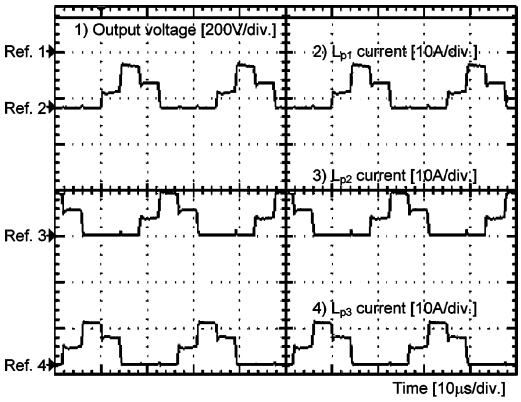

Fig. 19. Output voltage and currents through $L_{\rm p1}$, $L_{\rm p2}$, and $L_{\rm p3}$ for $D = 0.5$.

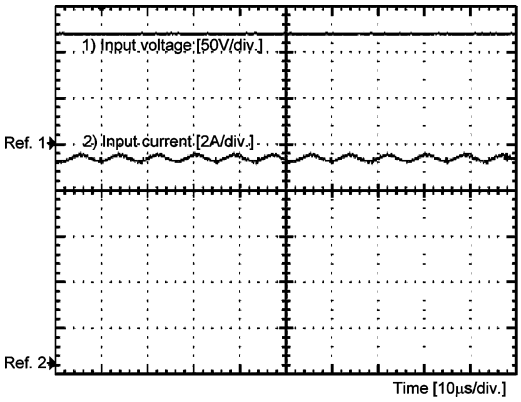

Fig. 20. Input voltage and input current for $D = 0.5$.

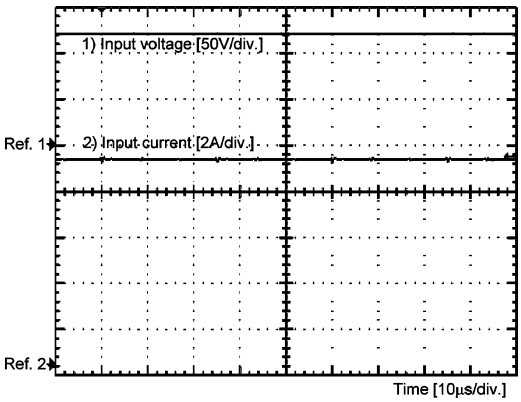

Fig. 21. Input voltage and input current for $D = 2/3$.

input current ripple, $D = 1/3$, was not tested so that operation in the forbidden region would be avoided.

In addition to the waveforms, the converter efficiency was measured for each of the three tested duty cycles in different load conditions. The results of the measurements are presented in Fig. 22. This figure shows that for all tested load conditions, the efficiency is higher for the lower duty cycle. The reduction of the duty cycle also reduces the maximum voltage across the switches, and consequently, the voltage across the resistor of the voltage clamp circuit, which is mainly responsible for the losses. The reduced losses in the voltage clamp circuit increase the overall efficiency of the converter.

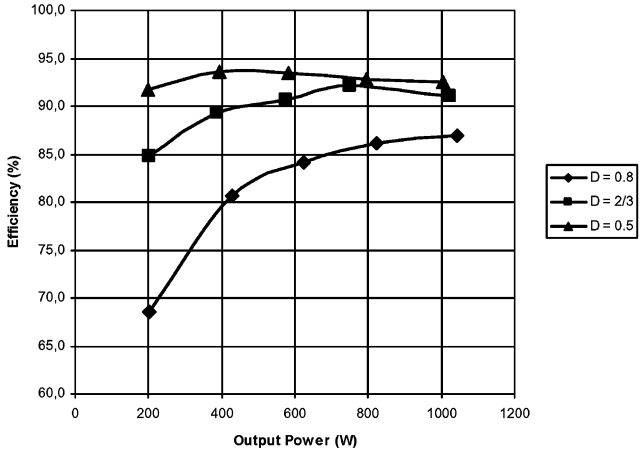

Fig. 22. Converter efficiency as a function of the output power for $D = 0.5$, $D = 2/3$, and $D = 0.8$.

VI. Conclusion

A three-phase current-fed push–pull dc–dc converter was proposed in this paper. Theoretical analysis was presented describing each mode of operation. The output characteristic of the converter, describing all modes of operation, was derived.

A simplified design example was presented where the main parameters of the converter were calculated. These parameters were used in the construction of a 1-kW prototype that presented experimental results in good agreement with the theoretical analysis, thus validating the analysis.

Operating the converter with a duty cycle of two-thirds proved to be interesting since zero input current ripple can be achieved using very low inductance.

The proposed converter is suitable for applications where renewable power sources or batteries are used. By using this converter, the filter size can be reduced and the losses caused by high currents can be more evenly distributed.

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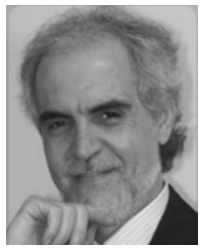

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