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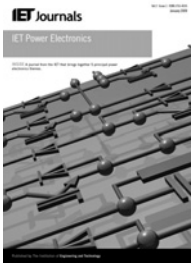

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Three-level zero-voltage switching pulse-width modulation DC–DC boost converter with active clamping

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Abstract: DC–DC step-up converters for high-output voltage applications typically demand high voltage devices, leading to high conduction and switching losses. This identified demand has motivated research on active clamping and multi-level topologies. On this context, this study presents the study of a novel DC–DC boost converter with three-level boost-type active clamping, zero-voltage switching (ZVS) soft-switching and constant frequency pulse-width modulation. As shown analytically and through experimental results, high efficiency and reduced voltage ratings for the power semiconductors are achieved, thus, making the topology suitable for converters requiring high-output DC voltage. Furthermore, a topological modification for achieving ZVS operation in all semiconductors and other types of switching cells for boost-type converters is introduced.

1 Introduction

DC–DC converters for high-voltage applications typically require high voltage-rated devices, which in their turn present more severe parasitic parameters, such as increased capacitances and reverse recovery. From a switching losses point of view, the main factors limiting the operation of traditional hard-switched pulse-width modulation (PWM) converters are the junction capacitances of the power semiconductors, parasitic inductances and diodes reverse recovery. In order to take advantage of their effects, soft-switching techniques have been proposed in the literature. These soft-switching techniques typically increase voltage and current stresses for the semiconductor devices. Zero-current switching (ZCS) techniques [1, 2] generally increase current stresses and zero-voltage switching (ZVS) techniques [3–7] generally increase the blocking voltage stresses [8].

The reduction of blocking voltages can be achieved with three-level non-isolated DC–DC PWM converters operating at constant frequency as shown in [9, 10]. However, these converters present hard-switching. Based on a literature review, important steps have been achieved on the research of more efficient converters employing soft-switching and simultaneously achieving lower blocking voltages. For instance, [11] introduces a buck converter (cf. Fig. 1*a*) employing a multi-resonant converter ZVS technique. As shown in [11] the maximum voltage across the switches equals 130% of the input voltage for 1.1 kW output power, 600 V input voltage and 220 V output voltage, resulting in an efficiency of 92.5%. Under similar operating conditions, the voltage across the switches of the buck converter presented in [12] (cf. Fig. 1*b*) is 120% of the input voltage. This is exactly twice the voltage achieved in [13] for 1 kW, 500 V input and 150 V output voltages, leading to 93% efficiency. Both the topologies shown in Fig. 1*a* [11] and Fig. 1*b* [12] present the same number of turn-off switches for similar values of blocking voltages across them. Even though [12] makes use of a two-level converter, the resulting voltage across the switches is slightly smaller than in the three-level converter analysed in [11]. On the other hand, the three-level buck converter of [11] employs pulse frequency modulation (PFM) and enables ZVS commutation throughout the full load range. The modulation strategies of [12, 13] do not secure ZVS commutation throughout the entire load range. Nevertheless, owing to the fixed carrier frequency, they are simpler to implement than PFM.

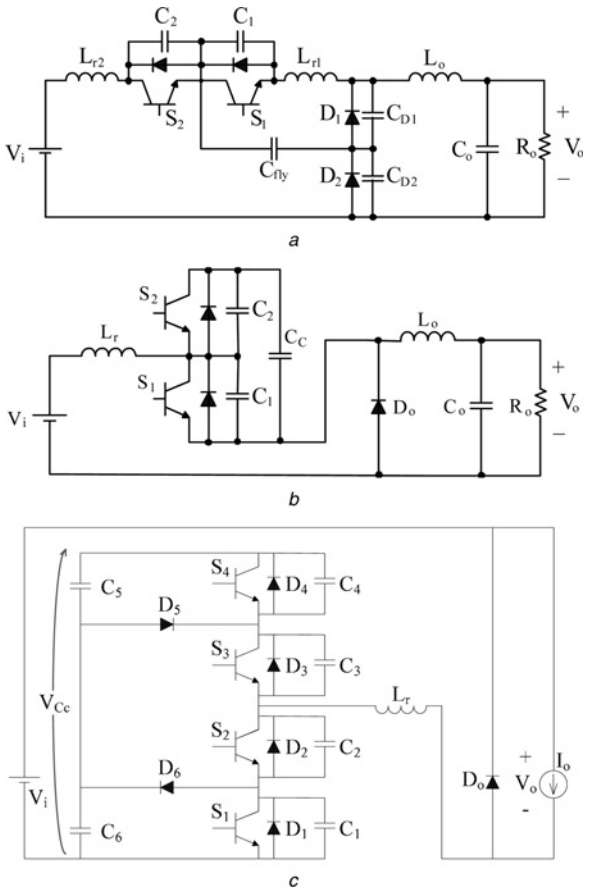

Figure 1 *Comparison of the topologies*

a Three-level ZVS PFM buck converter [11]
b Two-level ZVS PWM buck_boost converter [12]
c Three-level ZVS PWM buck_boost converter [13]

For the buck-type topology with boost-type clamping (buck_boost) shown in Fig. 1*c* [13], the maximum voltage across the switches is exactly half of that of the converter of Fig. 1*b* for the same specifications. Despite all the development achieved in the last years, applications where low electromagnetic emissions, low switching losses and high output voltages are requirements, still have not seen a definitive solution. Thus, it is the objective of this work to contribute in this area by proposing novel active clamping three-level converters and the technical solutions for their proper operation. The converters introduced in this work present similar characteristic to those of the converters analysed in [12], while reducing by half the voltage stresses in the switches by employing clamping techniques, similar to [13].

The main contribution of this paper is the reduction of the maximum voltage across the active switches while preserving commutation of these switches under zero-voltage conditions. Considering the voltage stress in a classical single-switch boost converter equal to 100% of the output voltage and that this switch does not commutate under zero voltage, it is shown that the maximum voltage across the switches in the specifications of this design is equal to 64% in the proposed converter. Switching in the two-level converter of [12] is also done under ZVS, still the voltage stress of these switches is 128% of the output voltage, with the same specifications. A challenge in the proposed topology is the balance on the clamping voltages. Thus, a control scheme to balance these voltages is proposed here.

The three-level ZVS PWM boost-type converter with boost-type active clamping (boost_boost) is here introduced and analysed with respect to its theoretical operation. Experimental results obtained in an evaluation performed in a prototype show good agreement with the proposed models. Furthermore, the proposal of other topologies based on the presented techniques is presented and a topological variation of the proposed converter where all semiconductors switch under ZVS is introduced.

2 Three-level boost_boost converter

In [13] the three-level ZVS PWM boost clamping technique is applied to the buck converter. The boost converter is chosen in the present work because of its capability of stepping-up the output voltage. By applying the boost-type of clamping techniques introduced in [13], the topology of the boost converter with boost clamping is derived (cf. Fig. 2).

For analysing this converter, the following simplifications are assumed:

- the switches are ideal;
- the converter operates in steady-state;
- input inductance L_i is such that, in conjunction with input voltage V_i, it can be assumed as a current source (I_i);
- resonant inductor L_r stores sufficient energy to complete the charging and discharging of the resonant capacitors

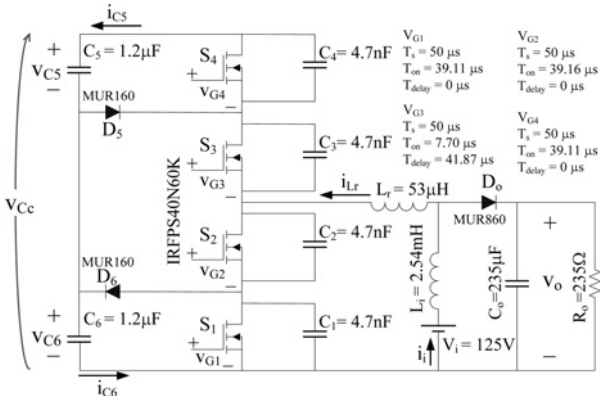

Figure 2 *ZVS three-level boost_boost converter, with the parameters designed in Section 3*

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($C_1 = C_2 = C_3 = C_4 = C_r$) and to properly bias the intrinsic diodes of the switches (D_1, D_2, D_3 and D_4);

- the auxiliary bus capacitance C_C ($C_C \approx (C_5 + C_6)/2$) is much larger than C_r and capacitors C_5 and C_6 are considered as nearly equal to DC voltage sources.

2.1 Basic operation

Depending on the difference of the voltages across capacitors C_5 and C_6, the time intervals between the turn-off of the switches and the charge of the resonant capacitors (C_r), the converter can operate in nine different situations. However, in all of these situations the converter operates with ZVS and maintains its static characteristic. Small differences appear only in a few operation stages and for a very short time. To simplify the analysis of the stages, the voltages across capacitors C_5 and C_6 are considered equal. This assumption can be done since these voltages are to be controlled. A resonant capacitor value C_r is assumed as if it is sufficient for achieving ZVS operation.

The necessary condition for ZVS to occur is that the switch is turned-on after its parallel capacitor is fully discharged. In other words, to achieve zero losses in the switching intervals, the gate-drive signals of switches S_1 and S_2 ($V_{G1,G2}$) should change states in between t_{11} and t_{12} and the drive signals of S_3 and S_4 ($V_{G3,G4}$) should be shifted in between t_6 and t_7. Voltage V_x shown in Fig. 4 is smaller than $V_{Cc}/2$ and depends on the turn-off intervals.

The operation stages are presented next considering the assumptions described here. Fig. 3 is to be referred in order to visualise the corresponding topological states. Fig. 4

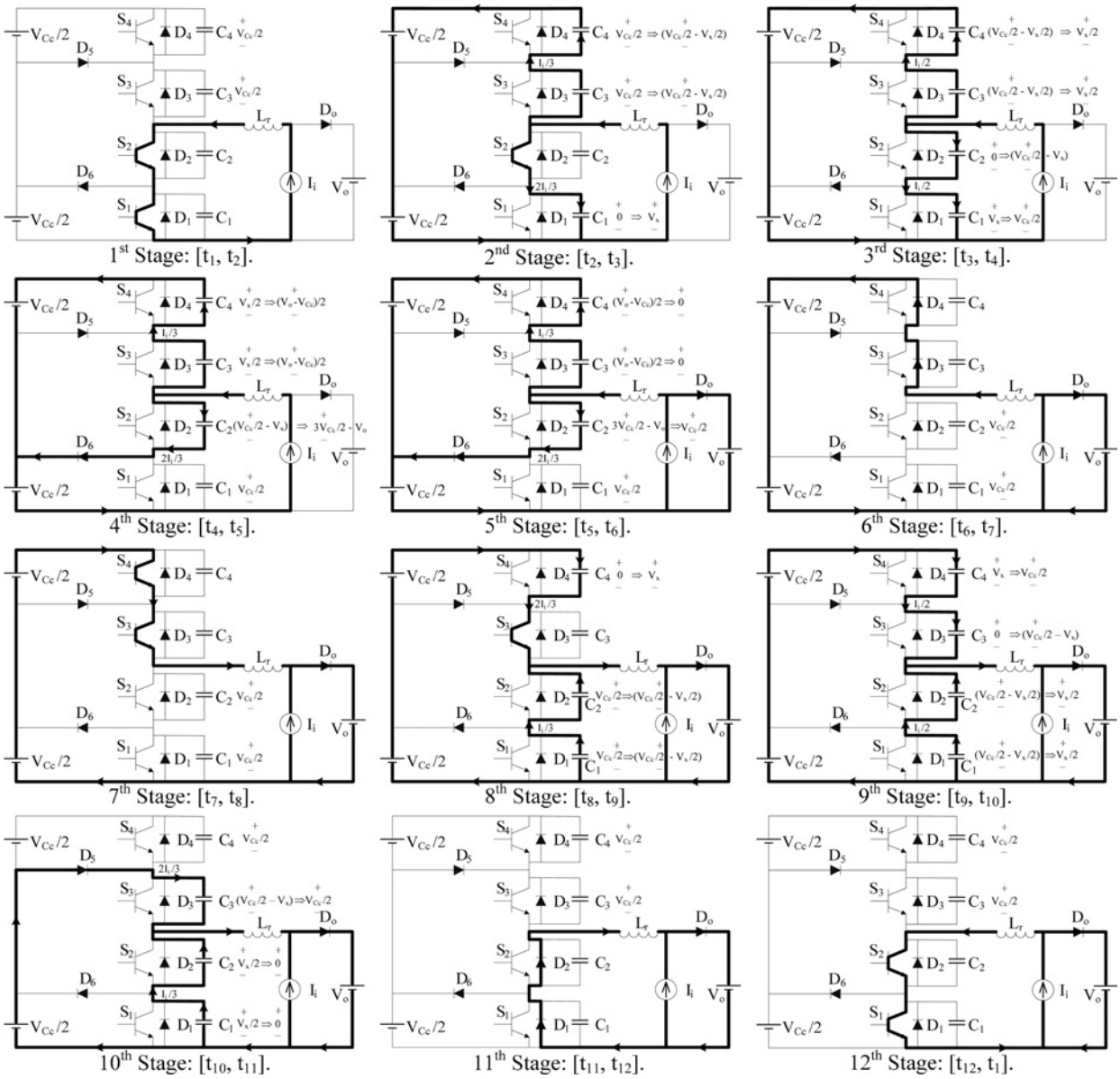

Figure 3 *Operation stages of the three-level ZVS boost_boost converter*

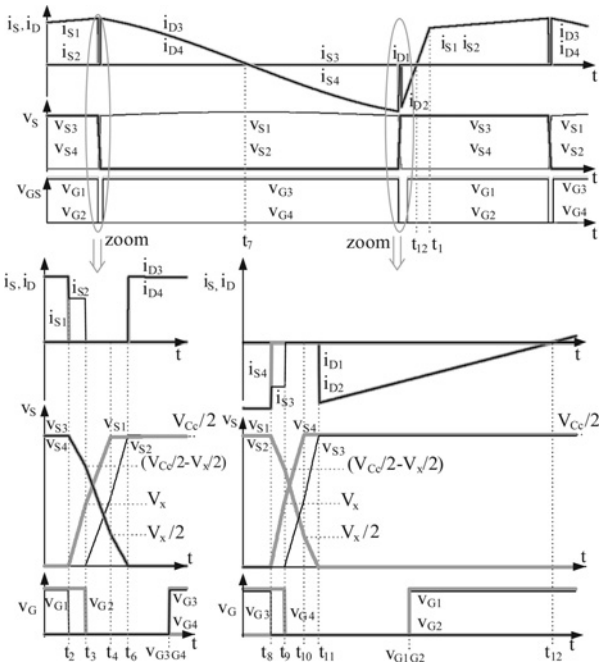

Figure 4 *Details of the waveforms of the three-level boost_boost converter with ZVS commutations*

presents the main waveforms of the converter. Each operation stage is described by employing these figures.

First stage [t_1–t_2]: Switches S_1 and S_2 are on and the current through inductor L_r is positive and equal to I_i since diode D_o is reversely biased.

Second stage [t_2–t_3]: Switch S_1 turns off, while S_2 remains on. The current divides itself among resonant capacitors C_1, C_3 and C_4. In other words, the current through inductor L_r, which is constant and equal to I_i, is split according to $2I_i/3$ flows through C_1 and $I_i/3$ through C_3 and C_4. The voltage across capacitor C_1 increases from zero to V_x and the voltages across C_3 and C_4 decrease from $V_{Cc}/2$ to $(V_{Cc}/2 - V_x/2)$.

Third stage [t_3–t_4]: Switch S_2 is turned off. The current through inductor L_r is evenly divided, so that the current through the resonant capacitors is $I_i/2$. This stage ends when the voltage across capacitor C_1 reaches $V_{Cc}/2$ and the voltages across capacitors C_3 and C_4 reach $V_x/2$. At the end of this stage, diode D_6 is forward biased.

Fourth stage [t_4–t_5]: A similar current distribution as in the second stage occurs. At the end of this stage, diode D_o is forward biased.

Fifth stage [t_5–t_6]: The voltage across inductor L_r remains null. Capacitors C_3 and C_4 are discharged until the voltage across them reaches zero.

Sixth stage [t_6–t_7]: In this stage diodes D_3 and D_4 are forward biased and conduct the current circulating through resonant inductor L_r, which decreases linearly and proportional to $(V_{Cc} - V_o)/L_r$ until zero.

Seventh stage [t_7–t_8]: Switches S_3 and S_4, which had been turned on before instant t_7, conduct. The current through inductor L_r continues to decrease linearly at the same rate as in the previous stage.

Eighth stage [t_8–t_9]: Switch S_3 is still on and switch S_4 is turned off. The current is divided again and one-third of the inductor current discharges capacitors C_1 and C_2 to $(V_{Cc}/2 - V_x/2)$, while the other two-thirds charge capacitor C_4 up to voltage V_x.

Ninth stage [t_9–t_{10}]: Switch S_3 is turned off. The current through the resonant capacitors is $I_i/2$.

Tenth stage [t_{10}–t_{11}]: Diode D_5 is forward biased. Capacitor C_3 is charged to $V_{Cc}/2$ by two-thirds of current I_{Lr}. Capacitors C_1 and C_2 are discharged to zero by half of the resonant inductor current.

Eleventh stage [t_{11}–t_{12}]: Diodes D_1 and D_2 are forward biased and their currents decrease linearly and proportional to V_o/L_r. During this interval, switches S_1 and S_2 are turned on.

Twelfth stage [t_{12}–t_1]: Current I_{Lr} changes direction and circulates through S_1 and S_2, increasing linearly and proportionally to V_o/L_r.

2.2 Static transfer characteristic

In order to compute the static transfer characteristic, the very small time intervals (between t_2 and t_6 and between t_8 and t_{11}) are ignored. These time intervals are rather short and do not appreciably influence the overall characteristic. Therefore Fig. 4 is redrawn employing this simplification as shown in Fig. 5. The duty cycle 'D' is defined as the interval between the turn-off of switches S_3 and S_4 and the turn-off of switches S_1 and S_2. In this way, the drive signals of the switches are not required to be complementary. Considering the performed simplifications,

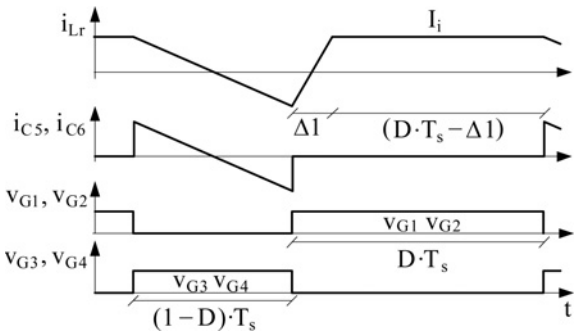

Figure 5 *Simplified waveforms of the three-level boost_boost converter neglecting the short-time variations due to ZVS commutations*

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the static transfer characteristics of the two- and three-level boost_boost converters are strictly the same.

The initial current through capacitors C_5 and C_6, i_{Cc}, is equal to I_i. The current through these capacitors is described as

$$i_{C5}(t) = i_{C6}(t) = i_{Cc}(t) = I_i - \frac{(V_{Cc} - V_o)}{L_r} t \quad (1)$$

For steady-state operation, the average of these current is zero. Integrating (1) yields the voltage across the auxiliary bus (V_{Cc}), as shown in

$$V_{Cc} = \frac{2L_r I_i}{T_s(1-D)} + V_o \quad (2)$$

The following variables are defined for the analysis of the converter

$$\beta = \frac{V_{Cc}}{V_o}$$

$\Rightarrow$ Ratio between the auxiliary bus voltage and the output voltage (3)

$$q = \frac{V_o}{V_i}$$

$\Rightarrow$ Ratio between the output voltage and the input voltage (4)

The normalised inductance L_n is a dimensionless quantity which is a function of the input voltage, output current and switching period. It is defined as

$$L_n = L_r \frac{I_o}{V_i T_s} = L_r \frac{I_i}{V_o T_s} \quad (5)$$

The parameter β is computed by replacing (2) and (5) with (3), so that

$$\beta = \frac{2L_n}{(1-D)} + 1 \quad (6)$$

From (6) the dependency of β on the duty cycle 'D' is obtained as plotted in Fig. 6.

In case of the two-level boost_boost converter, the maximum voltage across switches S_1 and S_2 is equal to bus voltage V_{Cc}. For a three-level converter depicted in Fig. 1*c*, the maximum voltage across the switches is equal to $V_{Cc}/2$. It can be seen in Fig. 6*a* that the auxiliary bus voltage decreases as the normalised resonant inductance (L_n) decreases.

The transfer characteristic can be derived from (7). This expression is valid for the steady-state operation of the converter. The average voltage across inductors L_r and L_i is obviously null. Thus, the following relationship between V_{Cc} and V_i exists

$$V_i = (1-D)V_{Cc} \quad (7)$$

Therefore the static gain is

$$q = \frac{V_o}{V_i} = \frac{V_o}{(1-D)V_{Cc}} \quad (8)$$

Replacing (6) in (8), yields

$$q = \frac{1}{1 - D + 2L_n} \quad \text{or} \quad q = \frac{1}{1 - (D - \Delta 1 f_s)} \quad (9)$$

Fig. 6*b* presents the static transfer characteristic of the boost_boost converter for different values of duty cycle 'D' in dependency of the normalised load current.

2.3 Balance of the clamping DC voltages

Owing to possible asymmetries in the gate signal commands and in the parasitic resistances of the switches and capacitors, the clamping DC voltages V_{C5} and V_{C6} are not guaranteed to be perfectly balanced in a general case. This challenge is typically present in three-level converters and it is also observable here. In order to balance these voltages, different voltage control schemes can be employed. As the total

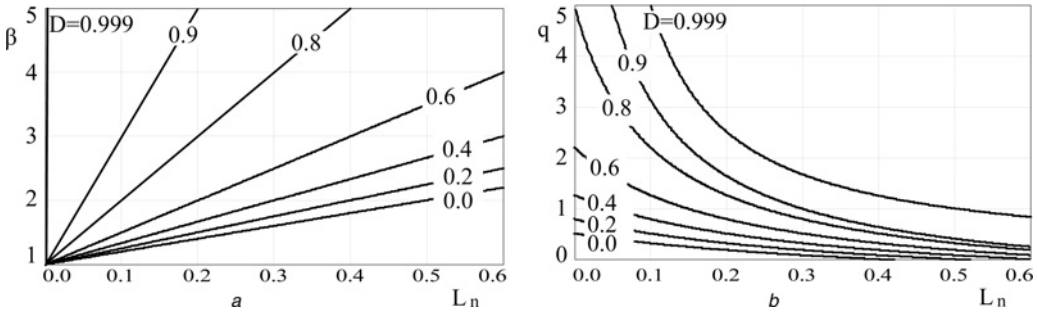

Figure 6 *Behaviour of the main parameters of the converter*

a Normalised auxiliary bus voltage for the boost_boost
b Output to input voltage for the boost_boost

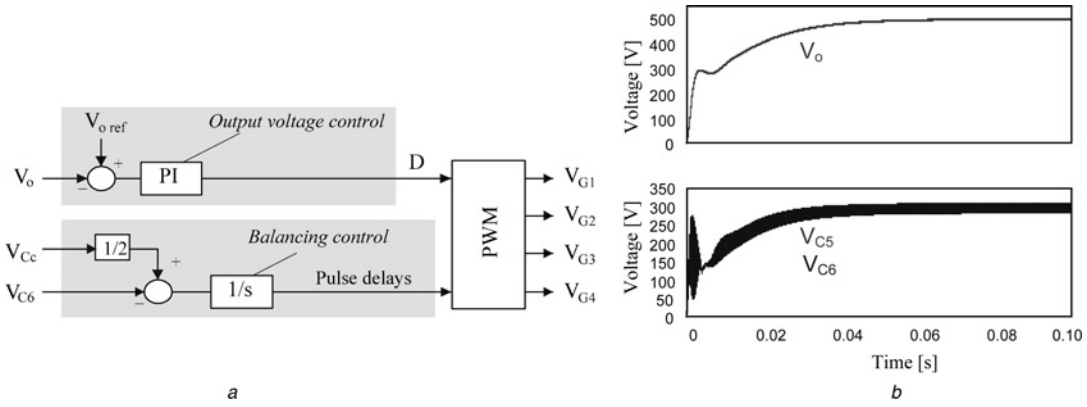

Figure 7 *Control of the clamping DC and the output voltage*

a Proposed control strategy for the boost_boost converter
b Performance of the clamping voltages balancing control loop, where the voltages are set to different levels and the control is capable of balancing in a stable way

clamping voltage $V_{C5} + V_{C6}$ differs from the output voltage, sensing of both voltages V_{C5} and V_{C6} is required.

The complete closed-loop control block diagram of the converter simultaneously regulating the output voltage and the balance of the clamping voltages is shown in Fig. 7*a*. It is seen that the output voltage, total and a partial clamping voltages are sensed in order to provide simultaneous control of the output voltage and balancing of the clamping voltages. Simple resistive dividers can be employed for all these three functions. The output voltage to duty cycle transfer function can, in a first step, be considered to be similar to that of a conventional boost converter as long as the control bandwidth does not include the resonances of the clamping capacitors and the resonant inductor. The balancing control loop is implemented by feeding back the error of the sensed clamping voltages into an integral controller, which acts on the delay times between the turn-off of switches S_1 and S_3 or S_2 and S_4. The control of the output voltage regulation has been implemented with a proportional-integral (PI) controller. This strategy is able to effectively perform both control functions.

This control scheme has been tested in a numerical simulation. The simulated control scheme is shown in Fig. 7*a*, whereas the simulation results are shown in Fig. 7*b*. It is observed that the proposed clamping voltages balancing and output voltage regulation control schemes are able to properly balance the clamping voltages while regulating the output voltage.

3 Converter design

Even though the proposed converter has been envisioned to operate in high-output voltage applications, the specifications for the laboratory prototype have been chosen to demonstrate the operation principles of the novel topology and experimentally validate the performed analysis, while not demanding for high voltage switches. This prototype is based on the following specifications:

- $V_i = 125$ V $\Rightarrow$ input voltage;
- $f_s = 20$ kHz $\Rightarrow$ switching frequency;
- $V_o = 500$ V $\Rightarrow$ output voltage;
- $P_o = 1$ kW $\Rightarrow$ output power;
- $\Delta V_o = 1\% \Rightarrow$ output voltage ripple;
- $\Delta I_i = 25\% \Rightarrow$ input current ripple;
- $\Delta V_{Cc} = 10\% \Rightarrow$ bus voltage ripple;
- $t_{2\_3} = 0.01\%/f_s \Rightarrow$ difference in the turn-off times between switches S_1–S_2 and S_3–S_4.

The values of the input current and the output resistance are computed with

$$I_i = \frac{P_o}{V_i} = 8 \quad \text{and} \quad R_o = \frac{V_o^2}{P_o} = 250\,\Omega \tag{10}$$

The duty cycle is calculated by isolating D in (9). Thus

$$D = 1 + 2L_n - \frac{V_i}{V_o} \Rightarrow D = 0.783 \tag{11}$$

In order to achieve ZVS operation, capacitor C_r should fulfil the condition

$$C_{r\_limite} = \frac{4(1-D)I_i t_{2\_3} V_o^2}{3V_i} = 0.94\,\text{nF}$$
$$\Rightarrow C_r = 4.7\,\text{nF} \tag{12}$$

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The larger the L_r is, the larger the ZVS operation range. However, the voltage across the switches will also be larger. To determine the resonant inductance, a minimum power limit for ZVS operation of 62% of the rated power (P_o) is defined, leading to

$$L_r = \frac{V_o}{(0.62P_o/V_i)f_s} \times \frac{1.1t_{2\_3} + 1.1C_rV_o/I_i - 4.4t_{2\_3}/3}{1/f_s - 2.2C_rV_o/(1-D)(0.62P_o/V_i)} = 53\,\mu\text{H} \quad (13)$$

$$L_r = 53\,\mu\text{H} \Rightarrow L_n = 0.017 \quad (14)$$

The value of the output capacitor is computed in the same manner as for a traditional boost converter. Thus

$$C_o = \frac{DV_o}{f_s\Delta V_o V_o R_o} \Rightarrow C_o = 156\,\mu\text{F} \quad (15)$$

Owing to the required current ratings, the capacitors have been chosen to be $C_o = 235\ \mu\text{F}$.

The input inductance can be chosen from the allowable input current ripple, which occurs during interval t_{6_1}

$$L_i = \frac{(V_o - V_i)}{\Delta I_i}\left[\frac{(1-D)}{f_s} + \frac{2I_iL_r}{V_o}\right] \Rightarrow L_i = 2.31\,\text{mH} \quad (16)$$

Integrating the current expressions for capacitors C_5 and C_6 and using the voltage ripple specifications for these capacitors (ΔV_{Cc}), capacitors C_5 and C_6 are calculated as

$$C_5 = C_6 = \frac{I_i(1-D)}{\Delta V_{Cc}f_s} - \frac{(V_{Cc} - V_o)(1-D)^2}{4\Delta V_{Cc}L_rf_s^2} \quad (17)$$

$$C_5 = C_6 = 0.8\,\mu\text{F} \Rightarrow C_5 = C_6 = 1.2\,\mu\text{F} \quad (18)$$

From (7) the auxiliary bus voltage is

$$V_{Cc} = \frac{V_i}{(1-D)} \Rightarrow V_{Cc} = 576.7\ \text{V} \quad (19)$$

4 Experimental results

A prototype with the parameters given in the previous section has been built according to the circuit schematics depicted in Fig. 2. In order to validate the performed steady-state analysis, the prototype is operated in open loop. The adjustments in the gate drivers delay times have been manually performed in order to balance the clamping DC voltages for a single-load operation point. This has proved sufficient for the balancing of the voltages as no additional control circuitry has been necessary to balance them; these voltages have remained balanced for a wide input voltage range variation (from zero to the rated voltage, V_i). The gate drive signals have been generated by Microchip's PIC18F4331 microcontroller and isolated with Semikron's SKHI10op drivers.

Experimental results of the three-level boost_boost converter (cf. Fig. 2) are presented in Fig. 8. The resonant inductor is subject to high voltage variations and as a result the shape of the L_r current shown in Fig. 8*a* presents a high ripple. The hard switching behaviour of the turn-off of the output diode causes voltage oscillations across L_r and

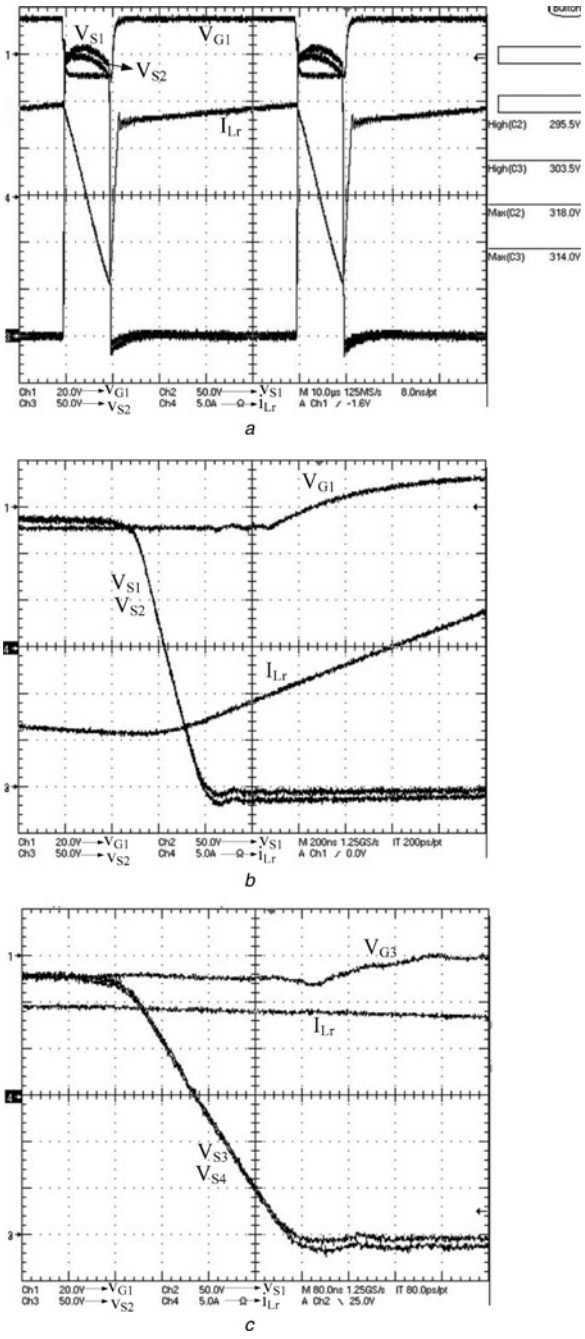

Figure 8 *Voltage across switches S_1 and S_2, drive signal for S_1, and current through the resonant inductor*

a Shown in two periods
b During S_1 and S_2 turn-off
c During S_3 and S_4 turn-on

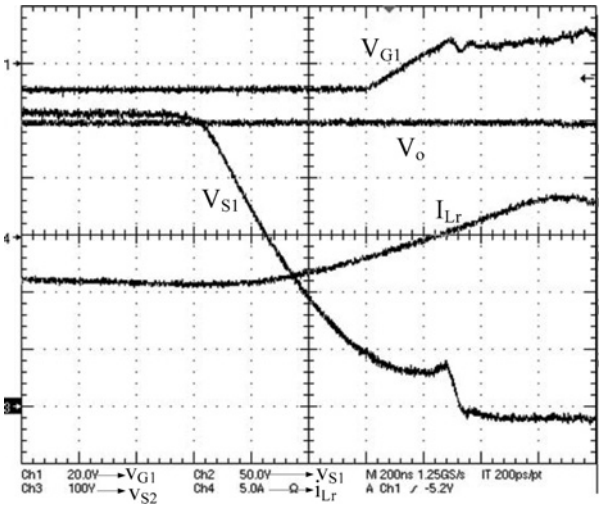

Figure 9 *Voltage across switches S_1 and S_2 for $P = 0.37P_o$*

it is reflected in the oscillations in the current I_{Lr}. The input inductor L_i must present a high value in order to reduce the current ripple.

The maximum peak voltage across the switches equal to 64% of the output voltage, which was measured to be 496 V, is presented in Fig. 8. The measured voltage agrees with the performed analysis, showing that the objective of reduction of the switched voltages is achieved in the proposed structure. Load and input voltage variations were also tested on this circuit. The measured efficiency for 100, 68 and 37% of the load were, respectively, 95.7, 96.6 and 97.4, not including the power losses of the drivers, which is measured to reduce the efficiency by 0.7%.

Fig. 8 shows the detail of the turn-off transition of the switches. During testing it has been observed that the transistors turned on and off under zero-voltage conditions (ZVS) for high output load current. For loads lower than 70% of the rated load, the resonant capacitors are not completely discharged when the switches are turned off, resulting in a commutation which is not ZVS. However, in these cases the turn-off losses are compensated for by lower conduction losses in the components of the circuit. Fig. 9 shows the hard-switching behaviour of switches S_1 and S_2 for a 37% load. It is observed that, even under low-load conditions, the turn-on of the switches is ZVS. In addition, the portion of turn-off that occurs under non-zero-voltage conditions presents a voltage that is much lower than in the case of conventional hard switching (cf. Fig. 9). Thus, low commutation losses are observed for a large load range. This proves the condition of soft-switching as indicated in the converter's theoretical analysis.

If the capacitance of the resonant capacitors were reduced, the ZVS operation range would increase. However, since shorter delay times would be required, it would be more challenging to fine tune the balance of the voltages across C_5 and C_6. This is because of the limited time delays

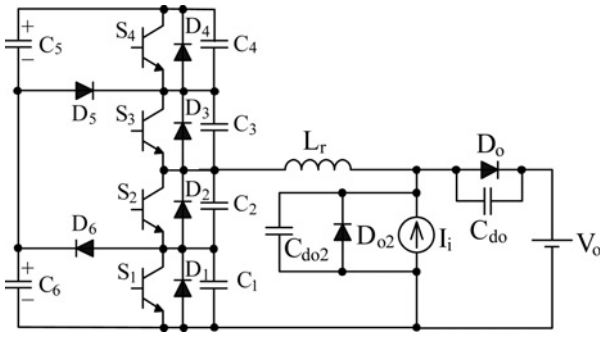

Figure 10 *Boost_boost converter with ZVS in the output diodes*

available when the input voltage increases. Another critical condition is the definition of the PWM pulses in a digital modulator, which might prove challenging for short ZVS commutation times.

5 ZVS of the output diode

In the boost_boost converter presented in the previous section, diode D_o does not commutate under zero-voltage conditions during turn-off. It only commutates under zero-voltage conditions during turn-on. If ZVS is desired in output diode D_o and the four switches (S_1, S_2, S_3 and S_4), diode D_{o2} is added to the circuit, as shown in Fig. 10. In this configuration all semiconductor devices commutate under ZVS. Furthermore, the static transfer characteristic and main waveforms are unaltered.

Considering that the capacitance values of the capacitors in parallel with diodes D_o and D_{o2} are very small or equal to the parasitic capacitances [14, 15], the current through inductor L_r will be slightly larger than in the case of the boost_boost converter presented previously. Ignoring this small increase in current I_{Lr} compared to I_i, the waveforms are similar to those presented in Fig. 4, where the main differences are restricted within the short-time commutation details of the switching of diodes D_o and D_{o2}. Furthermore, the high-frequency oscillations presented in the current across the resonant inductor can be alleviated with the soft turn-off of the output diode.

6 Conclusions

The boost topologies with ZVS have the advantage of reducing switching losses when compared to a conventional boost converter. Therefore these topologies are able to achieve higher efficiency at higher switching frequencies. It has been observed that the two- and three-level ZVS boost_boost converters present similar static characteristics as the conventional boost converter as the resonant inductance is reduced.

The main disadvantage of this topology compared to the two-level conventional boost converter is the increased

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number of components due to the commutation and three-level circuits. This increases its cost and restrains the applications where the proposed converter shows more advantages. Another feature for this type of converter is the balancing of the clamping voltages, which has been addressed in this work and can be performed at the expenses of an additional voltage sensor and control circuitry. On the other hand, the three-level topology proposed here operates with lower voltages across the transistors, enabling this topology to be employed in high-voltage applications.

Comparing the proposed topology to the two-level ZVS boost_boost converter of [12], it has been shown that the blocking voltages are cut in half for the proposed topology. However, the three-level converter presents two bidirectional current switches and an additional capacitor for the auxiliary bus when compared to the two-level converter. The clamping voltage is split into two DC voltages and is inherently stable. It is possible to operate with stable non-balanced voltages, depending on the gate drives timing, operating in open loop. This adjustment can be done manually or with the proposed balancing control.

The three-level technique presents more gate driver circuits as another disadvantage to two-level topologies. In a closed-loop application, the control of the two clamping voltages needs to be implemented and, thus, requires more circuit complexity. Thus, the proposed converter is thought as a suitable solution in applications where the switch technology poses limitation to the available voltage ratings, no insulation is required and high efficiency at high switching frequencies are demanded. Different boost PWM converters have been proposed based on three-level active clamping cells generated with the basic DC–DC converters. These converters present different characteristics and the boost_boost converter has been identified as potentially more advantageous for high-output voltage applications.

The two-level isolated converters with ZVS were further published by many authors [16–21]. Classical ZVS full- and half-bridge topologies present an output rectifier stage which prevents the use of the proposed clamping circuits. Nevertheless, several clamping topologies presented in the last section have been successfully employed in isolated flyback and forward converters [21]. The forward_boost three-level design found in [21] can be expanded to five-level using forward_boost [22].

7 References

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