

Three-Phase Cascaded Multilevel Inverter Using Power Cells With Two Inverter Legs in Series

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Abstract—In this paper, a modular three-phase multilevel inverter specially suited for electrical drive applications is proposed. Unlike the cascaded H-bridge inverter, this topology is based on power cells connected in cascade using two inverter legs in series. A detailed analysis of the structure and the development of design equations for the load voltage with n levels are carried out using pulsewidth-modulation phase-shifted multicarrier modulation. Simulations and experimental results for a 15-kW three-phase system, with nine voltage levels, validate the study presented.

Index Terms—Cascade systems, inverters, multilevel systems, pulsewidth modulation (PWM).

NOMENCLATURE

n_L	Number of voltage levels from line-to-line output voltage.
n_P	Number of voltage levels from phase-to-neutral voltage.
$v_{AB}(t)$	Instantaneous line-to-line output voltage.
$v_{AN}(t)$	Instantaneous phase-to-neutral voltage.
N_c	Number of power cells per phase.
V_{dc}	Isolated dc voltage source.
$v_n(t)$	Instantaneous voltage in the upper switch of the n th inverter leg, disconsidering the harmonics.
$v'_n(t)$	Instantaneous voltage in the lower switch of the n th inverter leg, disconsidering the harmonics.
$v_C(t)$	Instantaneous voltage in the power cell terminal.
$d(t)$	Instantaneous duty cycle.
M	Index of modulation.
θ_o	Phase-shifted sinusoidal modulator.
ω_o	Angular frequency modulator.
f_o	Frequency modulator.
θ_c	Phase-shifted triangular carrier.
ω_o	Angular frequency triangular carrier.
f_c	Frequency triangular carrier.
m_f	Frequency modulation index.

v_{cr}	Triangular carrier waveform.
J_n	Bessel function.
R_o	Resistive load.
L_o	Inductive load.

I. INTRODUCTION

MULTILEVEL inverters [1], [2] have been attracting wide industrial interest. They are considered an attractive alternative in order to reduce switch stress. The main characteristic of these converters is an output waveform with multiple voltage levels.

In recent decades, an extensive array of multilevel structures has appeared [3]–[11], for instance, the cascaded H-bridge (CHB) [12], neutral point clamped [13], and flying capacitor [14].

The CHB multilevel inverter is a popular topology and has found widespread applications in industry, for instance, in high-power medium-voltage drives [15]–[17] and reactive power compensation [18]. It is composed of multiple units of single-phase H-bridge power cells, using two inverter legs in parallel powered by isolated dc supplies. The inverter dc bus voltage is usually fixed, while its ac output voltage can be adjusted by different modulation schemes [12]. The dc supplies are normally obtained by multipulse diode rectifiers to achieve low line-current harmonic distortion and high input power factor.

The H-bridge cells are usually connected in cascade on their ac side to achieve medium-voltage operation and low harmonic distortion. In practice, the number of power cells in a CHB inverter is mainly determined by its operating voltage and manufacturing cost. The use of identical power cells leads to a modular structure, which is an effective means for cost reduction.

Cascaded multilevel inverters have been developed to use unequal dc bus voltages [19] or a single dc source [20], showing the possibility of different implementations for this topology.

An alternative three-phase cascaded multilevel inverter topology is proposed in this paper. It uses power cells connected in cascade using two inverter legs in series, instead of two parallel inverter legs, as conventionally found in CHB power cells. The analysis of the load voltage, for forecasting the resulting harmonic spectrum, is also presented. Finally, a 15-kW prototype with nine voltage levels will be implemented to analyze the theoretical studies carried out.

II. PROPOSED TOPOLOGY

The proposed three-phase multilevel inverter is shown in Fig. 1. This inverter is composed of $(3n_L - 3)$ switches and

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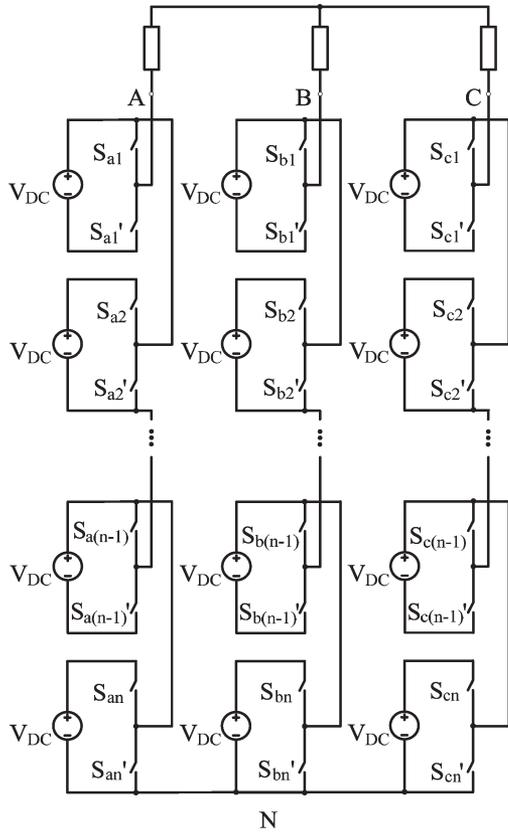


Fig. 1. Multilevel inverter proposed.

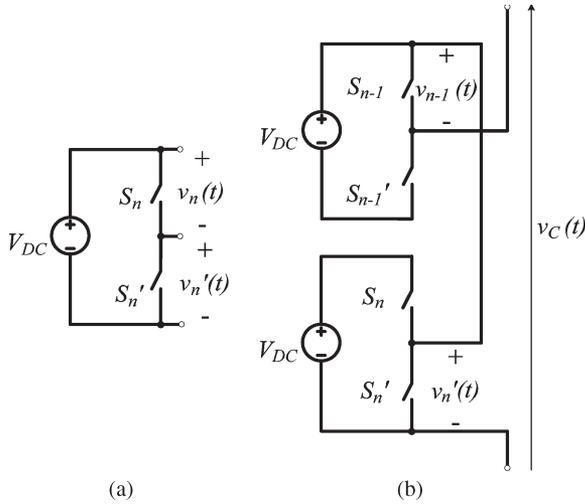


Fig. 2. (a) Inverter leg connected to the isolated dc voltage source. (b) Power cell using two inverter legs in series.

$(3n_L - 3)/2$ isolated dc voltage sources, where n_L is the number of voltage levels of the line-to-line output voltage. The load can be connected in delta or wye.

A basic inverter leg with two switches, working in a complementary way, is shown in Fig. 2(a). Each power cell is composed of two inverter legs with the connections defined in Fig. 2(b).

Voltage $v_C(t)$ in Fig. 2(b) is composed of three voltage levels: V_{dc} , 0, and $-V_{dc}$. When switches S_{n-1} and S_n conduct, the output voltage in the power cell is $v_C(t) = V_{dc}$. Similarly,

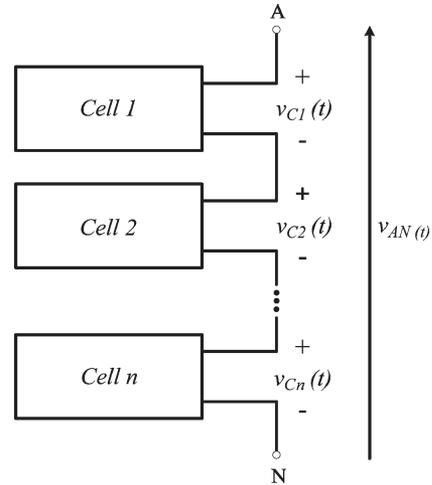


Fig. 3. Per-phase diagram of power cells in cascade.

with S'_{n-1} and S'_n switched on, $v_C(t) = -V_{dc}$. To obtain the level zero, the switches S_{n-1} and S'_n or S'_{n-1} and S_n should be switched on. Thus, by connecting the power cells in cascade (Fig. 3), with a certain phase shift in the switch command between two power cells in the same phase, the number of voltage levels from phase-to-neutral voltage (n_P) can arbitrarily increase.

The maximum numbers of voltage levels of the line-to-line output voltage $v_{AB}(t)$ and phase-to-neutral voltage $v_{AN}(t)$ are respectively represented by

$$n_L = 4N_c + 1 \tag{1}$$

$$n_P = 2N_c + 1 \tag{2}$$

where N_c is the number of power cells per phase. By construction, the number of voltage levels for this topology is always odd.

To understand how each inverter leg should be connected, a detailed analysis of the output voltage of the inverter leg is necessary.

Based on Fig. 2(b), $v'_n(t)$ and $v_{n-1}(t)$ can be defined according to

$$v'_n(t) = \frac{V_{dc}}{2} + \frac{V_{dc}}{2} M \cos(\omega_o t + \theta_o) \tag{3}$$

$$v_{n-1}(t) = \frac{V_{dc}}{2} - \frac{V_{dc}}{2} M \cos(\omega_o t + \theta_o) \tag{4}$$

disregarding harmonics generated by triangular carriers.

The resulting output voltage of each inverter leg can be deduced using (3) and (4). The presence of an average dc voltage ($V_{dc}/2$) is evident. Thus, the phase-to-neutral voltage (v_{AN}) in this inverter will also present an average dc value. Although the line-to-line output voltage does not present this average component, it should be eliminated, aiming at decreasing the peak voltage of v_{AN} . Therefore, when the inverter legs are connected as suggested in Fig. 2(b), the average voltage $V_{dc}/2$ in the phase-to-neutral voltage (v_{AN}) is cancelled.

The instantaneous voltage $v_C(t)$ of the power cell is defined as

$$v_C(t) = v'_n(t) - v_{n-1}(t) \quad (5)$$

$$v_C(t) = V_{dc}M \cos(\omega_o t + \theta_o). \quad (6)$$

The resulting phase-to-neutral voltage $v_{AN}(t)$ (Fig. 3) with N_c power cells can be obtained through

$$v_{AN}(t) = \sum_{n=1}^{N_c} v_{Cn}(t) \quad (7)$$

$$v_{AN}(t) = N_c V_{dc} M \cos(\omega_o t + \theta_o). \quad (8)$$

By using $v_{AN}(t)$ as a reference, the line-to-line output voltage for N_c power cells can be represented by

$$v_{AB}(t) = N_c \sqrt{3} V_{dc} M \cos\left(\omega_o t + \frac{\pi}{6}\right). \quad (9)$$

It should be noticed that, according to (8), the phase-to-neutral voltage $v_{AN}(t)$ has no average dc voltage.

III. MODULATION STRATEGY

As shown in Fig. 4, a pulsewidth-modulation (PWM) phase-shifted multicarrier modulation technique was used. All the triangular carriers have the same frequency and the same peak-to-peak amplitude and phase shift between two adjacent carrier waves to increase harmonic cancellation. A phase shift defined by

$$\frac{(k-1)\pi}{N_c}, \quad k = 1, 2, \dots, 2N_c \quad (10)$$

optimizes the harmonic cancellation according to the study in [21]. For an inverter with two power cells in cascade, it is necessary to employ four triangular carriers with phase shifts of $0, \pi/2, \pi,$ and $3\pi/2$.

Only the upper switch-gate signals for one phase are shown in Fig. 4, because the lower switch-gate signals are complementary. The other two phases are shifted by $\pm 120^\circ$.

To obtain the switch-gate signals, a comparison between the triangular carriers and the modulator is carried out as shown in Fig. 4. The resultant signal will be high when the instantaneous value of the sinusoidal wave exceeds the triangular carrier; otherwise, it will be low. The duration of each pulsewidth in the output comparator depends, therefore, on the time that the sine wave remains above the value of the triangular wave. These high-frequency pulses are sent to the switches of the circuit in Fig. 1, with four inverter legs in cascade.

The carrier waveforms employed in this modulation technique are usually triangular or sawtooth. In this paper, the triangular unipolar format was used because it reduces the harmonic content when compared with the sawtooth carrier [21].

Triangular carriers have, in general, a fixed scale, so the fundamental magnitude control of the output voltage is achieved by varying the sinusoidal modulator amplitude. This alters the pulsewidths, changing the output voltage amplitude.

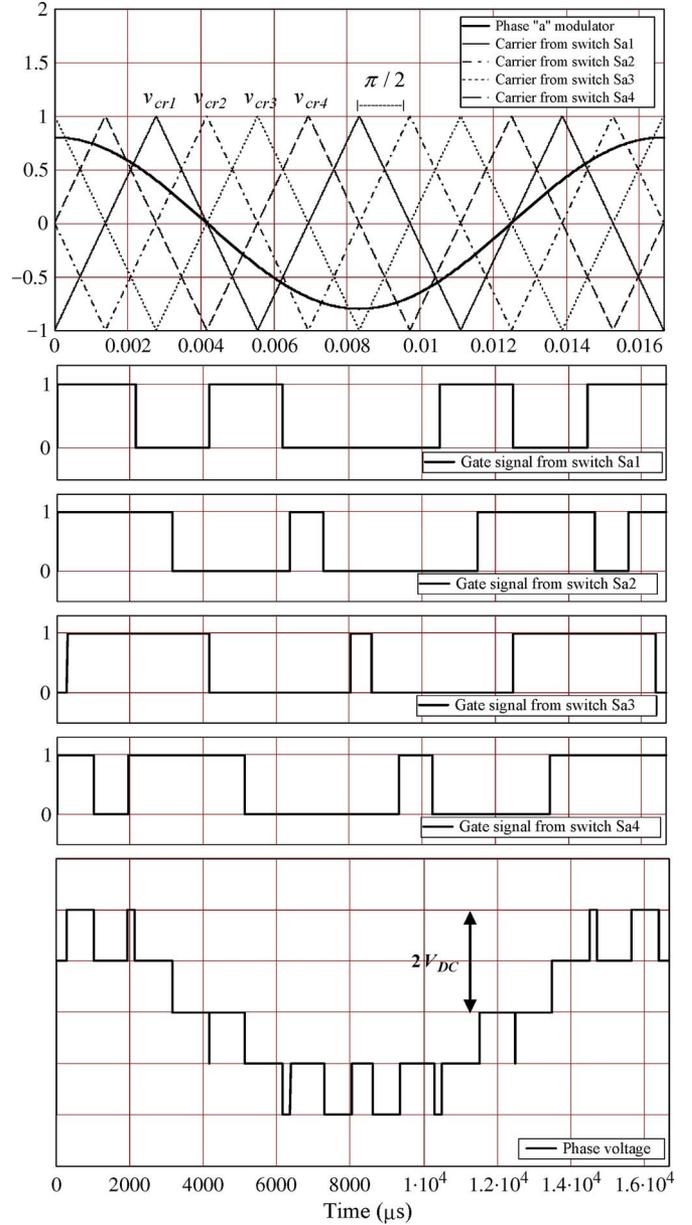


Fig. 4. Simulated waveform of the proposed multilevel inverter ($f_o = 60$ Hz, $f_c = 180$ Hz, $M = 0.8$, and $N_c = 2$).

In Fig. 5, the modulation schematic for one phase is presented. All comparators share the same modulator waveform, and each unipolar triangular carrier has a shift determined by (10).

The phase-shift modulation described here is similar to the one used in CHB multilevel inverters [21], [22]. A CHB multilevel inverter with n_P voltage levels requires $(n_P - 1)$ triangular carriers. In the phase-shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, with a phase shift between any two adjacent carrier waves also defined by (10). However, the phase shift between two parallel inverter legs of each power cell must be 180° .

Once the modulation strategy is defined in order to obtain analytical expressions for the instantaneous phase-to-neutral voltage $v_{AN}(t)$ and the instantaneous line-to-line output voltage

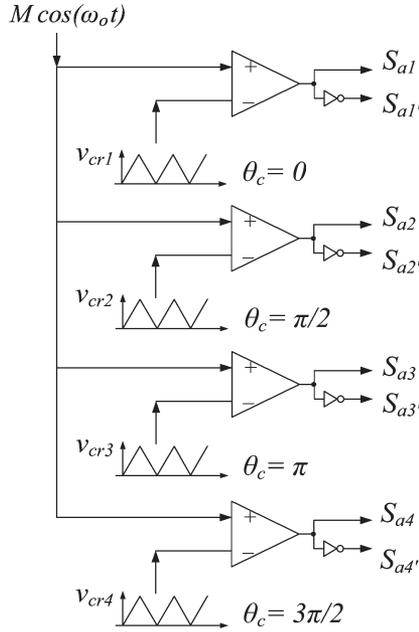


Fig. 5. Simplified modulation schematic.

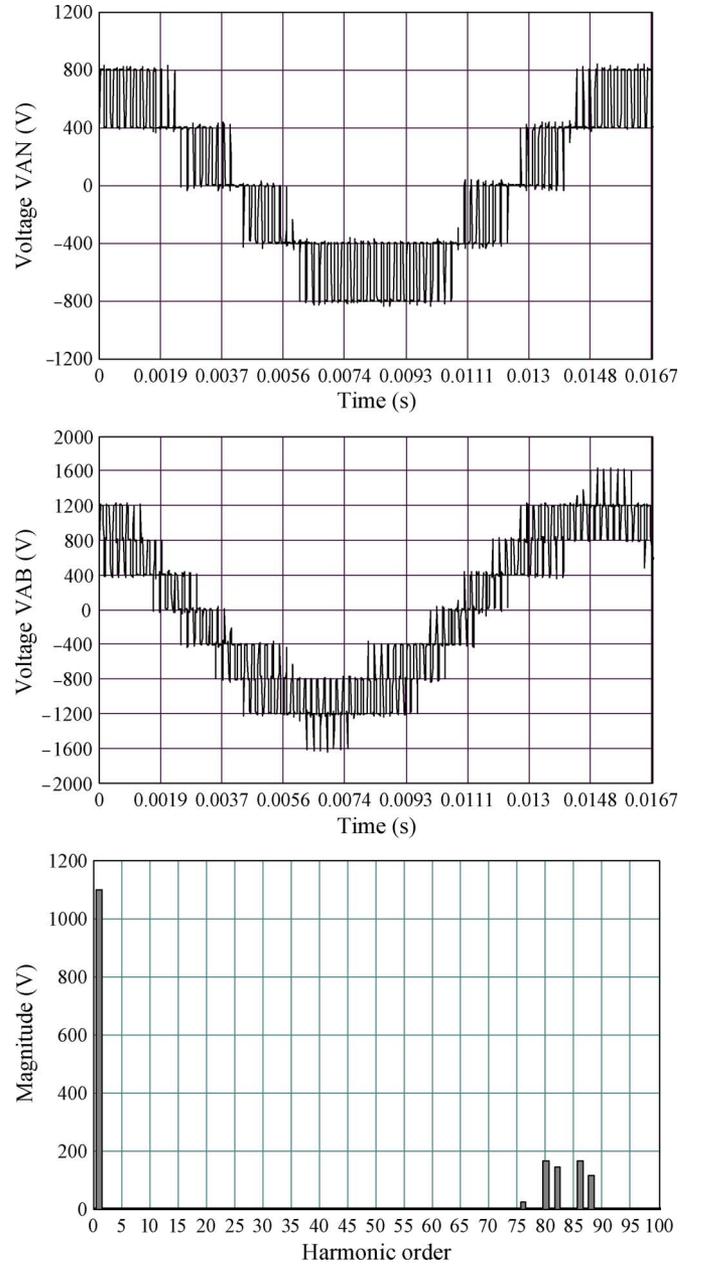
$v_{AB}(t)$ for N_c cells, including harmonics, the method developed in [23] is considered. As a result, voltages $v_{AN}(t)$ and $v_{AB}(t)$ can be respectively represented by

$$\begin{aligned}
 v_{AN}(t) &= N_c M V_{dc} \cos(\omega_o t + \theta_o) \\
 &+ \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} J_{(2n-1)}(N_c m \pi M) \\
 &\times \sin\left([2N_c m + (2n-1)] \frac{\pi}{2}\right) \\
 &\times \cos(2N_c m \omega_c t + (2n-1)\omega_o t) \\
 v_{AB}(t) &= \sqrt{3} N_c M V_{dc} \cos\left(\omega_o t + \frac{\pi}{6}\right) \\
 &+ \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} J_{(2n-1)}(N_c m \pi M) \\
 &\times \sin\left([2N_c m + (2n-1)] \frac{\pi}{2}\right) \\
 &\times \sin\left([2N_c m + (2n-1)] \frac{\pi}{3}\right) \\
 &\times \cos\left(2N_c m \left(\omega_c t - \frac{\pi}{3}\right) \right. \\
 &\quad \left. + (2n-1) \left(\omega_o t - \frac{\pi}{3}\right) + \frac{\pi}{2}\right). \quad (11)
 \end{aligned}$$

By means of these equations, it is possible to forecast the magnitude of every harmonic, and thus, the output filter can be easily designed, if it is necessary.

By using the time-domain data generated by (12), each desired harmonic component can be calculated through fast Fourier transformer techniques, and thus, a more detailed analysis of the harmonic spectrum can be done. Once the harmonics are obtained, the total harmonic distortion (THD) can also be calculated using

$$THD_V = \sqrt{\sum_{n=2}^{\infty} \left(\frac{V_{n_ef}}{V_{1_ef}}\right)^2}. \quad (13)$$

Fig. 6. Waveforms generated by (11) and (12) and harmonic spectrum of the output voltage $v_{AB}(t)$.

Equations (11) and (12) show explicitly that the carrier angular frequency ω_c is multiplied by $2N_c$. Thus, the voltage harmonics will also be multiplied by $2N_c$. Hence, once the number of power cells is defined, it is possible to determine the frequency of undesirable harmonics.

Equations (11) and (12) are represented in a graphical form in Fig. 6, for an inverter using two power cells per phase, a switching frequency of 1260 Hz, V_{dc} of 400 V, an output frequency of 60 Hz, and an rms fundamental output voltage of 784 V, generating a line-to-line output voltage with nine levels and a phase-to-neutral voltage with five levels. The maximum line-to-line output voltage and the phase-to-neutral voltage will be 1600 and 800 V, respectively.

For the same conditions, numerical simulations in PSIM software are carried out for validation, as shown in Fig. 7.

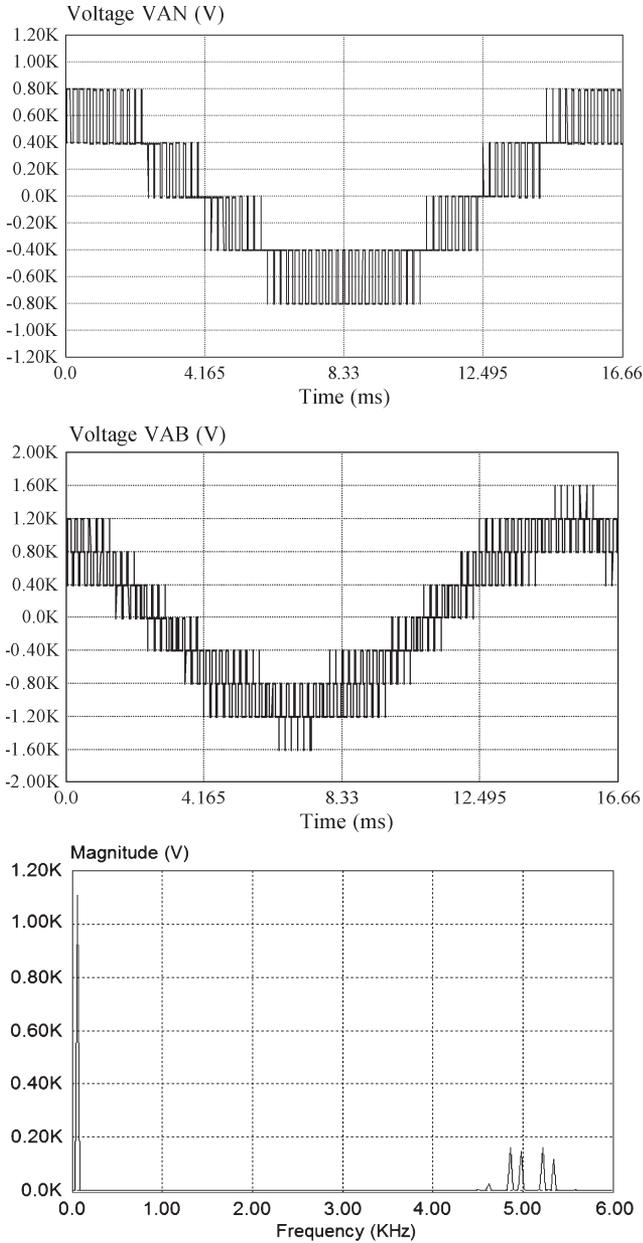


Fig. 7. Numerical simulation waveforms obtained through PSIM software.

In Figs. 6 and 7, the harmonic spectrum of the line-to-line output voltage is also presented. It can be observed that the voltage harmonics are multiplied by $2N_c$.

THD was calculated using (13), obtaining 32% as a result. A similar THD was obtained through PSIM software.

Similar results for the harmonic spectrum and THD can be found in CHB multilevel inverters, using the same modulation strategy. Instantaneous voltages $v_{AN}(t)$ and $v_{AB}(t)$, derived from the CHB inverter [22], do not present relevant differences when compared with (11) and (12).

IV. EXPERIMENTATION

A 15-kW three-phase multilevel inverter was implemented using an inductive–resistive load (displacement power factor of 0.93), connected in delta, with a modulation index of 0.8 and a

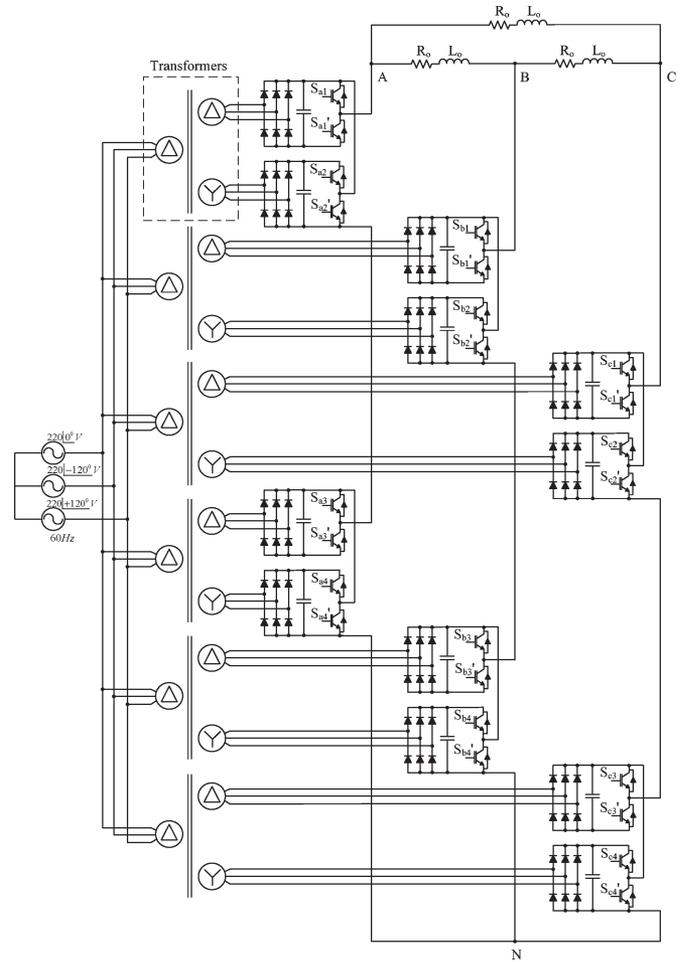


Fig. 8. Implemented three-phase multilevel inverter.

carrier wave frequency of 1260 Hz. The converter is supplied by the power grid (220 V and 60 Hz).

The frequency modulation index is defined by

$$m_f = \frac{f_c}{f_o} \quad (14)$$

where f_c and f_o are the frequencies of the modulating and carrier waves, respectively.

To obtain nine levels in the load voltage, according to (1), it is necessary to use two cells in cascade in each phase ($N_c = 2$), requiring a total of six power cells in a three-phase system.

The amplitude of each isolated source has the value of 400 V and will supply a power of 1.25 kW. Consequently, each voltage step has a value of 400 V. As a result, the load voltage will reach 1600 V due to the nine levels imposed. A 12-pulse rectifier was used in each cell to obtain a better performance. Figs. 8 and 9 show, respectively, a multilevel inverter schematic and a picture of the complete circuit implemented.

The line-to-line voltage v_{AB} reached a maximum value of 1600 V, being composed of nine levels (Fig. 10). The rms line-to-line voltage reached a value of approximately 782 V with an rms current of 6.4 A. In Fig. 11, the harmonic spectrum of the line-to-line voltage in the load is presented. This waveform is

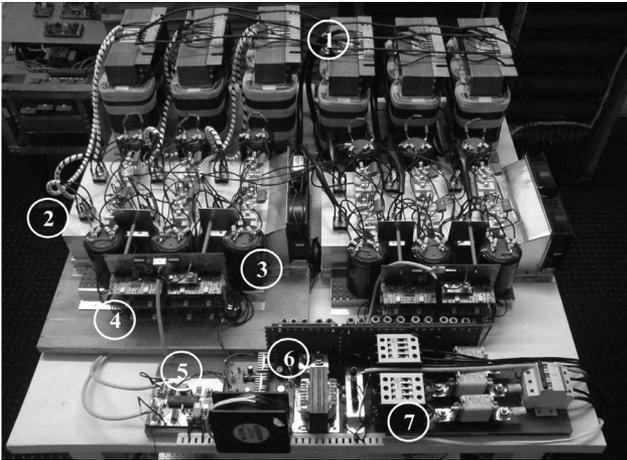


Fig. 9. Prototype of a 15-kW multilevel inverter with nine levels in the output voltage. The photograph shows the (1) transformers, (2) commutation cells and full-bridge rectifier on the heatsink, (3) dc-link capacitors, (4) IGBT drivers, (5) gate signal circuit, (6) auxiliary power supply, and (7) circuit protection.

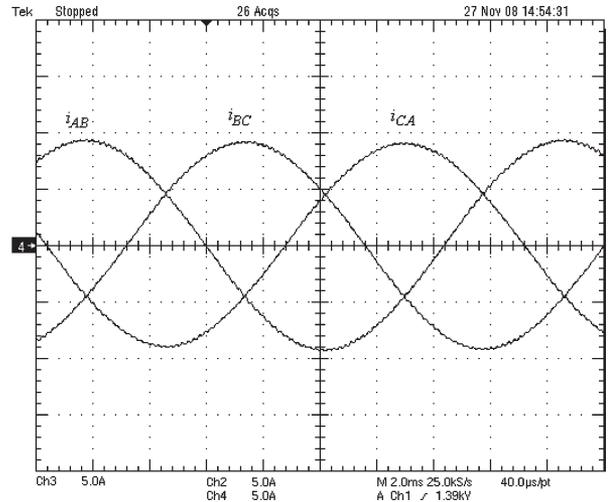


Fig. 12. Three-phase load currents.

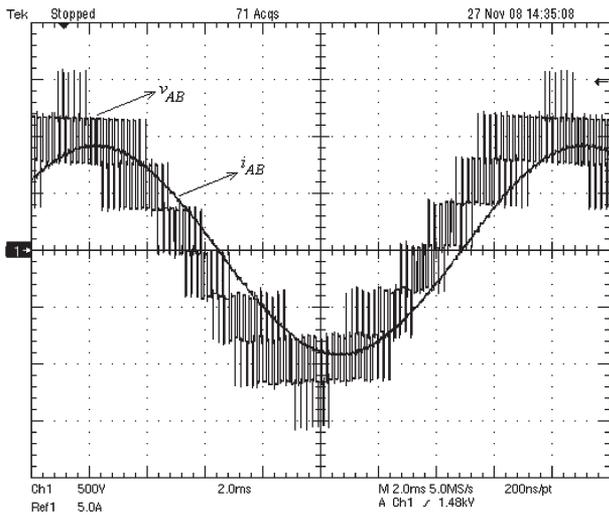


Fig. 10. Load voltage (v_{AB}) and current (i_{AB}).

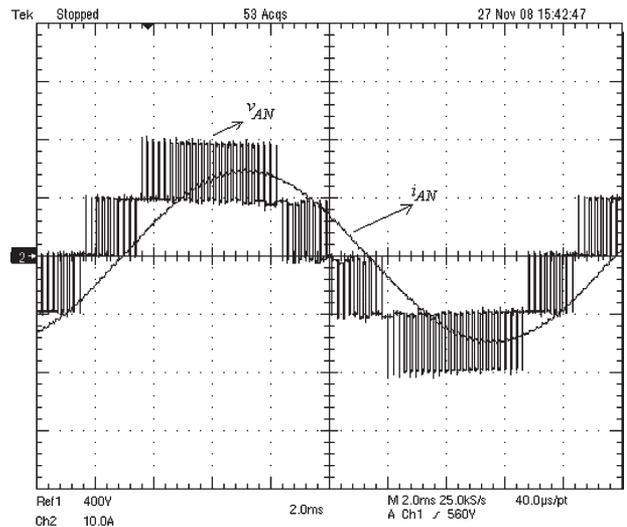


Fig. 13. Voltage (v_{AN}) and current (i_{AN}) in the phase.

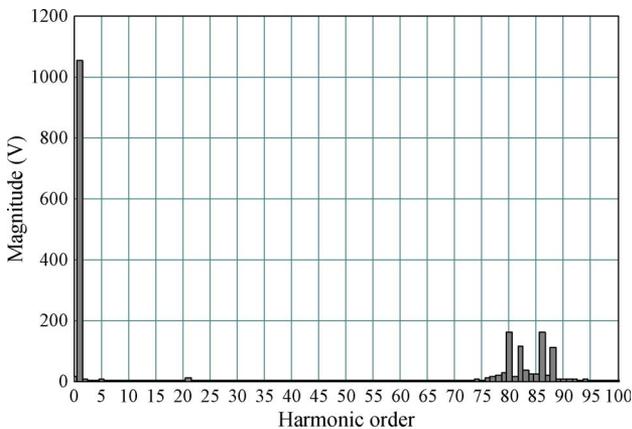


Fig. 11. Harmonic spectrum of the line-to-line output voltage v_{AB} .

similar to those observed in the theoretical (Fig. 6) and simulated (Fig. 7) graphs. It can be observed that the undesirable voltage harmonics were multiplied by $2N_c$, agreeing with (12). The THD of the output voltage is also approximately 32%. The

three-phase load currents shown in Fig. 12 present a sinusoidal format.

Fig. 13 shows the phase-to-neutral voltage with five levels. Each step has a value of 400 V reaching 800 V. The current presents a sinusoidal format, with a peak value of approximately 10 A and a frequency of 60 Hz. The average dc voltage in this figure is zero and the peak voltage does not cross the maximum phase voltage represented by $N_c V_{dc} M$, in accordance with (8), because of the connection done in Fig. 2(b).

In Fig. 14, the switch voltage waveform is shown. Although the output voltage is high, the maximum voltage over the switches has a value of 400 V. The maximum current value in the switches is approximately 16.4 A. The waveforms for all the inverter switches have the same format, however, with the phase shift defined by (10).

The voltage and current on one of the dc links are shown in Fig. 15. The dc source has a magnitude of $V_{dc} = 400$ V with small ripple. The inverter is composed of 12 isolated continuous sources, each one supplying a power of 1.25 kW, totaling 15 kW.

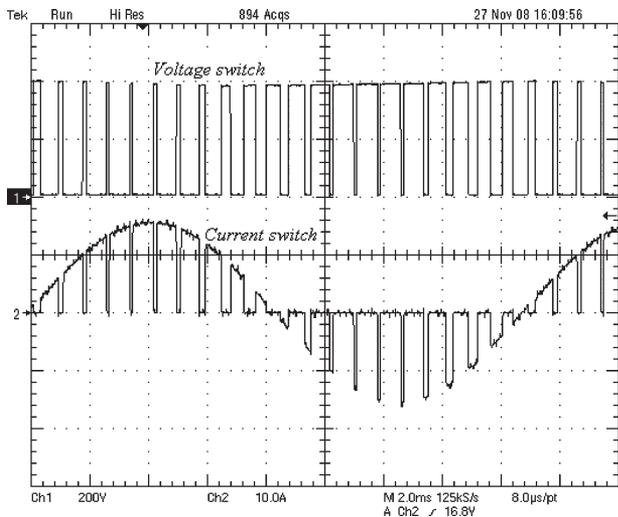
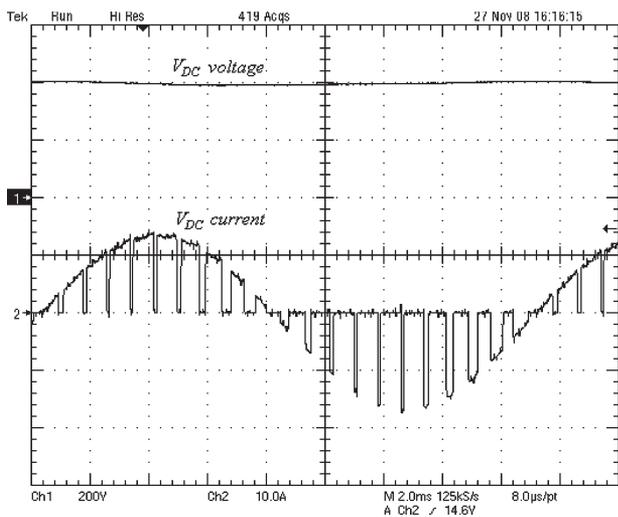


Fig. 14. Voltage and current in the switches.

Fig. 15. Voltage and current in the isolated source V_{dc} .

V. COMPARISON BETWEEN THE PROPOSED INVERTER AND CHB MULTILEVEL INVERTER

The main difference between the proposed topology and a CHB inverter is the way how the inverter legs are connected.

These two converters have the same number of switches on each power cell; thereby, the voltage levels generated in the terminals of each power cell are the same. Thus, the numbers of voltage levels of the phase-to-neutral voltage (v_{AN}) and line-to-line output voltage (v_{AB}) will also be the same, as described in Table I.

Each power cell in the proposed topology employs double the number of isolated dc voltage sources, with half the power.

The PWM phase-shifted multicarrier modulation technique used in the proposed topology is similar to that used in CHB multilevel inverters. However, if other modulation techniques are employed, for instance, PWM level-shifted multicarrier modulation or space vector modulation, accurate analysis should be done.

THDs in the load current and line-to-line output voltage were compared in those two converters with the same parameters.

TABLE I
COMPARISON BETWEEN THE PROPOSED INVERTER AND CHB MULTILEVEL INVERTER

Topology	Proposed inverter	Cascaded H-bridge inverter
Phase-to-neutral voltage levels	np	np
Line-to-line voltage levels	$2np-1$	$2np-1$
Number of power cells per phase	$(np-1)/2$	$(np-1)/2$
Number of switches per phase	$2(np-1)$	$2(np-1)$
Number of isolated dc voltage sources per phase	$(np-1)$	$(np-1)/2$
Load voltage THD	Similar	Similar
Modulation strategy	Similar	Similar
Power of each isolated dc voltage source	$\frac{P_{\text{nominal}}}{3(np-1)}$	$\frac{2P_{\text{nominal}}}{3(np-1)}$

Similar results are obtained by using numerical simulations (PSIM software).

Harmonic spectrum for the proposed topology was defined by (12), and an equivalent illustration for CHB multilevel inverters, using PWM phase-shifted multicarrier modulation, can be found in [22], showing the similarity between them.

VI. CONCLUSION

A three-phase multilevel inverter has been proposed, and its principle of operation has been confirmed by simulations and experimental results.

The applied PWM phase-shifted multicarrier modulation technique shows satisfactory performance.

Analytical equations for line-to-line and phase-to-neutral output voltages were developed. Once the number of power cells is chosen, through these equations, it is possible to calculate the magnitude of every harmonic component, and therefore, it is possible to determine the frequency of undesirable harmonics for design purposes.

A comparison between the proposed topology and the CHB multilevel inverter was also presented, showing similar characteristics; thus, the topology described in this paper can be seen as an alternative to be applied in similar applications.

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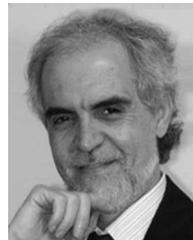
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