Three-Phase Push–Pull DC–DC Converter: Analysis, Design, and Experimentation

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***Abstract*—This paper presents a voltage-fed three-phase push–pull dc–dc converter. The main characteristics of the proposed converter are: small volume, low weight, reduced number of components, low voltage across the power semiconductors for duty cycles less than 1/3, and input current ripple cancellation when the duty cycle is equal to 1/3. Typical applications include battery chargers, electric vehicles, and renewable energy systems. The paper presents a theoretical analysis, design example, and experimental data for a 650 W, 150-125 VDC input, 75 VDC output, and 42 kHz switching frequency laboratory prototype. The measured performance agreed well with the theoretical predictions. The measured efficiency for 125 VDC input at full load is 95%.**

***Index Terms*—Isolated dc–dc converter, push–pull converter, three-phase dc–dc converter.**

I. Introduction

ISOLATION, high-power density, low cost, and high efficiency are all characteristics that are required in applications such as battery chargers, electric vehicles, and telecom, military, medical, and renewable energy systems.

This work proposes a voltage-fed three-phase isolated push–pull dc–dc converter, as shown in Fig. 1, which meets the main attributes of the classical push–pull dc–dc converter [1]–[10], shown in Fig. 2, and the three-phase isolated full-bridge dc–dc converter [11]–[19], shown in Fig. 3. The advantages of the proposed structure include:

1) Low conduction losses since there is only a single device voltage drop at the input and output and the rms current of the power components are low;
2) Reduced number of components when compared to the classical three-phase dc–dc converter shown in Fig. 3: three switches, three diodes, a three-phase transformer (T), a filter inductor (L_f), and a filter capacitor (C_o);
3) Good transformer copper and core utilization since the windings are placed in a common magnetic core;
4) The switches can be driven directly by the control circuit since all of the switches are connected to the same reference point;
5) Small output filter size (L_f, C_o) since the frequency of the output ripple current is three times the switching frequency $(3f_s)$; and

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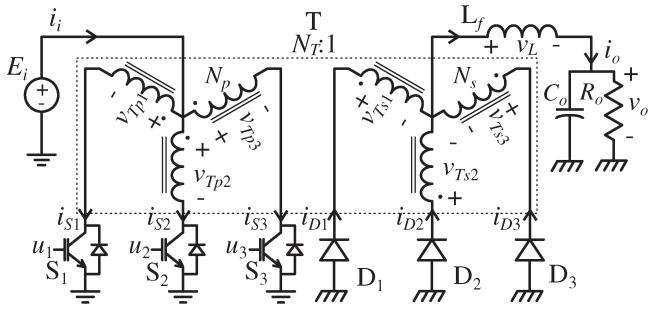

Fig. 1. Three-phase push–pull dc–dc converter.

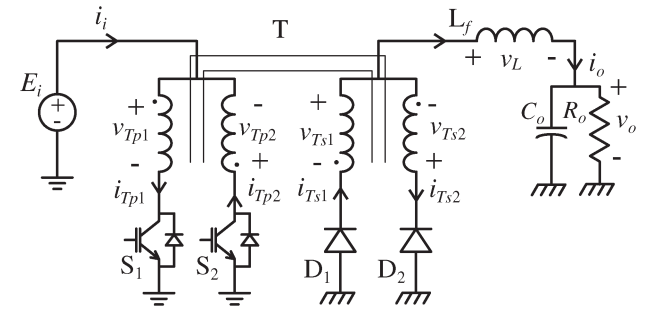

Fig. 2. Conventional push–pull dc–dc converter.

6) The maximum voltage of any switch is only one and a half times the input voltage $(3E_i/2)$.

The small number of components and the reduction in transformer and in output filter sizes allows for high-power density. Additionally, the reactive energy of the output filter (L_f, C_o) is zero when the duty cycle is equal to 1/3 (≈33.33%).

Despite the advantages presented by the three-phase push–pull converter as with all double-ended topologies, it is susceptible to transformer core saturation due to an imbalance in the volt-seconds applied to the phases, which causes some dc bias in the magnetizing current. Therefore, when a regulated voltage is required, current-mode control is suitable for this topology.

II. Circuit Operation

To simplify the explanation and the analysis of the converter operating principle, the following assumptions are made: 1) the converter operates in steady state; 2) all components are ideal; 3) output capacitor C_o is large enough to be considered a continuous output voltage; 4) the three-phase high-frequency transformer is symmetrical; and 5) the switches are driven by symmetrical three-phase signals as shown in Fig. 5.

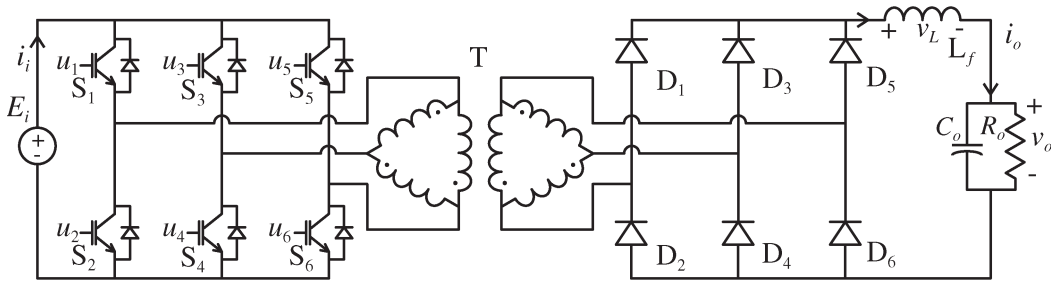

Fig. 3. Three-phase isolated dc–dc converter.

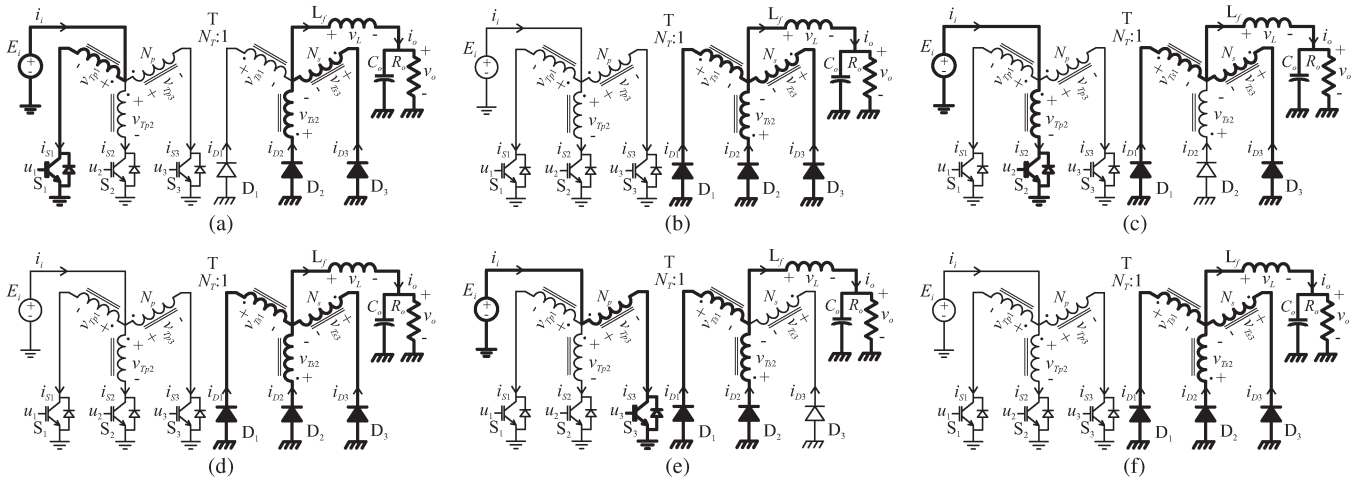

Fig. 4. Topological stages of CCM for duty cycle smaller than 1/3. In the first, third, and fifth stages inductor, L_f stores energy. In the second, fourth, and sixth stages, this energy is transferred to the load. (a) First stage (t_0, t_1). (b) Second stage (t_1, t_2). (c) Third stage (t_2, t_3). (d) Fourth stage (t_3, t_4). (e) Fifth stage (t_4, t_5). (f) Sixth stage $(t_5, t_0 + T_s)$.

The proposed converter presents two operation modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The switching transistors can be driven using a duty cycle in the range of 0 to 2/3, defined as the amount of time the switch is on in relation to the switching period: $D = t_{\rm on}/T_s$. However, duty cycles above 1/3 are avoided because this leads to a high voltage stress across semiconductor devices. Thus, in this paper, only operating principle in CCM and DCM modes for duty cycle range of 0 to 1/3 is described.

A. Continuous Conduction Mode for $D < 1/3$

CCM means that the current through inductor L_f never falls to zero between switching cycles.

During a switching period, the converter goes through six topological stages as shown in Fig. 4 and described in detail below.

The timing sequences for the three switches and the resulting circuit voltages and currents are shown in Fig. 5.

1) First Stage $[t_0, t_1]$*:* During this stage, power is transferred from the input source (E_i) to the load through active switch S_1 and diodes D_2 and D_3. Part of the energy transferred from the input source is stored in the inductor.

The first stage starts at instant t_0 when switch S_1 is turned on. The input voltage is applied to the corresponding transformer primary winding $(v_{T1p} = E_i)$, and thus, half the input voltage is induced across other primary windings $(v_{T2p} = v_{T3p} = E_i/2)$. Diodes D_2 and D_3 conduct the output current, consequently the current through switch S_1 is half the output current referred to the primary side $(i_L/2N_T)$. The voltages across the switches and diode that are off are $3E_i/2$ and $-3E_i/2N_T$, respectively. This stage ends when switch S_1 is turned off at instant t_1.

The third and fifth stages are similar to the first stage. In the third stage, the power is transferred through S_2, D_1, and D_3 and in the fifth stage through S_3, D_1, and D_2.

2) Second Stage $[t_1, t_2]$*:* During this stage, the energy stored in L_f is transferred to the load when all of the switches are off. This stage also corresponds to the second, fourth, and sixth stages.

The second stage starts at instant t_1 when switch S_1 is turned off. All of the diodes are forward biased. The voltage across the primary and secondary windings of the transformer is zero. The output voltage is applied to the inductor $(v_L = -V_o)$. The current through each diode is one-third of the inductor current $(i_L/3)$. The voltage across the switches is equal to the input voltage (E_i). This stage ends at instant t_2 when switch S_2 is turned on.

B. Discontinuous Conduction Mode for $D < 1/3$

In this mode, the inductor current falls to zero and remains there for part of the switching cycle. This occurs in the second, fourth, and sixth stages (Fig. 5) where the energy stored in the inductor is transferred to the load.

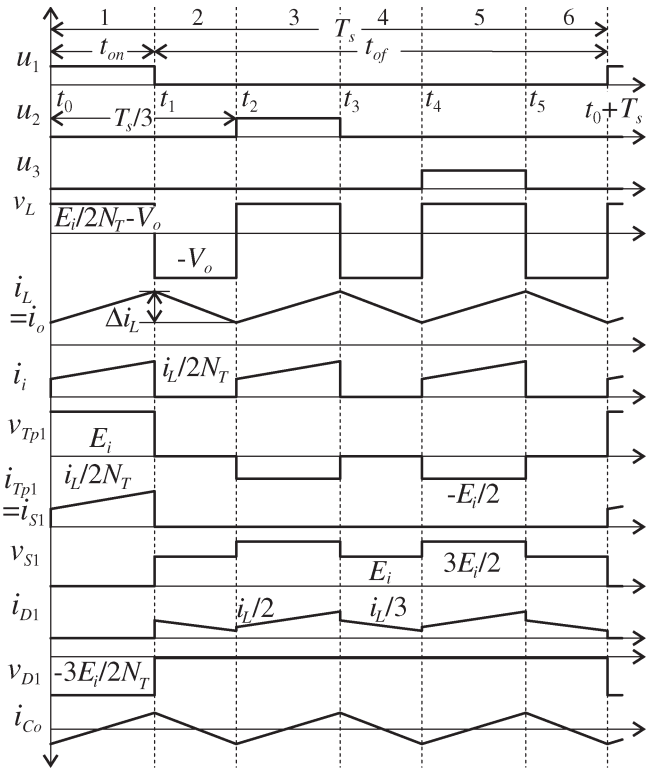

Fig. 5. Main waveforms of CCM for duty cycle smaller than 1/3.

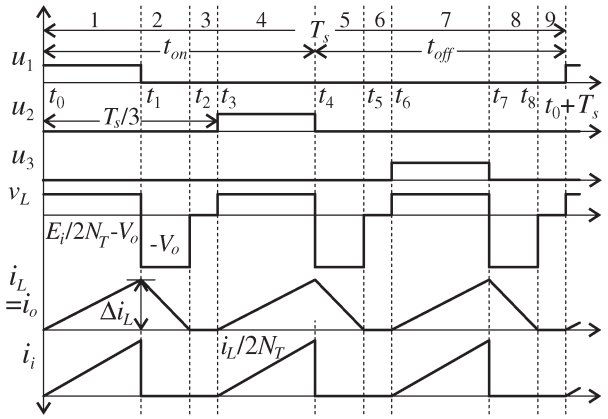

Fig. 6. Main waveforms of the DCM for duty cycle smaller than 1/3.

The main waveforms in DCM are shown in Fig. 6. During a switching cycle, the converter presents nine stages.

The *first* and *second stages* in the DCM are similar to the first and second stages of the CCM. The only difference is that the second stage ends when the inductor current reaches zero at instant t_2.

The *third stage* starts at instant t_2. The voltage across the inductor is zero. The diodes of the half bridge rectifier are reverse biased by the output source, and only the capacitor supplies the load. The input voltage is applied across the switches. This stage ends at instant t_3, when switch S_2 is turned on.

The remaining stages follow the same pattern using switches S_2 and S_3.

III. Mathematical Analysis

In this section, the main equations to compute the voltage and current stresses for design of the proposed converter in CCM are developed. The static gain expression for the DCM is also derived.

A. Static Gain

1) Static Gain in CCM: The average inductor voltage considering the assumptions detailed in the previous section is null for a 1/3 switching frequency

$$V_L = \frac{3}{T_s}\int_{t_0}^{T_s/3} v_L\,dt = 0 \tag{1}$$

The substitution of instantaneous inductor voltage shown in Fig. 5 yields

$$\left(\frac{E_i}{2N_T} - V_o\right)\frac{t_{\rm on}}{T_s} = V_o\left(\frac{1}{3} - \frac{t_{\rm on}}{T_s}\right) \tag{2}$$

Thus, the static gain of CCM is given by

$$\frac{V_o}{E_i} = \frac{3D}{2N_T}. \tag{3}$$

2) Static Gain in DCM: In DCM, the static gain is a function of the duty cycle and the output current.

The average value of the input current, shown in Fig. 6, is calculated using

$$I_i = \frac{3}{T_s}\frac{t_{\rm on}\Delta I_L}{4N_T} \tag{4}$$

where the current ripple is given by

$$\Delta I_L = \left(\frac{E_i}{2N_T} - V_o\right)\frac{t_{\rm on}}{L_f}. \tag{5}$$

Ideally, the relationship between the average input current and the average output current is

$$I_i = I_o\frac{V_o}{E_i}. \tag{6}$$

The normalized current equation is obtained by substituting (5) and (6) into (4)

$$\overline{I_o} = \frac{I_o L_f}{T_s E_i} = \frac{3D^2}{4N_T}\left(\frac{E_i}{2N_T V_o} - 1\right) \tag{7}$$

The static gain of the DCM is given by

$$\frac{V_o}{E_i} = \frac{1}{2N_T}\frac{3D^2}{4N_T\overline{I_o} + 3D^2} \tag{8}$$

B. Output Characteristic

Using the static gain equations, (3) and (8), and considering unity for the turns ratio of the transformer, $N_T = 1$, the output characteristic of the proposed converter is plotted as shown in Fig. 7. The boundary conduction mode (BCM) of the push–pull converter and the proposed three-phase push–pull converter are indicated in the plot. The comparison shows that the DCM

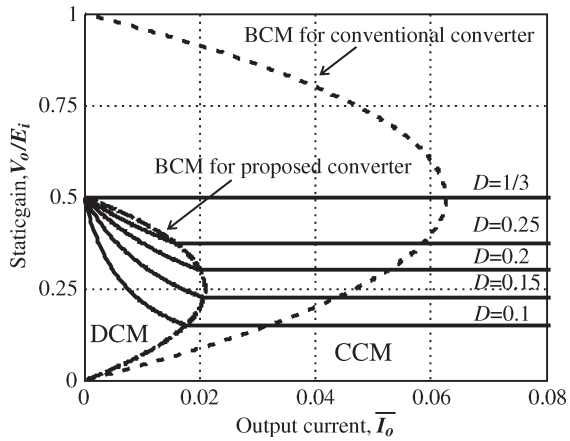

Fig. 7. Output characteristic of the proposed three-phase push–pull converter and the BCM of the conventional push–pull converter for $N_T = 1$.

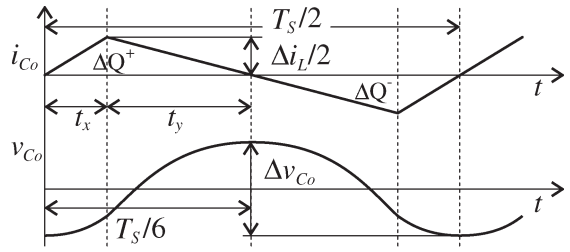

Fig. 8. Current and voltage ripple in the capacitor in CCM.

region of the conventional converter is more broad than that of the proposed converter at its widest point. The maximum static gain of the proposed converter is half the maximum static gain of the conventional push–pull converter.

C. Current Ripple

The current ripple in the inductor in CCM can be calculated during the storage stage or transfer stage. From Fig. 5, the inductor voltage during the storage stage is given by

$$v_L = L_f \frac{di_L}{dt} = L_f \frac{\Delta i_L}{t_{\rm on}} = \frac{E_i}{2N_T} - V_o. \tag{9}$$

Solving (9) yields

$$\overline{\Delta i_L} = \frac{L_f \Delta i_L}{V_o T_s} = \left(\frac{E_i}{2N_T V_o} - 1\right) \frac{t_{\rm on}}{T_s}. \tag{10}$$

The normalized current ripple for CCM is obtained by substituting (3) into (10)

$$\overline{\Delta i_L} = \frac{1 - 3D}{3} \tag{11}$$

D. Filter Capacitor

The output voltage ripple and the RMS current of the capacitor for CCM are obtained using the waveforms shown in Fig. 8.

1) Output Voltage Ripple: The output voltage ripple caused by charge variation in the capacitor is given by

$$\Delta v_o = \frac{\Delta Q^+}{C_o}. \tag{12}$$

According to Fig. 8, the positive charge is

$$\Delta Q^+ = \frac{\Delta i_L T_s}{24} \tag{13}$$

Thus, the output ripple is obtained by substituting (13) into (12)

$$\Delta v_o = \frac{\Delta i_L}{24 f_s C_o} \tag{14}$$

Alternatively, the output voltage ripple is expressed in a normalized form as

$$\overline{\Delta v_o} = \frac{\Delta v_o L_f C_o f_s^2}{V_o} = \frac{\overline{\Delta i_L}}{24} = \frac{1 - 3D}{72}. \tag{15}$$

2) RMS Current: For the current waveform shown in Fig. 8, the rms current is given by

$$I_{Crms} = \frac{\Delta i_L}{4\sqrt{3}} \frac{T_s - 6t_x}{3t_y}. \tag{16}$$

The relationship between t_x and t_y is

$$t_x + t_y = \frac{T_s}{6}. \tag{17}$$

Substituting (17) into (16) yields

$$I_{Crms} = \frac{\Delta i_L}{2\sqrt{3}}. \tag{18}$$

Equation (18) shows that the rms current through the capacitor transformer is directly proportional to the inductor current ripple. Therefore, the maximum value of one occurs when the other also assumes its maximum value.

E. Three-Phase Transformer

The rms values of the currents passing through primary and secondary transformer windings are computed neglecting the inductor current ripple. Thus, the transformer rms currents are given by

$$I_{T p\rm rms} = \frac{I_L}{2N_T}\sqrt{D}. \tag{19}$$

$$I_{T s\rm rms} = \frac{I_L}{3}\sqrt{\frac{3D+2}{2}}. \tag{20}$$

F. Semiconductors

1) Switches: The rms current of the switch is equal to the RMS current of the transformer primary winding ($I_{S\rm rms} = I_{T p\rm rms}$). The average current of the switch (I_S) is a third of the average input current

$$I_S = \frac{I_i}{3} \tag{21}$$

The maximum voltage across the switch occurs during the storage stage as shown in Fig. 5, where the voltage is

$$V_{S\max} = \frac{3}{2} E_i \tag{22}$$

TABLE I
COMPARISON OF PUSH–PULL CONVERTERS

	Push-pull converter	
Parameters	Proposed	Conventional
G_{mcc}	$\frac{3D}{2N_T}$	$\frac{2D}{N_T}$
$\overline{\Delta I_L}$	$\frac{1-3D}{3}$	$\frac{1-2D}{2}$
ΔV_o	$\frac{\Delta I_L}{24 f_s C_o}$	$\frac{\Delta I_L}{16 f_s C_o}$
I_{Crms}	$\frac{\Delta I_L}{2\sqrt{3}}$	$\frac{\Delta I_L}{2\sqrt{3}}$
I_{Tprms}/I_L	$\frac{\sqrt{D}}{2N_T}$	$\frac{\sqrt{D}}{N_T}$
I_{Tsrms}/I_L	$\frac{\sqrt{3D+2}}{3\sqrt{2}}$	$\frac{\sqrt{2D+1}}{2}$
I_S, I_D	$\frac{I_i}{3}, \frac{I_o}{3}$	$\frac{I_i}{2}, \frac{I_o}{2}$
V_S, V_D	$\frac{3E_i}{2}, \frac{3E_i}{2N_T}$	$2E_i, \frac{2E_i}{N_T}$

2) Diodes: The rms current of the diode is equal to the rms current of the transformer secondary winding ($I_{D\mathrm{rms}} = I_{Ts\mathrm{rms}}$). The average current of the diode (I_D) is a third of the average inductor current

$$I_D = \frac{I_L}{3} \tag{23}$$

The maximum voltage across the diode occurs during the storage stage

$$V_{D\max} = \frac{3}{2N_T} E_i \tag{24}$$

IV. COMPARISON BETWEEN PROPOSED CONVERTER AND CONVENTIONAL PUSH–PULL CONVERTER

The main equations for the conventional push–pull converter (Fig. 2) operating in CCM are obtained using a similar procedure employed for the proposed converter, and these equations are listed in Table I. It can be observed that the current and voltage ripples are zero for duty cycle of 1/2 and 1/3 in the conventional and proposed converter, respectively. However, the conventional converter does not admit this operation duty cycle since it causes short-circuiting of the input source. On the other hand, a duty cycle of 1/3 is admitted in the proposed converter. This characteristic is of great interest for applications which do not require voltage regulation, since it reduces the current and voltage ripples providing smaller filter sizes. Moreover, the input current of the proposed converter is continuous, minimizing the input filter size.

For applications that require voltage regulation, the project design should seek operation close to these duty cycles because this minimizes the filter sizes. Considering the same project specifications, the comparison shows that the inductance and the capacitance required from the filters of the proposed converter are 3/2 less than those ones required by the conventional push–pull converter. In addition, the switches of the latter are generally controlled with duty cycles of less than 45% to guarantee safe operation. Consequently, filter sizes of the conventional push–pull converter cannot be reduced to the same extent as those of the proposed converter.

TABLE II
DESIGN SPECIFICATIONS OF THE PROTOTYPE

Parameters		Value
Input voltage (E_i)	:	150∼125 VDC
Output voltage (V_o)	:	75 VDC
Output power (P_o)	:	650 W
Switching frequency (f_s)	:	42 kHz
Current ripple in L_f (ΔI_L)	:	20 %
Voltage ripple in C_o (ΔV_o)	:	0.2 %

Considering the current stresses, the semiconductors of the proposed converter have smaller values than conventional converter, permitting a better heat transfer generated from semiconductor power losses. Thus, the proposed converter is able to drive a greater power ratio than the conventional one. Furthermore, the switch voltage stress of the former is lower, and, consequently, the switching power loss is also lower.

V. DESIGN EXAMPLE

To illustrate the analysis and discussion, a prototype was built with the parameters presented in Table II. The design specification was selected considering the availability of components and equipment to construct and test a laboratory prototype, and the purpose is to verify the operation of the proposed converter.

A. Power Transformer

The turns ratio of the transformer is calculated from (3) and by selecting $D_{\max} = 0.3$ as the duty cycle

$$N_T = \frac{3E_{i\min}D_{\max}}{2V_o} = \frac{3 \cdot 125 \cdot 0.3}{2 \cdot 75} = 0.75. \tag{25}$$

Assuming an efficiency of $\eta = 95\%$, the average inductor current is

$$I_L = \frac{P_o}{V_o \eta} = \frac{650}{75 \cdot 0.95} = 9.11 \text{ A}. \tag{26}$$

Using (19) and (20), the RMS currents of the primary and secondary windings of the transformer are calculated as

$$I_{Tpef} = \frac{I_L}{2N_T}\sqrt{D_{\max}} = 3.32 \text{ A} \tag{27}$$

$$I_{Tsef} = \frac{I_L}{3}\sqrt{\frac{3D_{\max}+2}{2}} = 3.65 \text{ A}. \tag{28}$$

Limiting the current density to $J_{\max} = 380$ A/cm^2 and the flux density to $B_{\max} = 0.25$ T ($\Delta B = 2B_{\max}$, operation in two

quadrants) and assuming a window utilization factor of $k_w = 0.3$, the resulting area product of the transformer is

$$A_e A_w = \frac{2N_T V_o \cdot 10^4}{3 f_s J_{\max} \Delta B k_w} \left(2I_{T\text{prms}} + 2\frac{I_{T\text{srms}}}{N_T}\right) [\text{cm}^4]$$
$$= \frac{2 \cdot 0.75 \cdot 75 \cdot 10^4}{3 \cdot 42000 \cdot 380 \cdot 0.50 \cdot 0.3} \left(2 \cdot 3.32 + 2\frac{3.65}{0.75}\right)$$
$$= 2.58 \text{ cm}^4. \quad (29)$$

The EE-55/28/21 (Thornton) magnetic core was selected. The number of turns of the primary and secondary windings were $N_{Tp} = 12$ and $N_{Ts} = 16$, respectively.

B. Filter Inductor

The maximum current ripple occurs at the maximum input voltage, when the duty cycle is minimum

$$D_{\min} = \frac{2N_T V_o}{3E_{imax}} = \frac{2 \cdot 0.75 \cdot 75}{3 \cdot 150} = 0.25. \quad (30)$$

Thus, the maximum normalized current ripple is

$$\overline{\Delta i_{L(D_{\min})}} = \frac{1 - 3D_{\min}}{3} = \frac{1 - 3 \cdot 0.25}{3} = 0.083. \quad (31)$$

The inductance is obtained using (11)

$$L_f = \frac{V_o \overline{\Delta i_{L(D_{\min})}}}{f_s \Delta i_L} = \frac{75 \cdot 0.083}{42000 \cdot 9.11 \cdot 0.2} = 81\ \mu\text{H} \quad (32)$$

Employing $J_{\max} = 380$ A/cm^2, $B_{\max} = 0.25$ T and $k_w = 0.4$, the area product is

$$A_e A_w = \frac{L_f I_L^2 (1 + 0.5\Delta I_L)}{J_{\max} B_{\max} k_w} 10^4 \ [\text{cm}^4]$$
$$= \frac{81 \cdot 10^{-6} \cdot 9.11^2 \cdot (1 + 0.1)}{380 \cdot 0.25 \cdot 0.4} 10^4 = 1.94 \text{ cm}^4. \quad (33)$$

Magnetic core EE-42/20 was selected. The number of turns was $N_L = 16$. The measured inductance was 79 μH.

C. Filter Capacitor

The following parameter values are computed:

– Capacitance from (15)

$$C_o = \frac{V_o \overline{\Delta I_{L(D_{\max})}}}{24 f_s^2 \Delta V_o L_f} = \frac{75 \cdot 0.083}{24 \cdot 42^2 \cdot 0.15 \cdot 81} = 12\ \mu\text{F} \quad (34)$$

– Equivalent series resistance (ESR)

$$ESR = \frac{\Delta V_o}{\Delta I_L} = \frac{0.15}{1.82} = 0.082\ \Omega \quad (35)$$

– RMS current from (18)

$$I_{Crms} = \frac{\Delta I_L}{2\sqrt{3}} = \frac{0.2 \cdot 9.11}{2\sqrt{3}} = 0.5 \text{ A}. \quad (36)$$

Using the previously calculated values, two EPCOS B43501 (1000 μF/250 V) capacitors were selected.

D. Semiconductors

The maximum voltage of the switch and the diode are calculated using (22) and (24) for the case of maximum input voltage and result in 225 V and 300 V, respectively. The semiconductors selected were the Cool-MOS/SPP20N60S5 (600 V/20 A) and the SiC-Schottky/SDT10S60 (600 V/10 A). The criterion for selecting these switches was based on the drain to source on resistance. The SiC power diodes were selected because they allow the switching power losses to be minimized due to the relatively high voltage stress.

E. PWM Controller

The prototype is controlled using open-loop control. The gate drive signals were generated by the DSP TMS320LF2407 kit. A nonisolated drive circuit was employed.

VI. Experimental Results

The schematic and the photo of the laboratory prototype of the voltage-fed three-phase isolated push–pull dc–dc converter can be seen in Figs. 9 and 10, respectively. The switches are protected against overvoltage caused by the transformer leakage inductance by means of a passive voltage clamp circuit composed of D4-D6, C3, and R7.

The waveforms shown in Figs. 11 and 12 were obtained for the following parameters: a duty cycle of 26%, an input voltage of 148.7 V, an output voltage of 75 V, and a 657 W load. The results show that the input and output current frequencies are three times higher than the switch and diode current frequencies, the average switch current is a third of the average input current, the average diode current is a third of the average output current, the maximum diode current is half of the output current occurring when one switch is on, and that the maximum voltages across switching devices are 225 V for the transistor switch giving a ratio of $225\ \text{V}/148.7\ \text{V} = 1.51$ and 292 V for the diode giving a ratio of $292\ \text{V}/148.7\ \text{V} = 1.96$. These values closely match the expected theoretical ratios of 3/2 and $3/2N_T$, respectively.

Figs. 11–13 show that the input and output currents are evenly distributed through transistor switches and diodes.

The current waveforms for a duty cycle of 1/3 are shown in Fig. 13. The test parameters were: an input voltage of 75.2 V, an output voltage of 48 V, and a load of 341 W. The results show that both input and output currents are continuous. Furthermore, it can be seen that there is no ac component in the output current, consequently the reactive energy in the output filters are zero. On the other hand, the current waveforms show that the magnetizing current of the three-phase transformer flows through the primary side, causing an ac component in the input current.

The measured efficiencies of the laboratory prototype for maximum and minimum input voltage conditions are shown in Fig. 14. The results were obtained keeping the input and output voltage constant for any load. The curves show that the efficiency is higher for the case of minimum input voltage. This result is due to less reactive energy in the converter and

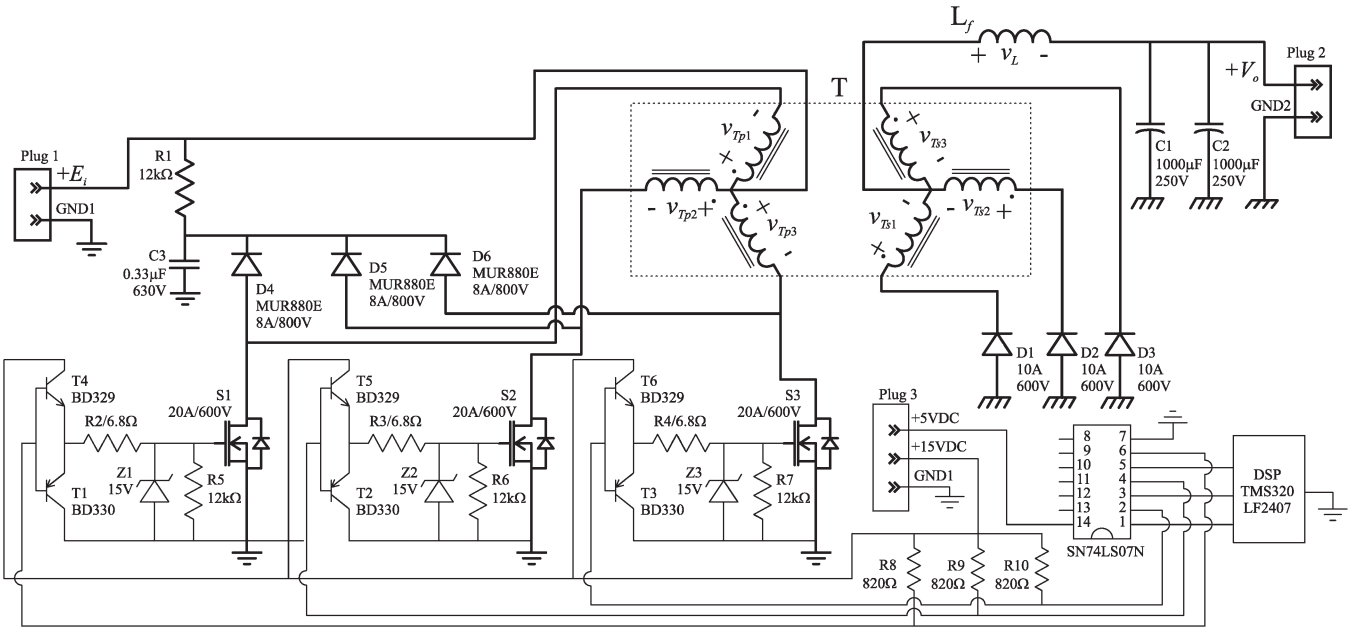

Fig. 9. Schematic of the laboratory prototype.

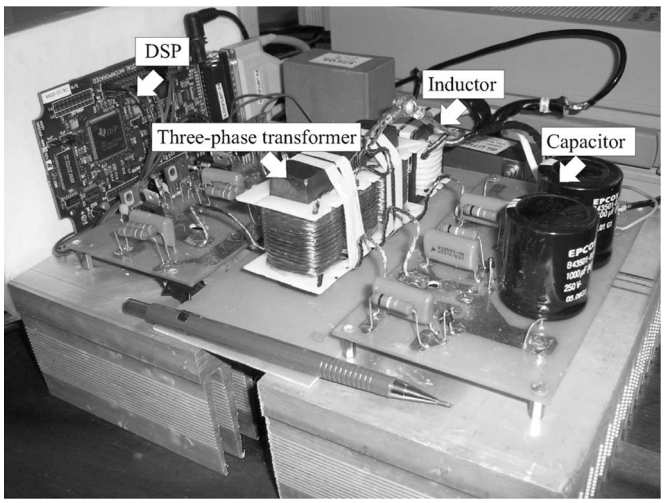

Fig. 10. Picture of the laboratory prototype.

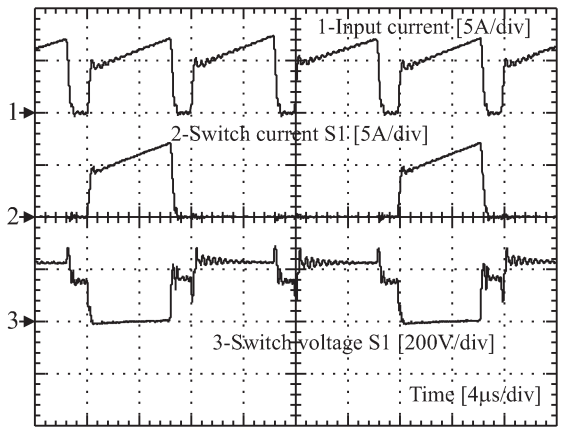

Fig. 11. Input current, and current and voltage of switch S1 for $D = 0.26$, $E_i = 148.7$ V, $V_o = 75$ V and $P_o = 657$ W.

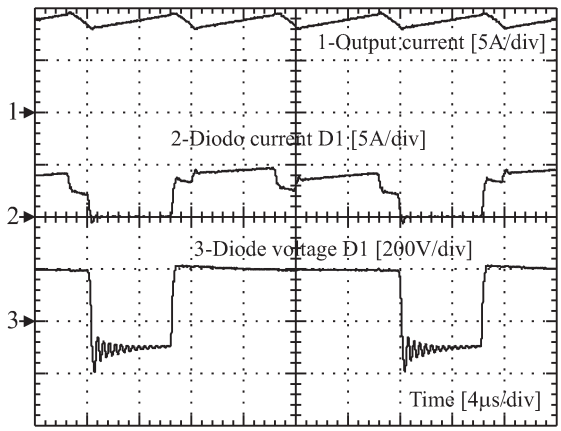

Fig. 12. Output current and current and voltage of diode D1 for $D = 0.26$, $E_i = 148.7$ V, $V_o = 75$ V, and $P_o = 657$ W.

lower voltage stresses on the switching devices that reduce the conduction and switching losses.

VII. Conclusion

From the theoretical analysis and the experimental data, we can draw the following conclusions.

a) Measured performance was in agreement with the theoretical predictions;
b) Measured efficiency of the 650 W designed and implemented laboratory prototype (150 Vdc input to 75 Vdc output with 45 kHz) was 95% at full load;
c) Frequency of the input current and the output current ripple is three times the switching frequency $(3f_s)$;
d) Input current ripple and output voltage ripple cancellation occurs when the converter operates with a duty cycle equal to 1/3;
e) Due to current sharing between the power semiconductors, three-phase high-frequency transformer, and current and voltage ripple cancellation (or attenuation), both the

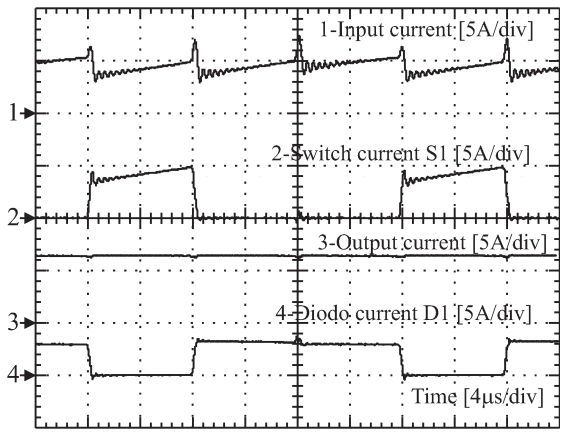

Fig. 13. Input current, current through switch S1, output current, and current through diode D1 for $D = 1/3$, $E_i = 75.2$ V, $V_o = 48$ V and $P_o = 341$ W.

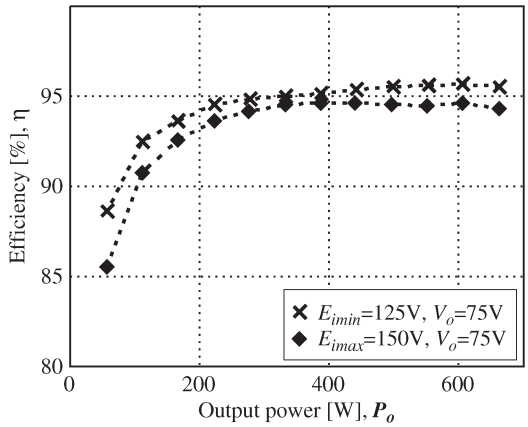

Fig. 14. Measured efficiency of the laboratory prototype for maximum and minimum input voltage.

efficiency and the power density are higher than in the case of the conventional push–pull dc–dc converter.

f) Voltage across a power switches are equal to 3/2 times the input voltage $(3E_i/2)$; furthermore, these devices can be driven by a nonisolated gate driver.

g) Proposed converter is a cost-effective solution for low input voltage isolated dc–dc converters of automotive and renewable energy applications.

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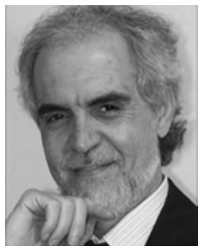

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