A ZVS-PWM Three-Phase Current-Fed Push–Pull DC–DC Converter
Romero Leandro Andersen, Member, IEEE, and Ivo Barbi, Fellow, IEEE

Abstract—In this paper, a ZVS-PWM three-phase current-fed push–pull dc–dc converter is proposed. When compared to single-phase topologies, the three-phase dc–dc conversion increases the power density, uses the magnetic core of the transformer more efficiently, reduces the stress on switches, and requires smaller filters since the frequency for its design is higher. The proposed converter employs an active clamping technique by connecting the primary side of the transformer to a three-phase full bridge of switches and a clamping capacitor. This circuit allows the energy from the leakage inductances to be reused, increasing the efficiency of the converter. If appropriate parameters are chosen, soft-commutation of the switches (ZVS) can also be achieved. The soft-commutation improves the efficiency even further, allows higher switching frequencies to be used, and reduces the electromagnetic interference significantly. Applications such as fuel cell systems, transportation, and uninterruptable power supplies are some examples that can benefit from the advantages presented by this converter. The theoretical analysis, a design example, and the experimental results for a prototype implementing this topology are presented. The prototype was designed to process 4 kW at full load with an input voltage of 120 V, an output voltage of 400 V, and a switching frequency of 40 kHz.

Index Terms—Active clamping, dc–dc power conversion, multi-phase, soft-commutation.

I. INTRODUCTION

THREE-PHASE systems are well known by their use in electric power generation transmission and distribution. The cost saving that they provide by employing less material than single-phase systems assured success in these areas and led to three-phase rectifiers, inverters, and also dc–dc converters.

Industrial environments have an increasing need for high-efficiency dc–dc converters. Applications including distributed generation and uninterruptable power supplies generally count on single-phase dc–dc converters with big and heavy transformers. The high volume associated with these converters makes them an expensive choice, and their use in the transportation area is sometimes impossible.

The introduction of high-frequency three-phase transformers on dc–dc converters brought the possibility of increasing power density, using the magnetic cores more efficiently and reducing the current stress on power switches. In addition, the increase in the high-frequency component seen by the filters allowed the use of much smaller inductors and capacitors [1].

After this, other three-phase dc–dc converter topologies were developed and compared [2], and techniques to increase the efficiency even more using soft-commutation [3]–[5] and reducing the number of semiconductors in the output rectifier bridge [6] were studied. Most studies conclude that the three-phase structures perform better than their single-phase counterparts [7]–[9].

However, depending on the topology, the voltage across the switches is not naturally clamped, requiring passive voltage clamps that dissipate energy stored in the leakage inductances [10]–[13] to prevent overvoltage. This energy loss reduces the efficiency of the converter. In order to avoid this problem, active clamping techniques have already been presented for single-phase converters and have successfully reused the energy that would be dissipated both in nonisolated [14] and isolated topologies [15]. To sum up, soft-commutation (ZVS) was also achieved with a correct parametric combination.

This paper proposes a three-phase current-fed push–pull dc–dc converter where the active clamping is performed, improving the topology presented in [12] and bringing the advantages of this technique to the three-phase dc–dc conversion. In this topology, a full three-phase bridge and a clamping capacitor on the primary side of the transformer are responsible for the active clamping without the need for an extra switch [16]. The switching losses can be significantly reduced, and electromagnetic interference is minimized as long as soft-commutation (ZVS) is achieved using appropriate parameters. As usual in three-phase topologies, the filters are designed for a frequency that is three times higher than the switching frequency, allowing size reduction.

In the future, the proposed converter could be applied as a high-efficiency alternative to many applications such as the energy processing of photovoltaic arrays and fuel cell systems [17]–[20] or automotive devices [21] and fuel cell powered vehicles [22], where the three-phase dc–dc conversion is already showing its benefits.

II. PROPOSED ZVS-PWM THREE-PHASE DC–DC CONVERTER

A. Circuit Description

The circuit of the proposed ZVS-PWM three-phase current-fed push–pull dc–dc converter is shown in Fig. 1. Switches $S_1$, $S_2$, and $S_3$ and the capacitor $C_g$ were added to the converter presented in [12] in order to achieve active clamping. Inductances

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The authors are with the Power Electronics Institute, Department of Electrical Engineering, Federal University of Santa Catarina, Florianópolis 88040-970, Brazil (e-mail: romero@inep.ufsc.br).

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ANDERSEN AND BARBI: ZVS-PWM THREE-PHASE CURRENT-FED PUSH–PULL DC–DC CONVERTER

Fig. 1. Circuit of the proposed ZVS-PWM three-phase current-fed push–pull dc–dc converter.

$L_{d1}$, $L_{d2}$, and $L_{d3}$ are responsible for maintaining the current during the commutation intervals. They represent the sum of the leakage inductance of the transformer and an external inductance, which is added to each phase if needed. The addition of capacitors $C_1$, $C'_1$, $C_2$, $C'_2$, $C_3$, and $C'_3$ and appropriate dead time between main and complementary gate signals provide the possibility to operate with soft-commutation.

B. Simplified Circuit

Despite the complete circuit being the one shown in Fig. 1, the analysis can be simplified, maintaining the same waveforms using the circuit of Fig. 2. This circuit, which will be used to describe the operation stages, represents the nonisolated equivalent version of the proposed converter with current source input and voltage source output. The transformer was substituted by a coupled three-phase reactor. Voltages and currents originally from the secondary side are referred to the primary side in this circuit. The time intervals related to the commutations will not be considered during the description of the operation stages due to being very short and interfering very little in the voltage gain. The commutation will be discussed separately in a later section.

C. Modulation

The gate signals are generated by the comparison of the modulating signal $V_M$ and three sawtooth carriers $120^\circ$ out of phase from each other. Fig. 3 shows the resulting gate signals. $V_{G1}$, $V_{G2}$, and $V_{G3}$ are the gate signals of $S_1$, $S_2$, and $S_3$, respectively, and $V'_{G1}$, $V'_{G2}$, and $V'_{G3}$ are the gate signals of switches $S'_1$, $S'_2$, and $S'_3$, respectively.

The proposed converter presents three different operation regions depending on the duty cycle $D$ according to Table I. The topology studied in this paper is capable of operating in the
three regions defined by Table I differently from the converter presented in [12] which could not operate in region R1 due to the absence of a demagnetizing path for the inductor. The converter proposed in this paper can transfer energy stored in the input inductor to the clamping capacitor if operation in region R1 is desired.

In this paper, this converter will be analyzed for operation in region R3. Operating in region R3 proves the principle of the active clamping in this topology for the worst case as, the higher the duty cycle is, the higher is the voltage across the switches. A good design for the other regions could achieve an even better result.

III. Principle of Operation and Voltage Gain

A. Operation in Region R3

Operating in region R3, the proposed converter has nine topological stages per switching period that can be described as follows.

Before the first stage, $S'_1$, $S_2$, and $S_3$ are already conducting.

1) First stage $(t_0, t_1)$—Starts when switch $S_1$ is turned on. Before this stage, $S'_1$ was conducting, and capacitor $C_g$ was delivering energy. Current $i_{Ld1}(t)$, initially negative and equal to $-I_L/3$, increases linearly through the intrinsic diode of $S_1$, as shown in Fig. 4(a), becoming positive and increasing its value though $S_1$ until reaching $I_L/3$, as shown in Fig. 4(b). Currents $i_{Ld2}(t)$ and $i_{Ld3}(t)$ decrease linearly from $2I_L/3$ to $I_L/3$ through switches $S_2$ and $S_3$, respectively. The load receives energy from the commutation inductances through diodes $D_1$, $D_5$, and $D_6$. The source does not transfer energy to the load during this stage.

2) Second stage $(t_1, t_2)$—Starts when currents $i_{Ld1}(t)$, $i_{Ld2}(t)$, and $i_{Ld3}(t)$ are equal to $I_L/3$. Currents $i_{Ld1}(t)$, $i_{Ld2}(t)$, and $i_{Ld3}(t)$ remain at $I_L/3$, and the diodes of the rectifier bridge remain off. This stage can be seen in Fig. 4(c). The source does not transfer energy to the load during this stage.

3) Third stage $(t_2, t_3)$—Starts when switch $S_2$ is turned off. Current $i_{Ld2}(t)$ decreases linearly from $I_L/3$ through the intrinsic diode of $S'_2$, as shown in Fig. 4(d), and then, it is equal to zero and starts to increase negatively, as shown in Fig. 4(e), until it reaches $-I_L/3$. In Fig. 4(d), the clamping capacitor $C_g$ receives energy from the commutation inductance, and in Fig. 4(e), the capacitor $C_g$ returns this energy. Currents $i_{Ld1}(t)$ and $i_{Ld3}(t)$ increase linearly from $I_L/3$ to $2I_L/3$ through switches $S_1$ and $S_3$, respectively. The load receives energy from the source through diodes $D_2$, $D_4$, and $D_6$.

The fourth and seventh topological stages are similar to the first stage, the fifth and eighth topological stages are similar to the second stage, and the sixth and ninth stages are similar to the third stage. The only difference is that other switches are on. After the ninth stage, the switching period is complete, and a new period starts with the first stage.

The main voltages of the circuit during the described stages are shown in Table II. The main theoretical waveforms for region R3 are shown in Fig. 5, whose time intervals are described by equations as presented in Table III. The waveforms shown in Fig. 5 and the voltages presented in Table II correspond to the symbols presented previously in Figs. 1 and 2.
TABLE II
MAIN VOLTAGES DURING EACH TOPOLOGICAL STAGE

<table>
<thead>
<tr>
<th>Voltage</th>
<th>1st Stage</th>
<th>2nd Stage</th>
<th>3rd Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>$v_{Ld}(t)$</td>
<td>$\frac{2}{3} \frac{V_i}{n}$</td>
<td>0</td>
<td>$\frac{1}{3} \frac{V_i}{n}$</td>
</tr>
<tr>
<td>$v_{Ld}(t)$</td>
<td>$-\frac{1}{3} \frac{V_o}{n}$</td>
<td>0</td>
<td>$\frac{2}{3} \frac{V_o}{n}$</td>
</tr>
<tr>
<td>$v_{Ld}(t)$</td>
<td>$-\frac{1}{3} \frac{V_o}{n}$</td>
<td>0</td>
<td>$\frac{1}{3} \frac{V_o}{n}$</td>
</tr>
<tr>
<td>$v_{Ld}(t)$</td>
<td>$\frac{2}{3} \frac{V_o}{n}$</td>
<td>0</td>
<td>$\frac{1}{3} \left( \frac{V_c}{n} - \frac{V_o}{n} \right)$</td>
</tr>
<tr>
<td>$v_{Ld}(t)$</td>
<td>$-\frac{1}{3} \frac{V_o}{n}$</td>
<td>0</td>
<td>$-\frac{2}{3} \left( \frac{V_c}{n} - \frac{V_o}{n} \right)$</td>
</tr>
<tr>
<td>$v_{Ld}(t)$</td>
<td>$-\frac{1}{3} \frac{V_o}{n}$</td>
<td>0</td>
<td>$\frac{1}{3} \left( \frac{V_c}{n} - \frac{V_o}{n} \right)$</td>
</tr>
<tr>
<td>$v_i(t)$</td>
<td>0</td>
<td>0</td>
<td>$\frac{V_c}{3}$</td>
</tr>
</tbody>
</table>

B. Voltage Gain

Equation (1) is the average current through the clamping capacitor $C_g$

$$\frac{3}{T_s} \int_0^{(1-D)T_s} \left( \frac{I_L}{3} + \frac{V_{Ld2}}{L_d} \cdot t \right) \cdot dt = 0. \quad (1)$$

Substituting $V_{Ld2}$ during the third stage from Table II in (1) and solving the integral yield

$$V_{Cg} - \frac{V_o}{n} = \frac{L_d \cdot f_s \cdot I_L}{1 - D}. \quad (2)$$

Considering the analysis that there are no losses in the converter, the following is valid

$$V_i \cdot I_L = V_o \cdot I_o. \quad (3)$$

Substituting $I_L$ from (3) in (2), the following is found

$$\frac{V_{Cg}}{V_o} = \frac{T_o}{1 - D} + \frac{1}{n} \quad (4)$$

where $T_o$ is given by

$$T_o = \frac{L_d \cdot f_s \cdot I_o}{V_i}. \quad (5)$$

As the average voltage across the inductors is zero, the average voltage across the switches $S_1$, $S_2$, and $S_3$ is the input voltage $V_i$, and the following can be written

$$V_i = (1 - D) \cdot V_{Cg}. \quad (6)$$

Equation (6) leads to the input–clamping capacitor voltage gain shown in

$$\frac{V_{Cg}}{V_i} = \frac{1}{1 - D}. \quad (7)$$

Fig. 5. Main theoretical waveforms for region R3.

TABLE III
EQUATIONS FOR TIME INTERVALS OF FIG. 5

<table>
<thead>
<tr>
<th>Stage</th>
<th>$\Delta t_1 = \frac{n \cdot I_{Ld} \cdot I_i}{V_o}$</th>
<th>$\Delta t_2 = \frac{L_d}{3}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>First stage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Second stage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Third stage</td>
<td>$\Delta t_3 = (1 - D) \cdot T_s$</td>
<td></td>
</tr>
</tbody>
</table>

Substituting (4) in (7) leads to the input–output voltage gain

$$q = \frac{V_o}{V_i} = \frac{n}{(1 - D) + n \cdot T_o}. \quad (8)$$
Equation (8) represents the voltage gain of the proposed three-phase current-fed push–pull dc–dc converter with active clamping in region R3. Equation (8) was used to plot the curves of the output characteristic of the converter shown in Fig. 6. The output characteristic shows the voltage gain divided by the turns ratio $q/n$ versus normalized output current multiplied by the turns ratio $n \cdot I_o$ for different duty cycles of region R3. As expected, the voltage gain is not only dependent on duty cycle, even in continuous conduction mode (CCM); there is also a voltage drop caused by the inductances $L_{d1}$, $L_{d2}$, and $L_{d3}$, which increases with the output current. Fig. 6 is plotted only for region R3 and considering CCM as the input current is considered free of ripple in the analysis. The theoretical curves show a good agreement with the simulated points obtained by numerical simulation of the circuit.

### IV. Commutation Analysis

The topological stages reveal that both the turning on and turning off of a switch in region R3 present a current module of $I_L/3$ available to perform the commutation. Immediately after switch $S_1'$ is turned off, Fig. 7 shows the situation during the dead time where capacitor $C_1'$ is charging and capacitor $C_1$ is discharging. After the complete discharge of $C_1$, the intrinsic diode of $S_1$ will start to conduct, and switch $S_1$ can be turned on under ZVS condition.

Voltage on capacitor $C_1$ and $C_1'$ can be expressed as

$$v_{C1}(t) + v_{C1}'(t) = V_{Cg}. \quad (9)$$

Deriving (9) and considering $C_1 = C_1' = C$ lead to

$$C \cdot \frac{dv_{C1}(t)}{dt} + C \cdot \frac{dv_{C1}'(t)}{dt} = 0. \quad (10)$$

Based on Fig. 7 and the equations presented, the following is obtained

$$|i_{c1}| = |i_{c1}'| = \frac{I_L}{6}. \quad (11)$$

If the input current $I_L$, the clamping voltage $V_{Cg}$, and the maximum commutation interval $\Delta t$ are known, the maximum commutation capacitance $C$ is given by

$$C = \frac{I_L \cdot \Delta t}{6 \cdot V_{Cg}}. \quad (12)$$

The capacitance $C$ is the sum of the intrinsic output capacitance of the switch $C_{oss}$ and the externally connected capacitance $C_{ext}$.

ZVS operation is intrinsic to this topology. It is the result of the topology, the modulation, and the parameters. If external capacitors and external inductors are not added, in some condition, the converter can still achieve soft-commutation because of the intrinsic capacitance of the switch and the leakage inductances of the transformer. The addition of external capacitors and inductors is done to guarantee a range of ZVS operation (e.g., from 40% to 100% load).

### V. Design Example

#### A. Specifications

In order to simulate the converter and to build a prototype, some specifications were defined as follows:

- $P_o = 4$ kW (output power);
- $V_i = 120$ V (input voltage);
- $V_o = 400$ V (output voltage);
\( f_s = 40 \text{ kHz} \) (switching frequency);
\( \eta = 93\% \) (expected efficiency);
\( \Delta I_L = 0.08 I_L \) (input current ripple).

### B. Clamping Voltage and Duty Cycle

The duty cycle was chosen to guarantee operation in region R3 and to generate an acceptable clamping voltage. Choosing a clamping voltage of 450 V, the duty cycle is calculated as follows:

\[
D = 1 - \frac{V_i}{V_{Cg}} = 1 - \frac{120}{450} = 0.733. \tag{13}
\]

### C. Turns Ratio of the Transformer, Effective Duty Cycle, and Commutation Inductance

The turns ratio of the transformer is calculated to achieve the desired output voltage considering the effective duty cycle reduction \( n \cdot T_o \). If an effective duty cycle reduction of 5\% is chosen, the turns ratio of the transformer is calculated as follows:

\[
n = \frac{V_o}{V_i} \cdot (1 - D + n \cdot T_o) = \frac{400}{120} \cdot (1 - 0.733 + 0.05) = 1.06. \tag{14}
\]

The turns ratio \( n \) was defined as the number of turns of the secondary winding divided by the number of turns of the primary winding.

After this, the commutation inductance is calculated as

\[
L_d = \frac{n \cdot T_o \cdot V_i}{f_s \cdot n \cdot I_o} = \frac{0.05 \cdot 120}{40 \times 10^3 \cdot 1.06 \cdot 10} = 14.15 \mu H. \tag{15}
\]

Finally, in the laboratory, a 15-\( \mu H \) commutation inductance was used, resulting in an effective duty cycle reduction of 5.3\% \((n \cdot T_o)\), which is still acceptable, allowing these values to be maintained.

### D. Duration of Operation Stages

The duration of the operation stages can be calculated as

\[
\Delta t_1 = \frac{n \cdot L_o \cdot I_o}{V_i} = \frac{1.06 \cdot 15 \times 10^{-6} \cdot 10}{120} = 1.325 \mu s \tag{16}
\]

\[
\Delta t_2 = (1 - D) \cdot T_s = (1 - 0.733) \cdot 25 \times 10^{-6} = 6.675 \mu s \tag{17}
\]

\[
\Delta t_3 = \frac{T_s}{3} - \Delta t_1 - \Delta t_2 = \left( \frac{25}{3} - 1.325 - 6.675 \right)\mu s = 333.3 \text{ ns.} \tag{18}
\]

### E. Boost Inductance

Operating in region R3, the boost inductance can be calculated as

\[
L = \frac{V_i}{\Delta I_L \cdot f_s} \left( D - \frac{2}{3} \right) = \frac{120 \cdot (0.733 - 2/3)}{0.08 \cdot 4 \cdot 10^9 / 0.33 \cdot 120 \cdot 40 \times 10^3} \approx 70 \mu H. \tag{19}
\]

### F. Peak Output Current

The peak current \( I_{o \text{ max}} \) of Fig. 5 is calculated as

\[
I_{o \text{ max}} = \frac{2/3 \cdot I_o}{(1 - D) + n \cdot T_o} = \frac{2/3 \cdot 10}{(1 - 0.733) + 0.05} = 21.03 \text{ A.} \tag{20}
\]

### G. RMS Value of the Current Through the Output Capacitor

The output capacitor can be chosen by the rms value of the current through it \( I_{\text{Coff}} \), which is calculated by

\[
I_{\text{Coff}} = I_o \sqrt{\frac{4/9}{(1 - D) + n \cdot T_o} - 1} = 10 \sqrt{\frac{4/9}{0.317} - 1} = 6.34 \text{ A.} \tag{21}
\]

Four capacitors of 1000 \( \mu F/250 \) V, a pair in series connected in parallel with the other pair in series, were used to fulfill the voltage and current requirements.

### H. External Commutation Capacitance

Considering a maximum commutation interval (dead time) of 1 \( \mu s \) and expecting ZVS from 40\% to 100\% load range, the maximum external commutation capacitance to be connected in parallel with each MOSFET (SPW47N60C3) that allows complete discharge was calculated as

\[
C_{\text{ext}} \leq \frac{0.4 I_L \cdot \Delta t}{V_{Cg}} - C_{\text{cos}} = \frac{0.4 \cdot 35.8 \cdot 1 \times 10^{-6}}{6 \cdot 450} - 2.2 \text{ nF} = 3.1 \text{ nF.} \tag{22}
\]

After simulation and laboratory tests, good results were obtained with external capacitors of 2.2 nF, which were chosen for the prototype.

If the signals are generated appropriately, the switches are turned on during the conduction interval of its intrinsic diode, so the turn on is naturally ZVS.

However, during the turn off, the commutation capacitance has to ensure that the voltage across the switch increases slowly so that the current is already in a reduced value near to zero.

Fig. 8 shows a simulation result for the rated power where switch \( S_1 \) is turning off. This simulation used the parameters calculated in this design example and the model of the MOSFET provided by the manufacturer. As expected, the voltage across the switch rises slowly, and most of the current is deviated to the external commutation capacitor. The current through the switch is very low during the rise of the voltage, resulting in low commutation loss. Soft-commutation was achieved from approximately 50\%–100\% load in simulation.

### VI. Prototype Implementation and Experimental Results

#### A. Prototype Description

A prototype implementing the proposed converter was built in order to validate the analysis. The main specifications and components used are shown in Table IV. A photograph of the prototype can be seen in Fig. 9.
TABLE IV
MAIN SPECIFICATIONS AND COMPONENTS OF THE PROTOTYPE

<table>
<thead>
<tr>
<th>Description</th>
<th>Quantity</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Power (P_o)</td>
<td>-</td>
<td>4 kW</td>
</tr>
<tr>
<td>Input Voltage (V_i)</td>
<td>-</td>
<td>120 V</td>
</tr>
<tr>
<td>Output Voltage (V_o)</td>
<td>-</td>
<td>400 V</td>
</tr>
<tr>
<td>Switching Frequency (f_s)</td>
<td>-</td>
<td>40 kHz</td>
</tr>
<tr>
<td>High-Frequency Three-Phase Transformer (T)</td>
<td>1</td>
<td>N/N_s=37/32</td>
</tr>
<tr>
<td>Input Inductor (L)</td>
<td>1</td>
<td>70 μH</td>
</tr>
<tr>
<td>Electrolytic Output Capacitors (C)</td>
<td>4</td>
<td>1000 μF / 250 V (electrolytic)</td>
</tr>
<tr>
<td>Polypropylene Output Capacitor</td>
<td>1</td>
<td>1 μF / 630 V (polypropylene)</td>
</tr>
<tr>
<td>Clamping Capacitors (C_C)</td>
<td>3</td>
<td>1.5 μF / 1 kV (polypropylene)</td>
</tr>
<tr>
<td>External Commutation Capacitors</td>
<td>6</td>
<td>2.2 nF (polypropylene)</td>
</tr>
<tr>
<td>MOSFETs</td>
<td>6</td>
<td>SPW47N60C3</td>
</tr>
<tr>
<td>Rectifier Diodes (D_1 – D_3)</td>
<td>6</td>
<td>MUR860</td>
</tr>
</tbody>
</table>

![Fig. 9. Photograph of the laboratory prototype.](image)

Three small inductors were externally added to each phase of the transformer to achieve the total commutation inductance of 15 μH.

On the primary side of the transformer, six MOSFETs CoolMOS SPW47N60C3 were used due to their fast switching characteristics and low resistance when turned on. The gate signals were generated by three PIC18F1330 microcontrollers, and the connection to the power switches was made using three MOSFET drivers SKHI 20opA by Semikron, one for each leg.

A dead time duration of 1 μs between the gate signals of the switches of the same leg was introduced by the drivers.

![Fig. 10. Input voltage and input current.](image)

![Fig. 11. Output voltage and output current.](image)

B. Experimental Results

Relevant waveforms were acquired when the converter was operating at its rated power of 4 kW. Fig. 10 shows the input voltage and input current. The input voltage is 120 V, and a very low ripple is presented by the input current as specified in the design example. The output voltage and output current shown in Fig. 11 are also at rated values of 400 V and 10 A, respectively.

The voltage and current in the primary winding \(L_{p1}\) and secondary winding \(L_{s1}\) are shown in Figs. 12 and 13, respectively. In both windings, the average voltage is zero as expected. The average current is zero only for the secondary winding \(L_{s1}\). On the primary side, there is a dc component which is one-third of the average input current of the converter in this topology.

On the primary side, the waveforms of the voltages across the MOSFETs are very similar to the theoretical analysis. These waveforms can be seen in Figs. 14 and 15 for complementary switches of the same leg. In addition to the voltages, the
$L_{p1}$ current is also presented in both figures. Active clamping and soft-commutation contribute to waveforms without voltage overshoot and smoothed switching slopes. The voltage is clamped at 450 V for both switches as designed.

The details of the commutation were not obtained experimentally because the measurement of the current through the switch would introduce a series inductance and would degrade the commutation. However, it can be noted that switch $S_1$ is turned on (its voltage become zero) during the negative part of $L_{p1}$ current, which is while the intrinsic diode is in conduction, and then, ZVS turn on occurs. As for the turn off, the voltage does not increase very rapidly as a result of the charge of the commutation capacitance. Overvoltage is also not present. This waveform also indicates soft-commutation during the turn off.

On the secondary side, the voltages and currents in the diodes are also as expected from the design. Figs. 16 and 17 show the voltage across $D_1$ and $D_4$, respectively, along with the current in $L_{s1}$. These voltages are naturally clamped at the output voltage of 400 V.
suitable applications include distributed generation, uninterruptable power supplies, and transportation.

**REFERENCES**


Romero Leandro Andersen (M’11) was born in Florianópolis, Santa Catarina, Brazil, in 1980. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 2003, 2006, and 2010, respectively.

He is currently a Postdoctoral Researcher with the Power Electronics Institute, Federal University of Santa Catarina. His interests include dc–dc power conversion, power converter modeling, and renewable energy sources.

Ivo Barbi (M’78–SM’90–F’11) was born in Gaspar, Santa Catarina, Brazil, in 1949. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina, Florianopolis, Brazil, in 1973 and 1976, respectively, and the Dr.Ing. degree from the Institut National Polytechnique de Toulouse, Toulouse, France, in 1979.

He founded the Brazilian Power Electronics Society and the Power Electronics Institute, Federal University of Santa Catarina, where he is currently a Professor.