IET Power Electronics

Research Article

IET Journals
The Institution of Engineering and Technology

Split-phase switched-capacitor ac–ac converter

ISSN 1755-4535
Received on 28th August 2014
Accepted on 13th December 2014
doi: 10.1049/iet-pel.2014.0686
www.ietdl.org

Telles Brunelli Lazzarin ✉, *Marcos Paulo Moccelini*, *Ivo Barbi*

Department of Electrical Engineering, Federal University of Santa Catarina, Florianópolis, Brazil
✉ *E-mail: telles@inep.ufsc.br*

Abstract: This study proposes an ac–ac direct static power converter based on the switched-capacitor (SC) principle, aimed at supplying a split-phase system from an ac single-phase voltage source. The main advantages of the proposed split-phase SC converter are (i) the provision of three output voltages, two being equal to the input voltage and one being twice the input voltage, (ii) balanced output voltages even under unbalanced loads, (iii) the absence of magnetic elements in the power circuit, (iv) the stress voltages in all components being equal to the input voltage, (v) the ability to be bidirectional, (vi) high efficiency and (vii) high power density. These characteristics make the proposed converter suitable for modern applications where a split-phase system needs to be generated from a renewable energy source, distributed generation system, uninterruptible power supply (UPS), battery bank, electric/hybrid vehicle, smart grid or even the electrical grid itself. To verify the performance of the proposed converter, a 1 kW prototype was built and tested with standard voltages, such as 110 V input voltage and 110 V/110 V/220 V output voltages. The efficiency, output voltage regulation, tests with input voltages of 16.6, 60 and 400 Hz and other experimental results are reported herein.

1 Introduction

A split-phase system is a 3-wire single-phase distribution system that can supply three single-phase voltages, which are provided by the series-connection of two sources. Conventionally, a split-phase system is generated by transformers with two secondary windings (or autotransformers), as demonstrated in Fig. 1. In most cases, the common central point is connected to the ground. This system is the ac equivalent of the original Edison 3-wire direct current system. Split-phase systems are used in North America for residential and light commercial applications (120 V/240 V), in Europe to feed farms and small groups of houses (230/460 V) and in the United Kingdom for electrical tools and portable lighting at, for instance, construction sites (55–110 V) [1–6]. An advantage of this system is that lighting and small loads are connected from the ends to a neutral wire (v_{o1} and v_{o2} in Fig. 1) and large appliances are connected across the two-end conductors, and thus operate with double the voltage (v_{o3} in Fig. 1). The split-phase system is also employed to feed the trains in railway power-supply systems, where the electrification system works at voltages as high as 15 kV–16.66 Hz (as exemplified in [7]).

Recently, the number of renewable energy sources, distributed generation systems, UPS systems, energy storage in batteries, electric and hybrid vehicles and smart grids has been increasing [8], and these systems employ power converters. Therefore, when they need to be connected to a split-phase system, the conversion from single- or three-phase to a split-phase can be carried out by one static power converter.

Static converters based on the switched-capacitor (SC) have been an important research topic for many years. Currently, the number of topologies that use this principle is growing and the SC has been employed in low and high power dc–dc converters [9–13], resonant SC dc–dc converters [14–17], charge balancing circuits for batteries [18] and hybrid converters as rectifiers [19], inverters [20, 21], multilevel converters [22, 23], unidirectional dc–dc converters [24–26], bidirectional dc–dc converters [27] and indirect ac–ac converters [28, 29]. Interesting studies on models, dynamics, efficiency and design of SC converters are presented in [30–36]. Recently, the SC principle has also been used in direct single- and three-phase ac–ac power converters [37–40], which opened up a new field for SC converters. SC power converters (SCPCs) can achieve a significant size reduction and increased efficiency in relation to the conventional converters. Furthermore, SCPC can operate in open-loop, they can be either unidirectional or bidirectional and their operation principles are simple.

The aim of this paper is to introduce a direct ac–ac SCPC that generates a split-phase system from an ac single-phase voltage source. The proposed direct ac–ac converter employs only capacitors and switches in the power circuit. It is bidirectional, the output voltage follows the waveform of the input voltage, the generation of the gate drive signals is simple and it works in open-loop. The proposed topology is suitable for application in houses, farms, commercial properties and devices where a split-phase system must be generated from a single-phase ac voltage source. A detailed analysis of the proposed converter, equivalent circuits, design methodology and relevant experimental results are reported herein.

2 Proposed split-phase SC ac–ac converter

2.1 Proposed converter

The proposed direct ac–ac converter based on an SC that produces a split-phase system is presented in Fig. 2*a*. The circuit is composed of four bidirectional switches and three capacitors represented by S_1, S_2, S_3, S_4, C_1, C_2 and C_S. Bidirectional switches have to be used because the converter operates with alternate current. The practical implementation of a bidirectional switch employs two conventional metal–oxide semiconductor field effect transistor (MOSFET), as shown in Fig. 2*b*. This study uses a model for the bidirectional switch, which can also be seen in Fig. 2*b*.

The principle of the converter operation consists of two main stages: one when the capacitor C_s (switching capacitor) is parallel-connected to the capacitor C_1 (S_1 and S_3 ON) and another when C_s is parallel-connected to C_3 (S_2 and S_4 ON). The SC C_s transfers its voltage to C_1 and C_2 and ensures voltage balance in the capacitors even with unbalanced loads. An SCPC can operate in three modes, which are defined by the charge and discharge of the SC as follows: complete charge (CC), partial charge (PC) and no charge (NC) [41]. The best operation regions are in the PC and

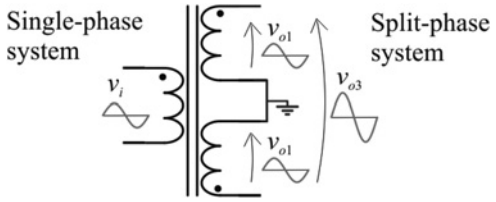

Fig. 1 *Typical split-phase system*

NC modes and the waveforms described in this section, in the operation stages, relate to the converter operating in PC mode.

The converter operates with a fixed duty cycle of close to 0.5 (typical in an SC) and in open-loop. A dead time must be implemented since the switches are series-connected (as a leg). The converter uses gate drive signals, as shown in Fig. 2*c*. Hence, when an ac–ac input voltage is connected at points 'a' and 'b', as shown in Fig. 2*a*, its value is copied to v_{o1} (voltage between points 'c' and 'd') and v_{o2} (voltage between points and 'd' and 'e'), and thus v_{o3} (voltage between points 'c' and 'e') can be obtained through the sum of v_{o1} and v_{o2}, as illustrated in Fig. 2*a*.

The SC keeps the appropriate output voltages under both balanced and unbalanced loads and the voltage stresses across the capacitors and bidirectional switches are equal to the voltage v_i. The main theoretical waveforms in one period of v_i are illustrated in Figs. 3*a*–*c*.

The ground point is not shown in Fig. 2*a*; however, it can be connected to point 'd' making the converter outputs similar to those of a typical split-phase system (as illustrated in Fig. 1). Alternatively, the ground point can be connected to point 'e' or 'c' or not connected to any point. In all of these cases, the converter will function properly since the ground point does not modify the converter operation and, in many applications, the proposed converter can be used without it.

2.2 Topological stages

The proposed converter presents two main topological stages and two caused by the dead time, as shown in Fig. 4. The theoretical waveforms of each stage for the positive half of v_i are also shown in Fig. 4, considering the SC operating in PC mode. The waveforms for the negative half are similar; however, the voltage polarities and current flows must be inverted.

First stage: This stage starts when switches S_1 and S_3 are turned ON and the capacitors C_S and C_1 are parallel-connected. The capacitor C_1 charges with the i_{C_1} current supplied by C_s and v_i. The current i_{C_1} is limited by resistances R_{on} from S_1 and S_3 and the circuit presents first-order behaviour (RC circuit). The C_2 capacitor discharges on R_{o2} and R_{o3} and thus its current i_{C_2} is constant. Switch currents i_{S_1} and i_{S_3} are defined by capacitors and load currents, and therefore they present a constant and an exponential component. The voltage across C_1 (v_{C_1}) increases and the voltages across C_2 and C_s (v_{C_2} and v_{C_S}) decrease. Switches S_1 and S_3 are turned OFF at the end of the first stage. This topological stage and its main waveforms are shown in Fig. 4*a*.

Second stage: This stage starts when switches S_2 and S_4 are turned ON and it is similar to the first stage. C_S and C_2 are parallel-connected, C_2 charges with the i_{C_2} current supplied by C_s and v_i. The current i_{C_2} also presents first-order behaviour. C_2 discharges on R_{o1} and R_{o3}, and thus its current i_{C_1} is constant. Currents i_{S_2} and i_{S_4} are also defined by capacitors and load currents, and therefore they present a constant and an exponential component. The voltage v_{C_2} increases and the voltages v_{C_1} and v_{C_S} decrease. Switches S_2 and S_4 are turned OFF at the end of the third stage. This topological stage and its main waveforms can be seen in Fig. 4*c*.

Converter during the dead time: These periods are defined during the dead time (t_m) and they happen twice in one switching period. There is no connection from the C_S capacitor to the output capacitors C_1 and C_2 during t_m. Therefore C_S charges with the i_i current supplied by v_i and its voltage increases. The loads R_{o1}, R_{o2} and R_{o3} are fed by capacitors C_1 and C_2, and thus their currents are constant and their voltages decrease. The main waveforms during the dead time are illustrated in Fig. 4*b*.

3 Quantitative analysis

3.1 Ideal static voltage gain

The sinusoidal input voltage (v_i) is reproduced across the capacitors C_1 and C_2, as indicated in Fig. 3*a*. Therefore the output voltages of the proposed converter are composed of $v_{o1} = v_{C_1}$, $v_{o2} = v_{C_2}$ and $v_{o3} = v_{C_1} + v_{C_2}$. Hence, the ideal voltage gains are defined by

$$g_{v1} = \frac{v_{o1}}{v_i} = \frac{v_i}{v_i} = 1 \tag{1}$$

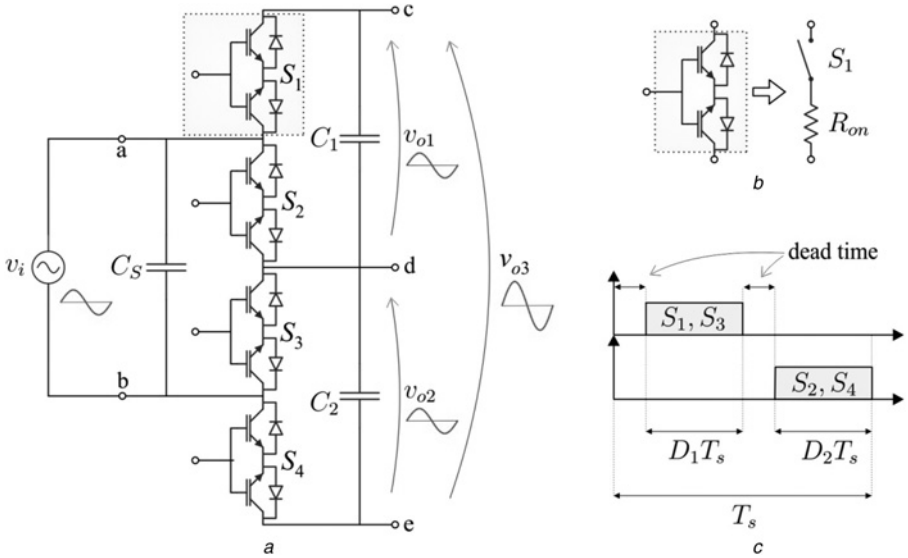

Fig. 2 *Direct ac–ac converter*

a Proposed split-phase SC ac–ac converter
b Practical implementation of bidirectional switches employing two conventional MOSFET and their model
c Gate drive signals considering the dead time

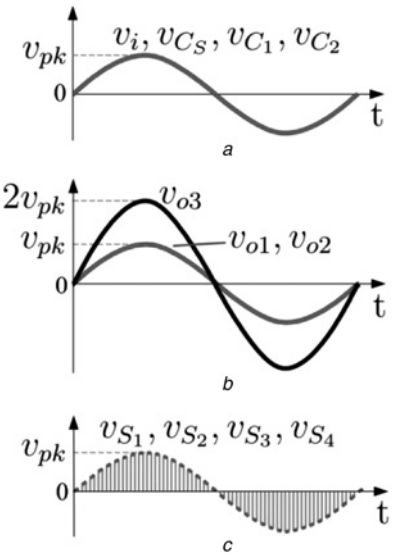

Fig. 3 *Theoretical waveforms*

a Voltages from the input source and across the capacitors
b Output voltages
c Voltage across the switches

$$g_{v2} = \frac{v_{o2}}{v_i} = \frac{v_i}{v_i} = 1 \tag{2}$$

$$g_{v3} = \frac{v_{o3}}{v_i} = \frac{v_i + v_i}{v_i} = 2 \tag{3}$$

3.2 Voltage stress across the capacitors and the MOSFET

The topological stages in Fig. 4, one of which is reproduced in Fig. 5*a*, demonstrate that the v_i voltage is applied across all components. Details of voltages across the capacitors and the MOSFETs are illustrated in Figs. 5*a* and *b*. Thus, the maximum voltage stress across the components is the peak value of v_i, with v_i being defined as

$$v_i = V_{i,\text{pk}} \sin(\omega t) \tag{4}$$

and thus

$$V_{C,\max} = V_{S,\max} = V_{i,\text{pk}} \tag{5}$$

3.3 Current stress in the capacitors

The highest current stresses are those of capacitors C_1 and C_2. The waveform of their currents can be analysed in Fig. 5*c*, where 'x' is the element '1' or '2', $i_{\text{LOAD}x}$ is $i_{ox} + i_{o3}$, T_s is the switching period and D is the duty cycle.

The waveform analysis in Fig. 5*c* allows the average value of i_{Cx} in one switching period to be written as

$$\langle i_{Cx} \rangle = \frac{i_{Cx,\max} D_x T_\text{s} - i_{\text{LOAD}x}(1 - D_x) T_\text{s}}{T_\text{s}} \tag{6}$$

where $i_{Cx,\max}$ is considered as the average value of i_{Cx} in $D_x T_\text{s}$. This is possible if the SC operates in PC or NC. Thus, $i_{Cx,\max}$ can be written as

$$i_{Cx,\max} = \frac{\langle i_{Cx} \rangle D_x T_\text{s} - i_{\text{LOAD}x}(1 - D_x)}{D_x} \tag{7}$$

The root mean square (rms) value of i_{Cx} in one switching period (T_S) can be written as

$$\langle i_{Cx,\text{rms}} \rangle_{T_\text{s}} = \sqrt{\frac{1}{T_\text{s}} \int_0^{T_\text{s}} i_{Cx}^2 \, \text{d}t} \tag{8}$$

Defining i_{Cx} and solving the integration gives

$$\langle i_{Cx,\text{rms}} \rangle_{T_\text{s}} = \sqrt{\left[i_{Cx,\max}^2 D_x - i_{\text{LOAD}x}^2 (1 - D_x)_\text{s} \right]} \tag{9}$$

The rms value of i_{Cx} in one period of v_i (ac input voltage) can be represented by

$$I_{Cx,\text{rms}} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} \langle i_{Cx,\text{rms}} \rangle_{T_\text{s}}^2 \, \text{d}\omega t} \tag{10}$$

Replacing (7) in (9) and the result in (10), $I_{Cx,\text{rms}}$ is dependent on $\langle i_{Cx} \rangle$ and $i_{\text{LOAD}x}$. The circuit analysis allows these currents to be defined as

$$\langle i_{Cx} \rangle = V_{i,\text{pk}} \cos(\omega t) \omega C_x \tag{11}$$

and

$$i_{\text{LOAD}x} = V_{i,\text{pk}} \sin(\omega t) G_{\text{LOAD}x} \tag{12}$$

where $G_{\text{LOAD}x}$ is the conductance 'seen' by the output 'x' (1 or 2) and is given by

$$G_{\text{LOAD}x} = \frac{1}{R_\text{ox}} + \frac{2}{R_{o3}} \tag{13}$$

The definitions of (12) and (13) are also applied in (10), and thus the integral is solved. Therefore the value of $I_{Cx,\text{rms}}$ is given by

$$I_{Cx,\text{rms}} = V_{i,\text{pk}} \sqrt{\frac{\omega^2 C_x^2 + G_{\text{LOAD}x}^2 (1 - D_x)}{2 D_x}} \tag{14}$$

which provides the rms value of i_{Cx} in one period of v_i.

The SC capacitor C_S is parallel-connected with the input voltage source, and thus its rms current is given by

$$I_{\text{CS},\text{rms}} = V_{i,\text{rms}} \omega C_\text{S} \tag{15}$$

3.4 Current stress in the MOSFET

The waveform of the MOSFET current is shown in Fig. 5*d*. Its analysis allows it to define that

$$i_{Sx,\max} = i_{Cx,\max} + i_{\text{LOAD}x} \tag{16}$$

The rms value of i_{Sx} in T_S can be written as

$$\langle i_{Sx,\text{rms}} \rangle_{T_\text{s}} = \sqrt{\frac{1}{T_\text{s}} \int_0^{T_\text{s}} i_{Sx}^2 \, \text{d}t} \tag{17}$$

Defining i_{Sx} and solving the integration, $\langle i_{Sx,\text{rms}} \rangle_{T_\text{s}}$ is given by

$$\langle i_{Sx,\text{rms}} \rangle_{T_\text{s}} = \sqrt{\left(i_{Cx,\max} + i_{\text{LOAD}x} \right)^2 D_x} \tag{18}$$

IET Power Electron., 2015, Vol. 8, Iss. 6, pp. 918–928

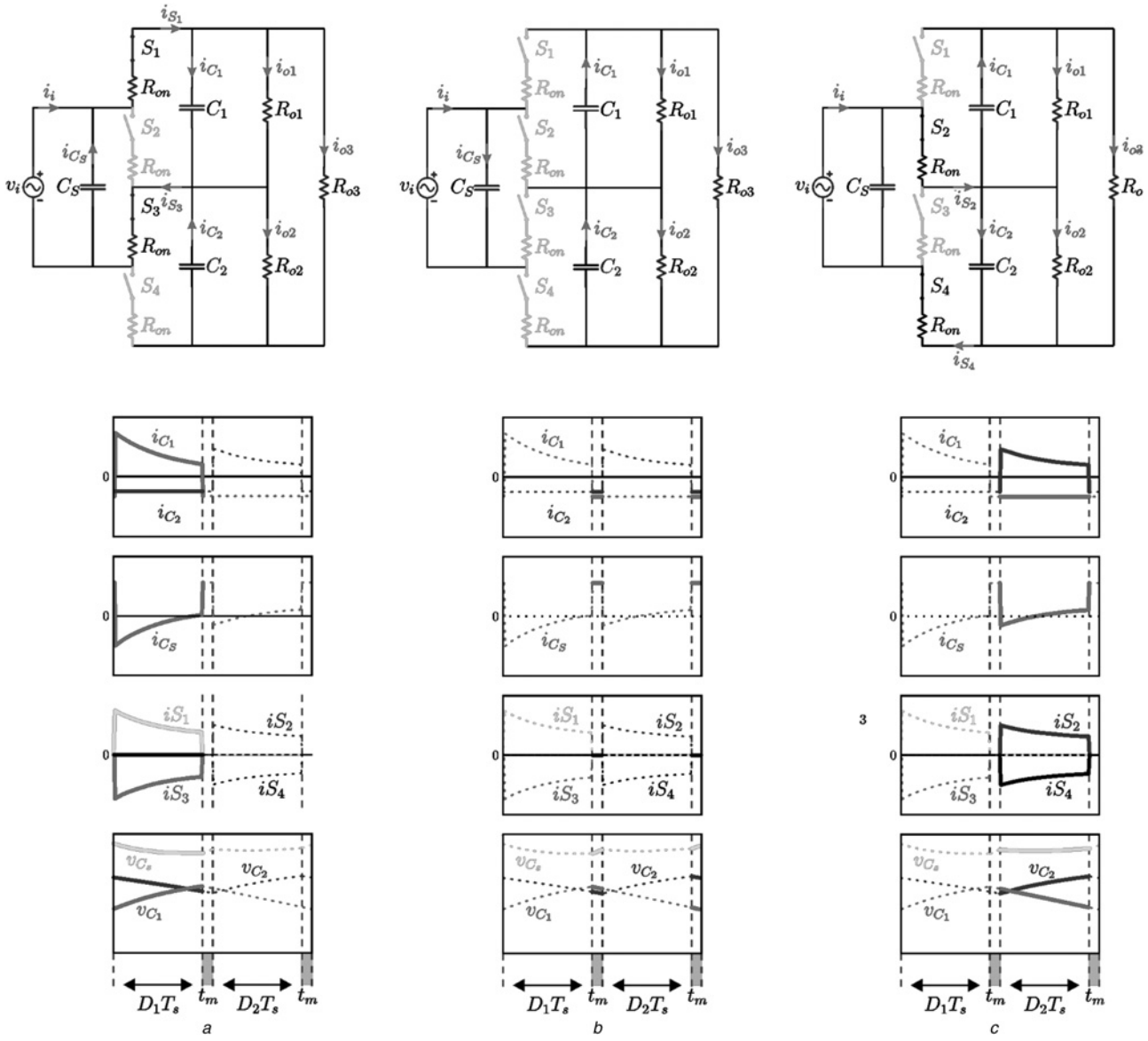

Fig. 4 *Topological stages and theoretical waveforms at high frequency for the positive half-cycle of the input voltage*

a First stage and its main waveforms
b Converter during the dead time its main waveforms
c Second stage its main waveforms

The rms value of i_{Sx} in one period of v_i is obtained from

$$I_{Sx,\,\mathrm{rms}} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} \langle i_{Sx,\,\mathrm{rms}}\rangle_{T_s}^2 \, \mathrm{d}\omega t} \tag{19}$$

On substituting (7), (11), (12) and (18) in (19) and solving the integration, the value of $I_{Sx,\mathrm{rms}}$ is given by

$$I_{Sx,\,\mathrm{rms}} = v_{\mathrm{p}}\sqrt{\frac{\omega^2 C_x^2 + G_{\mathrm{LOAD}\,x}^2}{2D_x}} \tag{20}$$

Expressions (14) and (20) are approximate values because of the definition of $i_{Cx,\mathrm{max}}$; however, their errors are small when the SC operates in PC or NC modes. These expressions also demonstrate that the rms values of the currents in the capacitors and in the MOSFET are dependent on the duty cycle and for this reason a D value close to 0.5 (maximum value) and a short dead time are used.

3.5 Equivalent circuit

The proposed converter, shown in Fig. 2, can be represented through the equivalent circuit seen in Fig. 6, which does not consider the variables provided by the commutation frequency. The equivalent circuit allows a simple and fast analysis of the converter variables of low frequency (input voltage frequency) to be carried out.

The elements from the equivalent circuit are:

- R_{p}: parallel resistances that represent the switching loss because of the intrinsic capacitance of the MOSFET;
- R_s: series resistances which indicate the conduction loss in the switches and capacitors;
- C_{eqi}, $C_{\mathrm{eqo},x}$: parallel capacitances which define the reactive power flow required by the converter; and
- R_{o1}, R_{o2} and R_{o3}: resistances which indicate the loads connected to the converter.

These elements are calculated as presented in [38] and the main equations are described as follows.

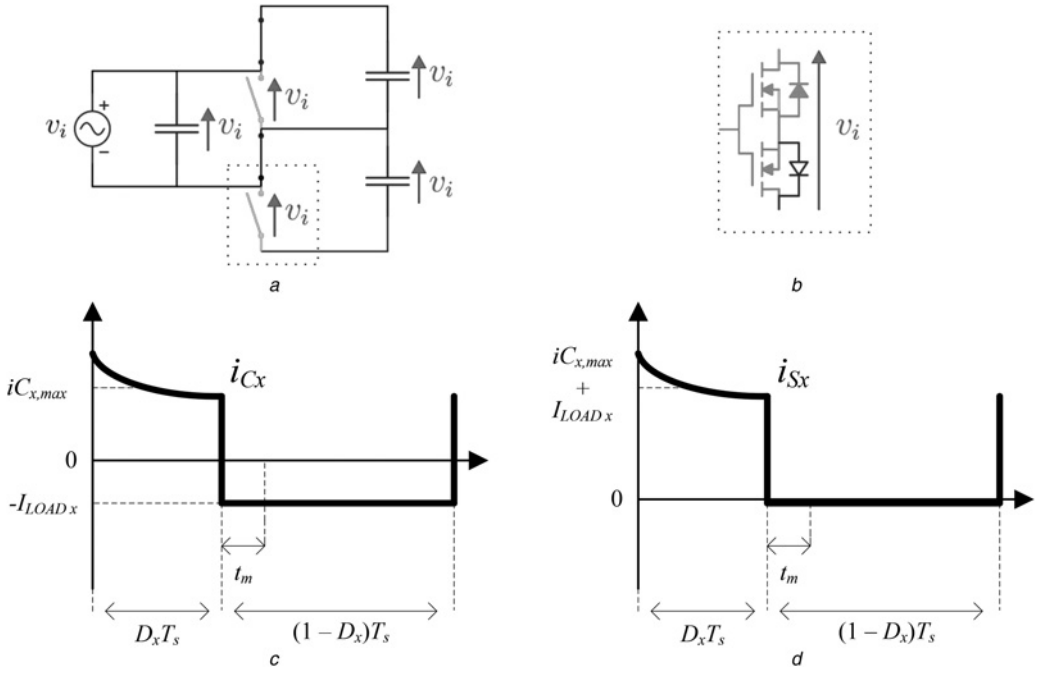

Fig. 5 *Analysis of the proposed converter*

a Voltage stress across the capacitors
b Voltage stress across the MOSFET
c Waveform of the SC current in one switching period
d Waveform of the MOSFET current in one switching period

The series resistances are defined by

$$R_{\mathrm{s}} = \frac{1}{2f_{\mathrm{s}}\tau} \cdot \frac{\left(1 - \mathrm{e}^{-1/f_{\mathrm{s}}\tau}\right)}{\left[1 - \left(\mathrm{e}^{-D_1/f_{\mathrm{s}}\tau} + \mathrm{e}^{-D_2/f_{\mathrm{s}}\tau}\right) + \mathrm{e}^{-1/f_{\mathrm{s}}\tau}\right]} \tag{21}$$

and the parallel resistances are given by

$$R_{\mathrm{p}} = \frac{1}{2C_{\mathrm{OSS}}f_{\mathrm{s}}} \tag{22}$$

τ is given by

$$\tau = 2R_{\mathrm{on}}C_{\mathrm{S}} \tag{23}$$

and R_{on} by

$$R_{\mathrm{on}} = 2R_{\mathrm{DS(on)}} \tag{24}$$

where $R_{\mathrm{DS(on)}}$ is the static drain–source on-resistance of a MOSFET; C_{OSS} is the output capacitance of a MOSFET and; and f_{s} is the switching frequency.

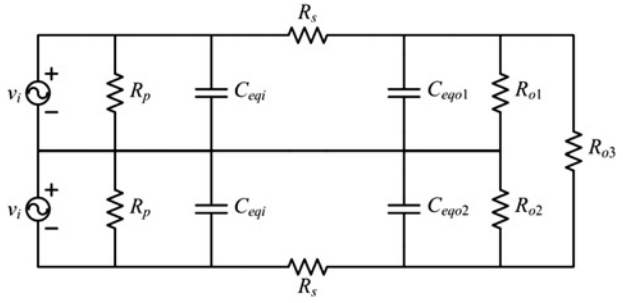

Fig. 6 *Equivalent circuit of split-phase SC ac–ac converter 'seen' by load side*

The input parallel capacitances are obtained from

$$C_{\mathrm{eqi}} = \frac{C_{\mathrm{S}}}{2} \tag{25}$$

and the output parallel capacitances are defined by

$$C_{\mathrm{eqo1}} = C_1 \tag{26}$$

and by

$$C_{\mathrm{eqo2}} = C_2 \tag{27}$$

Thus, the selection of the SC capacitor, duty cycle, switching frequency and MOSFET biases the values for the equivalent circuit elements.

3.6 Analysis of the proposed converter employing the equivalent circuit

The analysis of the equivalent circuit supplies equations which can be employed to design the proposed ac–ac converter. These equations are shown in Table 1 and they provide important information on the split-phase ac–ac converter. The variables f and $R_{\mathrm{eqo},x}$ in these equations are the frequency of the ac input source and the equivalent resistance of the load seen by the output 'x' of the split-phase system, respectively, the latter being defined by

$$R_{\mathrm{eqo},x} = \frac{1}{(1/R_{o,x}) + (2/R_{o3})} \tag{28}$$

3.7 Design methodology of the capacitors

The proposed converter is composed for capacitors and switches, and thus the appropriate choice of capacitances is important for the proper operation of the structure. The capacitors influence two characteristics of the proposed converter. One is its operation

IET Power Electron., 2015, Vol. 8, Iss. 6, pp. 918–928

Table 1 Equivalent circuit equations

Variable	Equation
real voltage gain	$g_{v,x} = \dfrac{R_{\text{eqo},x}}{R_\text{s} + R_{\text{eqo},x} + \text{j}\omega C_{\text{eqo},x} R_\text{s} R_{\text{eqo},x}}$
conduction losses	$P_{\text{loss},R_\text{s}} = \sum_{x=1}^{2} \dfrac{v_i^2[1-(\omega C_{\text{eqo},x} R_\text{s})^2]}{R_{\text{eqo},x}^2} R_\text{s}$
switching losses	$P_{\text{loss},R_\text{p}} = 2\dfrac{v_i^2}{R_\text{p}}$
input active power	$P_i = \sum_{x=1}^{2} v_i^2 \left[\dfrac{R_{\text{eqo},x} + R_\text{s} + R_\text{s}(R_{\text{eqo},x}\omega C_{\text{eqo},x})^2}{(R_{\text{eqo},x} + R_\text{s})^2 + (R_{\text{eqo},x} R_\text{s} \omega C_{\text{eqo},x})^2} + \dfrac{1}{R_\text{p}} \right]$
input reactive power	$Q_i = \sum_{x=1}^{2} v_i^2 \left[\dfrac{R_{\text{eqo},x}^2 \omega C_{\text{eqo},x}}{(R_{\text{eqo},x} + R_s)^2 + (R_{\text{eqo},x} R_\text{s} \omega C_{\text{eqo},x})^2} + \omega C_\text{eqi} \right]$
output active power in v_1 and v_2	$P_{o1} = \dfrac{(v_i g_{v1})^2}{R_{o1}}$ and $P_{o2} = \dfrac{(v_i g_{v2})^2}{R_{o2}}$
output active power in v_3	$P_{o3} = \dfrac{[v_i(g_{v1} + g_{v2})]^2}{R_{o3}}$
total output active power	$P_o = P_{o1} + P_{o2} + P_{o3}$
PF	$\text{PF} = \dfrac{P_i}{\sqrt{P_i^2 + Q_i^2}}$
efficiency	$\eta = \dfrac{P_o}{P_i}$

mode (CC, PC or NC) and the other is the reactive power that flows through the converter. In this paper, the aim was to design the capacitors considering the power reactive, since other parameters can be set to adjust the operation mode.

The proposed converter has three capacitors, which can be equal ($C_S = C_1$ and C_2). The losses can be neglected ($R_\text{s} = R_\text{p} = 0$, $P_i = P_o$) in this analysis, and thus the input parallel capacitances are given by

$$C_\text{eqi} = 1.5 C_\text{S} \tag{29}$$

and the input total capacitance seen by the input voltage is obtained by

$$C_{\text{total}\,i} = 3 C_\text{S} \tag{30}$$

The reactive power that flows through the converter is defined in [38] and it is written as

$$Q_i = 6\pi f C_\text{S} V_i^2 \tag{31}$$

Q_i is a capacitive reactive power and it is not dependent on the load type (similarly to the reactive power that flows in a transformer because of magnetising inductance). Therefore the maximum capacitance that can be employed in the converter in relation to a maximum value for the specified reactive power ($Q_{i\max}$) is given by

$$C_\text{S} = C_1 = C_2 \le \frac{Q_{i\,\max}}{6\pi f V_i^2} \tag{32}$$

Thus, a design can specify $Q_{i\max}$ as a percentage of P_o and the capacitor values are then defined.

Capacitors can also be defined by analysing a specified input power factor (PF). On the basis of (31), the maximum capacitance that can be used in relation to a value for the input PF, considering a resistive load and neglecting the losses, is given by

$$C_\text{S} = C_1 = C_2 \le \frac{P_o}{6\pi f V_i^2} \sqrt{\frac{1-\text{PF}^2}{\text{PF}^2}} \tag{33}$$

Defining a normalised capacitance (C_N) as

$$C_\text{N} = \frac{C_\text{S} 6\pi f V_i^2}{P_o} \tag{34}$$

normalised values for C_S, C_1 and C_2 in relation to the input PF of the proposed converter are obtained by

$$C_\text{N} = \sqrt{\frac{1-\text{PF}^2}{\text{PF}^2}} \tag{35}$$

The graph in Fig. 7 is based on (35) and it can be used to select the capacitors of the proposed converter.

4 Design example

4.1 Specification

A design specification was defined with the objective of verifying the performance of the proposed converter, which is:

- $S_o = 1000$ VA output power;
- PF ≥ 0.96 power factor (capacitive);
- $V_{i,\text{rms}} = 110$ V input voltage;
- $V_{o1,\text{rms}} = 110$ V output voltage 1;
- $V_{o2,\text{rms}} = 110$ V output voltage 2;
- $V_{o3,\text{rms}} = 220$ V output voltage 3;
- $f_i = 60$ Hz frequency of ac voltage;
- $\eta > 95\%$ expected efficiency; and
- $D = 0.4$ duty cycle.

The proposed ac–ac converter is designed to operate in PC mode, which requires that $f_\text{s}\tau \ge 0.1$. Thus, for an adequate design the duty cycle must be close to 0.5, the capacitor calculated according to the desired reactive power and the switches and the switching frequency selected so as to maintain $f_\text{s}\tau$ higher than 0.1, while still keeping the switch conduction resistance low (R_on) and the switching frequency (f_s) achievable in the practical implementation. In the following sections, the voltage and current stresses across the components, the choice of components and the choice of switching frequency are presented.

4.2 Voltage and current stresses across the capacitor and MOSFET

The maximum voltage across the components is the peak value of v_i, thus

$$V_{C,\max} = V_{S,\max} = V_{i,\text{pk}} = V_{i,\text{rms}}\sqrt{2} = 155.56\ \text{V} \tag{36}$$

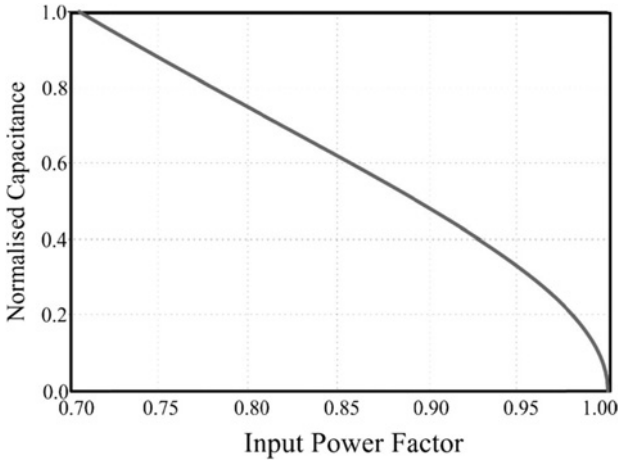

Fig. 7 *Normalised capacitance of C_S, C_1 and C_2 against input PF*

The current stress can be estimated based on the equations detailed in Section 3.3 and considering a balanced load of 1 kVA on outputs 1 and 2 through

$$R_{o1} = R_{o2} = 23\,\Omega \quad \text{and} \quad R_{o3} = \infty\,\Omega \tag{37}$$

The rms values of the current across capacitors C_1 and C_2 are given by

$$I_{C_1,\text{rms}} = I_{C_2,\text{rms}} = 6.0\,\text{A} \tag{38}$$

and that across the SC capacitor is given by

$$I_{C_S,\text{rms}} = 1.2\,\text{A} \tag{39}$$

The rms values for the current in all MOSFET are equal and defined by

$$I_{Si,\text{rms}} = 7.7\,\text{A} \quad i = 1,\ 2,\ ...,\ 8 \tag{40}$$

4.3 Capacitance calculation

The capacitance values for C_1, C_2 and C_S were defined based on the graph in Fig. 7, with the aim of fulfilling the PF specification. The specified value at rated power was 0.96, thus

$$C_N = 0.29 \tag{41}$$

and the absolute values for the capacitances are

$$C_S = C_1 = C_2 \leq \frac{P_o}{6\pi f V_i^2} C_N = 21.7\ \mu\text{F} \tag{42}$$

A value of 20 μF was projected for the three capacitors and each one is composed of two parallel-connected capacitors of 10 μF/400 V/11 A/equivalent series resistance (ESR) = 1.8 mΩ (CDE Cornell Dubilier model 932C4W10 J-F). The capacitors selected are of polypropylene film, because the ac voltages will be applied on them in the proposed converter. A constant reactive power of 273 VAR will flows by converter.

4.4 Choice of switches

The MOSFET that implements the bidirectional switches were chosen with the aim of obtaining the appropriate $f_s\tau$ and a low conduction resistance. Thus, the MOSFET FQA62N25C was selected, which has an $R_{DS(on)}$ value of 35 mΩ at 25°C (or 60 mΩ at 100°C) and accepts up to 62 A. Its maximum drain–source voltage is 250 V and its typical output capacitance (C_{OSS}) is 945 pF. The total conduction resistance of a bidirectional switch (R_{on}) is twice the resistance of a MOSFET and, therefore, the resistance R_{on} is 120 mΩ at 100°C.

4.5 Choice of switching frequency

The values of C_1, C_2, C_S and R_{on} can be applied in the equations in Table 1, and thus the efficiency of the proposed converter can be predicted based on the switching frequency. This procedure allows a switching frequency that provides a high efficiency to be selected. In this case, the switching frequency selected was 100 kHz, and thus the expected efficiency at rated power was 97.3%. The estimated conduction loss was about 23.9 W and the switching loss was about 4.6 W.

The values defined for C_S, f_s and R_{on} ensure a $f_s\tau$ value of 0.48, and therefore the converter operates in PC mode, as desired.

5 Prototype implementation and experimental results

A prototype was built to verify the operation of the proposed converter according to the specifications detailed in Section 4.1 and is shown in Fig. 8*a*. The circuit provides two 110 V output voltages in a split-phase configuration from one 110 V input voltage. The proposed converter operates in open-loop and employs a simple gate driver circuitry (UC3525 pulse width modulation (PWM) modulator), as shown in Fig. 8*b*.

The specific power and the volumetric power density obtained for the prototype were 1.41 kW/kg and 0.7 kW/l. A similar 1 kVA split-phase transformer presented 0.37 kW/kg of specific power and 0.86 kW/l of volumetric power density. Thus, the weight of the proposed converter is reduced by a factor of 3.8 and the volume increased by a factor of 1.2 with regard to the equivalent autotransformer.

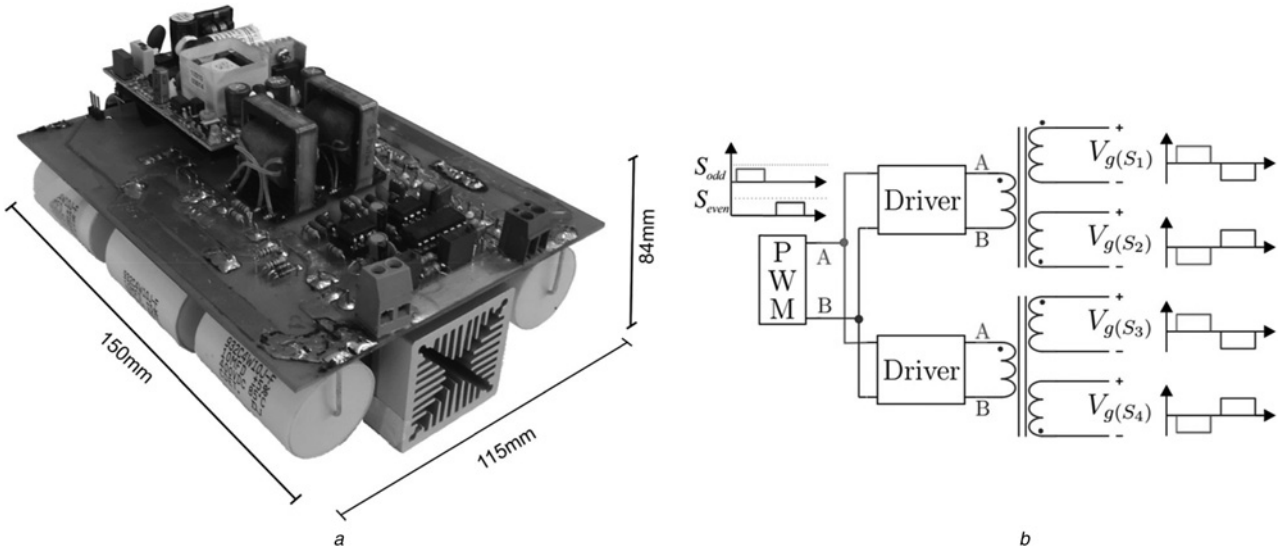

Fig. 8 *Prototype*
a Photo (specific power: 1.41 kW/kg)
b Block diagram of the gate drive circuitry

IET Power Electron., 2015, Vol. 8, Iss. 6, pp. 918–928

Experimental tests were carried out to verify the performance of the proposed converter and the output voltages were measured as shown in Fig. 2.

The system was tested under balanced and unbalanced resistive loads. In the latter case, the following loads were applied: 500 W on v_{o1}, 100 W on v_{o2} and 400 W on v_{o3}, and the input and output voltages of the converter are shown in Fig. 9*a* (the output voltages measured were $v_{o1} = 105$ V, $v_{o2} = 107$ V and $v_{o3} = 212$ V). The output voltages are filtered by capacitors C_2 and C_3, and thus the voltage ripple at 100 kHz was 1% and the total harmonic distortion (THD) was 0.3%. As expected, the voltages v_{o1}, v_{o2} and v_{o3} are in phase with v_i, the amplitudes of v_{o1} and v_{o2} are similar to that of v_i and the amplitude of v_{o3} is twice that of v_i. Therefore it was verified that the aim of obtaining two output voltages (a split-phase system) from one single-phase voltage source was achieved. The output currents i_{o1}, i_{o2} and i_{o3} are presented in Fig. 9*b*. These unbalanced loads are typical of a split-phase system and even in these cases the proposed converter maintains regulated output voltages.

Another important test was carried out to verify the performance under different types of loads. An inductive–resistive load of 200 VA with a PF of 0.6, a non-linear load of 400 VA with a crystal factor of 2.5 and a resistive load of 300 W were applied to outputs 1, 2 and 3, respectively. Even under these conditions, the output voltages remained regulated, as can be seen in Fig. 9*c*. The voltage measurements were $v_{o1} = 108$ V, $v_{o2} = 106$ V and $v_{o3} = 214$ V. The equivalent circuit of the proposed converter showed a small series resistance (R_s). Therefore there is only a small voltage drop on R_s with a non-linear load, and thus the non-linear current causes an insignificant distortion in the voltages (THD were lower than 1%). The output currents i_{o1}, i_{o2} and i_{o3} are shown in Fig. 9*d*, where i_{o1} is the lag, i_{o2} is a typical non-linear current and i_{o3} is a typical resistive load.

One advantage of the proposed converter in relation to conventional converters is that it can operate within a wide range of frequencies, with no change in the design. This is because the power circuit does not have magnetic elements. The converter was tested, applying input voltages of 16.66 Hz (Fig. 10*a*) and 400 Hz (Fig. 10*b*), to verify this characteristic. The input voltage v_i and output voltages v_{o1} and v_{i2} for both cases are properly regulated.

The experimental efficiency curve obtained is shown in Fig. 11*a* and it is clear that for a wide range of loads it was higher than 96%, the rated power was 95.8% and the maximum value was 97.2% at 40% of load. The output voltage regulation curves for v_{o1}, v_{o2} and v_{o3} in Fig. 11*b* show that the voltage drop in the rated power was $< 3.5\%$ (3.85 V). The input PF curve for resistive load in Fig. 11*c* shows very good agreement between the calculations

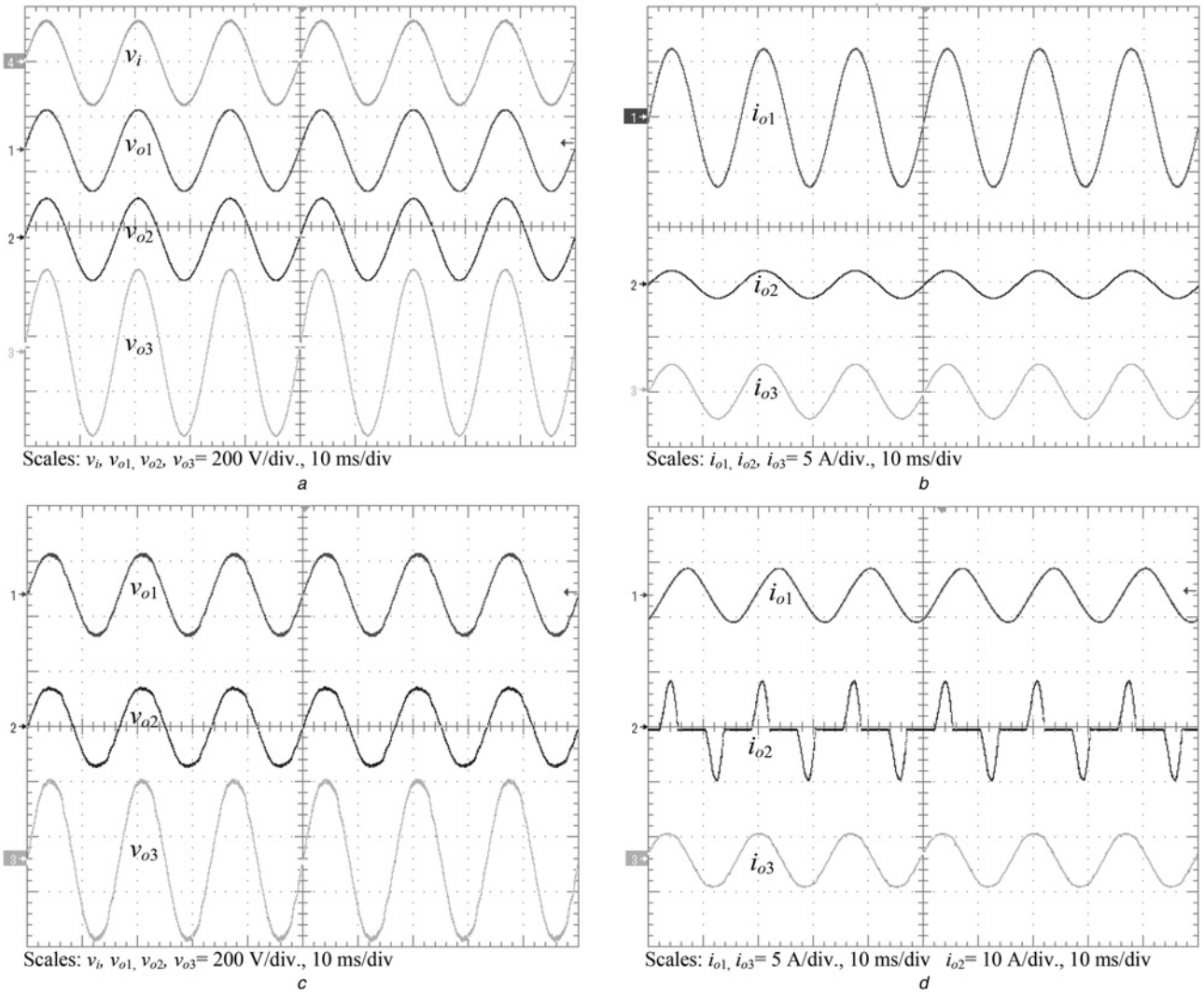

Fig. 9 *Experimental results*

a Input and output voltages (v_i, v_{o1}, v_{o2} and v_{o3}) under resistive and unbalanced loads
b Output currents (i_{o1}, i_{o2} and i_{o3}) under resistive and unbalanced loads
c Output voltages under different types of loads: inductive–resistive (v_{o1}), non-linear (v_{o2}) and resistive (v_{o3})
d Output currents under different types of loads: inductive–resistive (i_{o1}), non-linear (i_{o2}) and resistive (i_{o3})

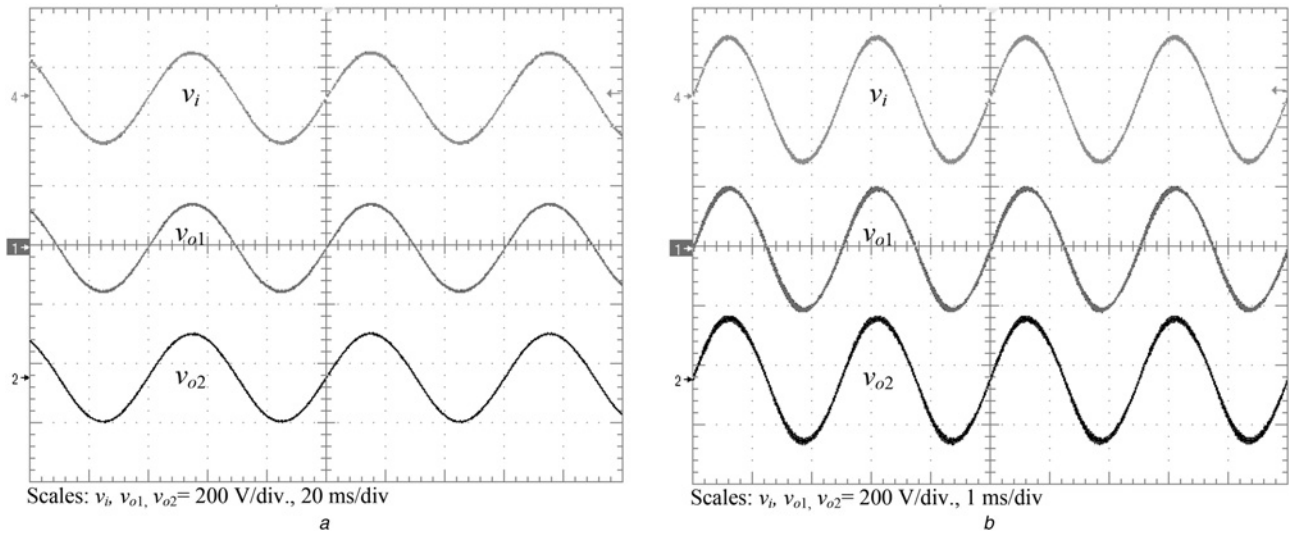

Fig. 10 *Experimental results*

a Input (v_i) and output voltages (v_i, v_{o1}, v_{o2}) for an input voltage of 16.66 Hz
b Input (v_i) and output voltages (v_{o1}, v_{o2}) for an input voltage of 400 Hz

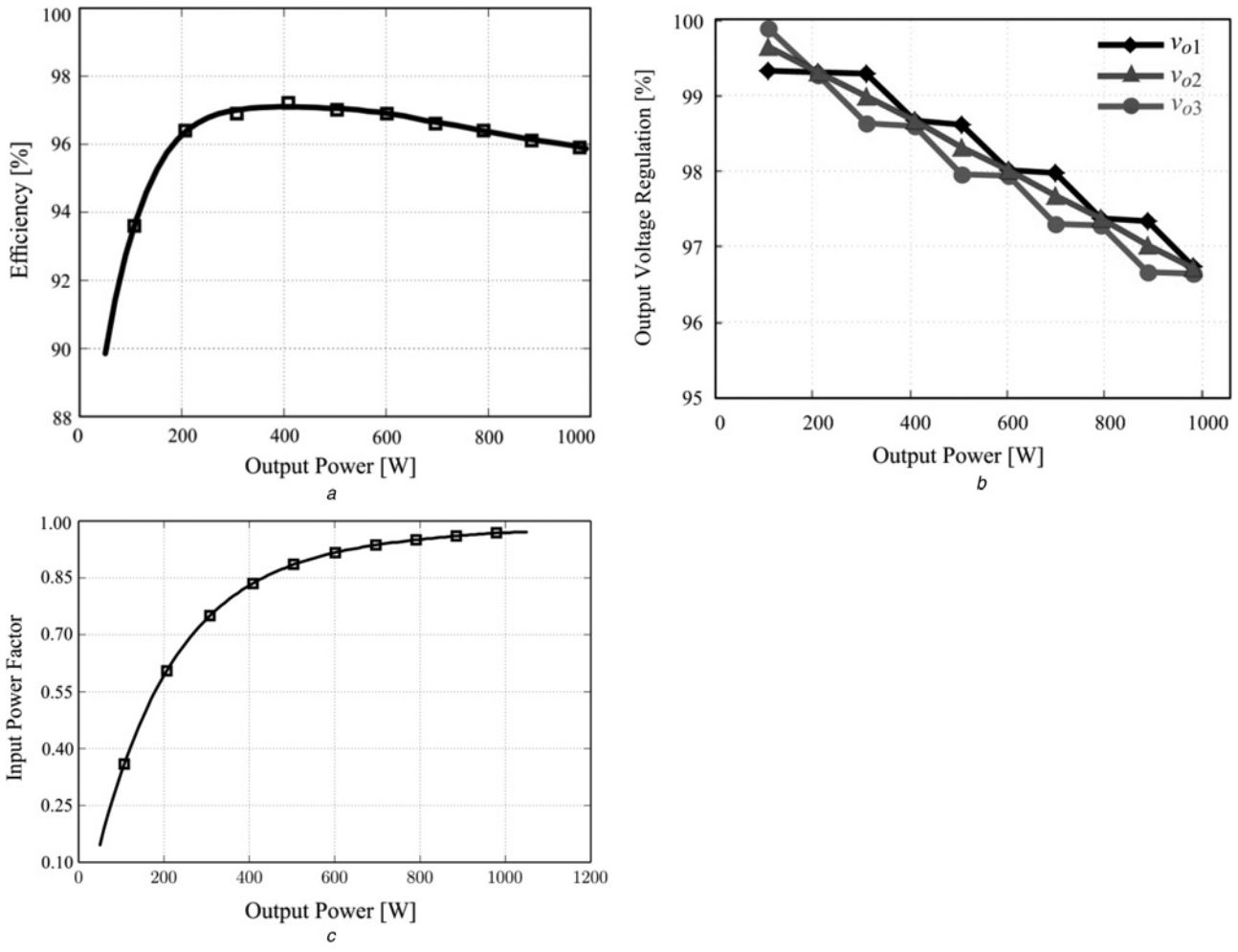

Fig. 11 *Experimental results*

a Experimental efficiency curve for the proposed converter
b Experimental regulation curves for output voltages v_{o1}, v_{o2} and v_{o3}
c Experimental input power factor curve for resistive load

IET Power Electron., 2015, Vol. 8, Iss. 6, pp. 918–928

Table 2 Quantitative comparison between the proposed converter and an equivalent split-phase transformer

Characteristic	Proposed converter	Split-phase transformer
gain	1 : 1 : 1	1 : 1 : 1
specific power, kW/kg	1.42	0.37
density POWER, kW/l	0.7	0.86
maximum efficiency, %	97.2	93.5
efficiency at rated power, %	95.8	90.5
regulation, %	97	91%
input PF	0.96 (capacitive)	0.99 (inductive)
weight, kg	0.7	2.7
volume, l	1.42	1.16
cost	1 pu	0.2 pu

and experimental measurements. The PF is close to one (> 0.96) at rated power.

A quantitative comparison between the tested prototype and a 1 kVA split-phase transformer of low cost is shown in Table 2. The results verify that the proposed converter has a better performance than the split-phase transformer.

6 Conclusions

A split-phase direct ac–ac power converter based on the SC principle has been introduced and verified. The converter outputs, which are two series-connected voltage sources, were used to implement a split-phase system and to supply three output voltages from one single-phase voltage source (two equal to and one twice the input voltage).

The main notable characteristics of the proposed split-phase converter based on the SC are that: (i) it carries out direct ac–ac conversion; (ii) it employs only capacitors and switches in the power circuit, which can improve its efficiency, power density, specific power and the circuit can operate with input voltages in a wide range of frequencies, without requiring changes in its design; (iii) the three output voltages provided by the converter follow the waveform of the input voltage and they remain balanced even under unbalanced, inductive and non-linear loads and (iv) the converter operates in open-loop with a constant duty cycle of close to 0.5 and the stress voltage in all components is equal to the input voltage.

When the proposed converter is compared with a commercial split-phase transformer (usually of low cost), the main advantages of the proposed converter are related to the weight, specific power, efficiency, regulation, absence of magnetic elements and range of operation frequency. The main disadvantages are associated with the cost, reliability and operation temperature. Further studies need to be carried out to address these drawbacks, which are frequently evident when power converters are compared with conventional technologies.

The proposed split-phase converter based on SC is suitable for modern applications around the world where a split-phase system needs to be generated from a renewable energy source, distributed generation, UPS, battery bank, electric/hybrid vehicle, smart grid or even the electrical grid itself. It can also be used in devices and traditional applications where currently conventional transformers and autotransformers are employed.

7 References

1 Bakshi, U.A., Bakshi, M.V.: 'Voltage control and distribution system', in Power system – I (Pune, India, Technical Publications Pune, 2009), ch. 8, pp. 2–7
2 Croft, T., Summers, W.: 'American electricians' handbook' (McGraw Hill, New York, 1987, 7th edn.), ch. 3, pp. 3–22
3 Gonen, T.: 'Electric power distribution system engineering' (CRC Press, Boca Raton, 2007, 2nd edn.), pp. 280–290
4 Tanaka, T., Sekiya, T., Tanaka, H., Hiraki, E., Okamoto, M.: 'Smart charger for electric vehicles with power quality compensator on single-phase three-wire distribution feeders'. 2012 IEEE Energy Conversion Congress and Exposition (ECCE), 2012, pp. 3075–3081
5 Kersting, W.H.: 'Center-tapped transformer and 120/240 V secondary models', *IEEE Trans. Ind. Appl.*, 2009, **45**, (2), pp. 575–581
6 Wei, W., Yingnan, W., Lijie, X., Yanfang, C., Rui, L.: 'Application of single-phase three-wire transformer model in distribution network with solar home system'. 2011 Int. Conf. on Advanced Power System Automation and Protection (APAP), October 2011, vol. 3, no., pp. 1851–1856
7 Pilo, E., Rouco, L., Fernandez, A., Abrahamsson, L.: 'A monovoltage equivalent model of bi-voltage autotransformer-based electrical systems in railways', *IEEE Trans. Power Deliv.*, 2012, **27**, pp. 699–708
8 Boroyevich, D., Cvetkovic, I., Burgos, R., Dong, D.: 'Intergrid: a future electronic energy network?', *IEEE J. Emerg. Sel. Top. Power Electron.*, 2013, **1**, pp. 127–138
9 Liangzong, H.: 'High-performance bridge modular switched-capacitor converter with small component requirement based on output impedance analysis for low loss', *IEEE Trans. Power Electron.*, 2013, **28**, pp. 4668–4680
10 Amjadi, Z., Williamson, S.S.: 'A novel control technique for a switched-capacitor-converter-based hybrid electric vehicle energy storage system', *IEEE Trans. Ind. Electron.*, 2010, **57**, pp. 926–934
11 Yuh-Shyan, H., Hsiao-Hsing, C., Yuan-Bo, C., Jiann-Jong, C.: 'A high-efficiency DC–DC converter with wide output range using switched-capacitor front-end techniques', *IEEE Trans. Ind. Electron.*, 2014, **61**, pp. 2244–2251
12 Jiao, Y., Luo, F.L.: 'N-switched-capacitor buck converter: topologies and analysis', *IET Power Electron.*, 2011, **4**, pp. 332–341
13 Chang, Y.H.: 'Complex programmable logic device-based closed-loop implementation of switched-capacitor step-down DC–DC converter for multiple output choices', *IET Electr. Power Appl.*, 2007, **1**, pp. 926–936
14 Yuan-mao, Y., Cheng, K.W.E.: 'Multi-input voltage-summation converter based on switched-capacitor', *IET Power Electron.*, 2013, **6**, pp. 1909–1916
15 Ye, Y., Cheng, K.W.E.: 'Multi-port voltage-subtracting circuit based on resonant switched-capacitor', *IET Power Electron.*, 2012, **5**, pp. 693–701
16 Ko, Y.P., Lee, Y.S., Chao, W.H.: 'Analysis, design and implementation of fuzzy logic controlled quasi-resonant zero-current switching switched-capacitor bidirectional converter', *IET Power Electron.*, 2011, **4**, pp. 683–692
17 Chan, C.K., Cheng, K.W.E., Ho, S.L.: 'Half-bridge converter based on switched-capacitor resonance without using deadtime control for automotive applications', *IET Power Electron.*, 2011, **4**, pp. 657–662
18 Kim, M., Kim, C., Kim, J., Moon, G.: 'A chain structure of switched capacitor for improved cell balancing speed of lithium-ion batteries', *IEEE Trans. Ind. Electron.*, 2013, p. 1
19 Ueno, F., Inoue, T., Oota, I.: 'Realization of a switched-capacitor AC–DC converter using a new phase controller'. IEEE Int. Symp. on Circuits and Systems, 1991, 2, pp. 1057–1060
20 Tsunoda, A., Hinago, Y., Koizumi, H.: 'Level and phase shifted PWM for 7-level switched-capacitor inverter using series/parallel conversion', *IEEE Trans. Ind. Electron.*, 2013, p. 1
21 Hinago, Y., Koizumi, H.: 'A switched-capacitor inverter using series/parallel conversion with inductive load', *IEEE Trans. Ind. Electron.*, 2012, **59**, pp. 878–887
22 Jing, Z., Han, Y., Xiangning, H., Cheng, T., Jun, C., Zhao, R.: 'Multilevel circuit topologies based on the switched-capacitor converter and diode-clamped converter', *IEEE Trans. Power Electron.*, 2011, **26**, pp. 2127–2136
23 Babaei, E., Sheermohammadzadeh Gowgani, S.: 'Hybrid multilevel inverter using switched-capacitor units', *IEEE Trans. Ind. Electron.*, 2013, p. 1
24 Yi-Ping, H., Jiann-Fuh, C., Tsorng-Juu, L., Lung-Sheng, Y.: 'Novel high step-up DC–DC converter with coupled-inductor and switched-capacitor techniques', *IEEE Trans. Ind. Electron.*, 2012, **59**, pp. 998–1007
25 Zhao, Y., Li, W., Deng, Y., He, X.: 'High step-up boost converter with passive lossless clamp circuit for non-isolated high step-up applications', *IET Power Electron.*, 2011, **4**, pp. 851–859
26 Mishima, T., Hiraki, E., Nakaoka, M.: 'High-frequency link symmetrical active edge resonant snubbers-assisted ZCS-PWM DC–DC converter', *IET Electr. Power Appl.*, 2007, **1**, pp. 907–914
27 Lee, Y.S., Ko, Y.P.: 'Switched-capacitor bi-directional converter performance comparison with and without quasi-resonant zero-current switching', *IET Power Electron.*, 2010, **3**, pp. 269–278
28 Oota, I., Ueno, F., Harada, I., Inoue, T.: 'Power supply for electroluminescent lamp employing a switched-capacitor AC–AC converter', *Electron. Commun. Jpn. 2, Electron.*, 1995, **78**, p. 4
29 Terada, S., Oota, I., Eghchi, K., Ueno, F.: 'A switched-capacitor (SC) AC–DC or AC–AC converter with arbitrarily output voltage using the same circuit configuration'. PESC '06. 37th IEEE Power Electronics Specialists Conf., 2006, pp. 1–4
30 Ben-Yaakov, S.: 'On the influence of switch resistances on switched-capacitor converter losses', *IEEE Trans. Ind. Electron.*, 2012, **59**, pp. 638–640
31 Evzelman, M., Ben-Yaakov, S.: 'Average-current-based conduction losses model of switched capacitor converters', *IEEE Trans. Power Electron.*, 2013, **28**, pp. 3341–3352
32 Villar-Pique, G., Bergveld, H.J., Alarcon, E.: 'Survey and benchmark of fully integrated switching power converters: switched-capacitor versus inductive approach', *IEEE Trans. Power Electron.*, 2013, **28**, pp. 4156–4167
33 Henry, J.M., Kimball, J.W.: 'Practical performance analysis of complex switched-capacitor converters', *IEEE Trans. Power Electron.*, 2011, **26**, pp. 127–136
34 Muller, L., Kimball, J.W.: 'A dynamic model of switched-capacitor power converters', *IEEE Trans. Power Electron.*, 2014, **29**, pp. 1862–1869
35 Chun-Kit, C., Siew-Chong, T., Tse, C.K., Ioinovici, A.: 'On energy efficiency of switched-capacitor converters', *IEEE Trans. Power Electron.*, 2013, **28**, pp. 862–876

36 Kiratipongvoot, S., Siew-Chong, T., Ioinovici, A.: 'Phase-shift interleaving control of variable-phase switched-capacitor converters', *IEEE Trans. Ind. Electron.*, 2013, **60**, pp. 5575–5584
37 Lazzarin, T.B., Andersen, R.L., Martins, G.B., Barbi, I.: 'A 600 W switched-capacitor AC–AC converter for 220 V/110 V and 110 V/220 V applications', *IEEE Trans. Power Electron.*, 2012, **27**, pp. 4821–4826
38 Andersen, R.L., Lazzarin, T.B., Barbi, I.: 'A 1 kW step-up/step-down switched-capacitor AC–AC converter', *IEEE Trans. Power Electron.*, 2013, **28**, pp. 3329–3340
39 Lazzarin, T.B., Moccelini, M.P., Barbi, I.: 'Direct buck-type AC/AC converter based on switched-capacitor'. Proc. Brazilian Power Electronics Conf. (COBEP2013), Gramado, Brazil, 2013, p. 6
40 Lazzarin, T., Barbi, I., Andersen, R.: 'A switched-capacitor three-phase AC–AC converter', *IEEE Trans. Ind. Electron.*, 2014, p. 1
41 Ben-Yaakov, S.: 'Behavioral average modeling and equivalent circuit simulation of switched capacitors converters', *IEEE Trans. Power Electron.*, 2012, **27**, pp. 632–636