A Family of High-Voltage Gain Single-Phase Hybrid Switched-Capacitor PFC Rectifiers

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Abstract—This paper presents the derivation, the analysis, and the experimentation of a family of unidirectional three-level PFC rectifiers, based on pulse-width-modulated hybrid switched capacitor principle. The topologies feature reduced voltage stress across the switches, low number of switches, control of the output voltage, and high-voltage gain without the utilization of transformers. Experimental results for a laboratory prototype of 220 V$_{r.m.s.}$ to 1600 V$_{d.c.}$ voltages and nominal power of 2500 W are included in the paper, to validate the theoretical analysis, where the measured maximum efficiency reached 97.91%. The proposed converters are suitable for applications that require rectification with unity power factor and high-voltage gain.

Index Terms—High gain, hybrid switched-capacitor converters, power factor correction (PFC), three-level, unidirectional.

I. INTRODUCTION

RECENTLY, applications requiring dc power supplies with high voltage have increased, for both laboratory researches and industry [1], [2]. Converters with these features are desired in renewable energy systems, X-ray systems, and motor drivers. In many of these applications, the main source is the ac grid and ac–dc conversion requires a high dc-link voltage. It can be used to feed a load or as input stage to another power supply. The large majority of applications does not require isolation and bidirectional flow, leading to simple and robust unidirectional solutions. In the literature, there are a variety of proposals for high-voltage gain ac–dc converting, which can be divided into active and passive solutions.

Within the passive solutions, converters that have become popular are the voltage multipliers, e.g., Cockcroft–Walton and Dickson converters [3]–[6]. These consist only of diode-capacitor cells and can be cascaded in several stages in order to increase the voltage gain. Also, this kind of structure has not controlled semiconductors, besides having low voltage stress on the components. However, such structures, because they operate at the frequency of the power grid, present high capacitance, which increases the volume and cost. In addition, the current drawn from the power grid has a strong harmonic distortion, which makes it prohibitive for some applications. Another drawback is the impossibility of regulating the output voltage, being the function of output load and input voltage and, therefore, cannot operate as a universal power supply.

By contrast, the active PWM solutions could have high power factor and excellent regulation of output voltage, independent of output load and input voltage. Typically, PFC operation is performed by storing and transferring energy from inductors. The need for operation as PFC comes from the imposition of strict technical standard, such as IEC 61000-3-2, which enjoin limit to amplitude of harmonic frequencies produced by the static power converter.

With the objective of increasing the voltage gain, active voltage-doubler or three-level PWM converters are employed because they allow the voltage stress in the semiconductors and the ripple current in the inductor to be reduced [7]–[12]. Additionally, these converters have low conduction and commutation losses, and high power density [7].

However, the three-level PWM converters present limitations concerning the voltage range operation, typically less than 1000 V, due to restrictions of commercial components. For higher voltages, other solutions must be used, such as converters with more levels or galvanic isolation. Nonetheless, it increases the number of switches, cost, and complexity [13]–[17].

Due to the limitations of voltage multipliers and active conventional boost converters, currently the number of topologies that combine the output characteristics of the multiplier converters operating at high frequency (switched capacitors) with the input characteristics of conventional converters (inductive storage) has increased. The converters that combine such features are referred to as hybrid switched-capacitor converters (HSCC) [18]–[24].

HSCC are attractive because they reduce the voltage stress on the switches, have a low number of switches and higher voltage gain and do not require isolation [18]. Additionally, they present low-ripple current, due to the presence of the inductor, and better output voltage regulation than conventional switched-capacitor topologies. These converters are often proposed in high gain dc–dc conversion [5], [18], [20]–[29]. However, the utilization of this concept in high gain ac–dc conversion is still unusual, what propitiates opportunities for research [30]–[33].

Due to the limitations of conventional three-level PFC rectifiers and based on the characteristics of the voltage multiplier converters, this paper proposes a new family of hybrid switched-capacitor PFC rectifiers with unidirectional flow and three-level operation for applications requiring high-voltage gain.

II. PROPOSED CONVERTERS

The family of six hybrid switched-capacitor unidirectional ac–dc converters applied to power factor correction is shown in

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Fig. 1. Family of six proposed high-voltage gain ac–dc hybrid unidirectional converters.

The proposed converters are named Type I to Type VI. Every converter is composed of eight to ten diodes, eight capacitors and, depending on the topology, could have one or two power switches. The switches of the topologies are represented by insulated-gate bipolar transistors. However, other technologies of semiconductors, e.g., MOSFET’s can be used.

The main feature of this family is the reduced number of power switches to achieve high-voltage gain. It implies reduced losses and lower number of gate-drivers circuits. The converters preserve the characteristics of the voltage multipliers, i.e., increased voltage gain. They also have the input characteristics of the conventional three-level converters, i.e., input current control. The capacitors $C_{j,k}$, $j \in \{1 \ldots 3\}$, $k = A, B$ does not require active control to balance voltage. A comparative analysis between proposed converters can be seen in Table I.

Due to the connection with the midpoint 0, the semiconductors are subjected to one-quarter of the dc-link voltage in contrast to one-half of the full dc-link voltage in typical three-level rectifiers.

The capacitors $C_{0,A}$ and $C_{0,B}$ are not necessary for the operation of topologies; however, they are inserted to provide a low impedance path for 120-Hz ripple in the instantaneous power. These capacitors have very large capacitance compared with the capacitors $C_{j,k}$, $j \in \{1 \ldots 3\}$, $k = A, B$.

<table>
<thead>
<tr>
<th>Features</th>
<th>Type I</th>
<th>Type II</th>
<th>Type III</th>
<th>Type IV</th>
<th>Type V</th>
<th>Type VI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semiconductors in conduction during first operation stage</td>
<td>3</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Semiconductors in conduction during second operation stage</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Elements subject to $V_o/4$</td>
<td>all</td>
<td>all</td>
<td>all</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Elements subject to $V_o/2$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Number of fast diode</td>
<td>6</td>
<td>8</td>
<td>8</td>
<td>10</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Number of slow diode</td>
<td>2</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

A. Operational Stages

Fig. 2 shows the operational stages of the six proposed converters. There are two stages, one for storage and another for energy transfer. In this figure, the inductor $L_b$ and input voltage $v_g$ were represented by a current source $i_g$.

The Type I converter is used to illustrate the operation stages; however, the other converters have similar operations. In order
to simplify the equations, a small resistor \( r_{C3,A} \) is inserted, representing ESR of the capacitor \( C_{3,A} \) (see Fig. 3).

The other parasitic resistances are neglected during analysis.

The output capacitors \( C_{o,A} \) and \( C_{o,B} \) can be modeled as voltage sources.

For analysis, it is supposed that converters operate in the no-charge conduction mode (NC), the definition proposed by [34]. It is assumed that the time constant \( RC \) of the circuit is much larger than the switching time, \( T_i \), \( (RC \gg T_i) \), i.e., there is no significant change of current in the capacitors during the switching time \( T_i \).

The first stage of operation is characterized by the turn ON of the switch \( S_{1,A} \) [see Fig. 3(a)]. During this time interval, the inductor \( L_b \) stores energy through the input voltage \( v_g \). As the voltage across the capacitor \( C_{1,A} \) is slightly larger than the voltage over the capacitor \( C_{3,A} \), the diode \( D_{2,A} \) conducts transferring energy from \( C_{1,A} \) to \( C_{3,A} \). The level 0 V is applied in the switched terminal \( a \), relative to node \( o \).

During the second stage, the switch \( S_{1,A} \) is turned OFF and the diodes \( D_{1,A} \) and \( D_{3,A} \) start conducting, transferring the energy stored in the inductor to the capacitors \( C_{1,A}, C_{2,A} \) and the load. During this time interval, the level \( +V_o/4 \) is placed on the switched terminal \( a \), relative to node \( o \).

In Fig. 3, it can be observed that all components are submitted to one-fourth of the output voltage, allowing the use of low-voltage semiconductors. In Fig. 4, the main waveforms of the Type I converter, which are valid to the positive half-cycle of the voltage grid are presented. In this figure, the details of the shape current of diode \( D_{2,A} \) to three modes, complete charge—CC; partial charge—PC, and no charge—NC are illustrated [34]. It can be seen that PC and NC modes have similar shapes.

### B. Steady-State Analysis

The steady-state analysis is focused on the Type I converter; however, it can be extended to other converters. It is considered that the converter operates in continuous conduction mode. Only the series resistances of the capacitors \( C_{3,k}, k \in \{A, B\} \) are considered in the analysis. The purely sinusoidal input voltage \( v_g \) is assumed constant within one switching period \( T_s \). Also, the input current \( i_g \) ripple is neglected and dc-link voltage is kept constant, thus it can be represented by a voltage source (see Fig. 3).

Considering that both input voltage \( v_g \) and input current \( i_g \) are purely sinusoidal, then

\[
\begin{align*}
v_g &= V_{g, pk} \cdot \sin(\omega t) \\
i_g &= I_{g, pk} \cdot \sin(\omega t)
\end{align*}
\]

where \( V_{g, pk} \) and \( I_{g, pk} \) are the peak voltage and peak current input, respectively.

Neglecting the voltage drop across the inductor \( L_b \), the function of duty cycle could be defined as

\[
d = 1 - M \cdot \sin(\omega t)
\]

where \( M \) is the modulation index and equals to

\[
M = \frac{4 \cdot V_{g, pk}}{V_o}.
\]

Through the operation stages, it can be determined, and a set of equations can be written describing the behavior of the
currents in all the elements for each operating stage

First operation stage

\[
\begin{align*}
    i'_{C,1,A} &= -\frac{1}{4} \left( 1 - d \right) i_g \\
    i'_{C,2,A} &= \frac{1}{4} \left( 1 - d \right) i_g \\
    i'_{C,3,A} &= i_{D,2,A} = \frac{1}{2} \left( 1 - d \right) i_g \\
    i'_{S,1,A} &= \frac{1}{2} \left( 1 + d \right) i_g \\
    i'_{D,1,b} &= i_g
\end{align*}
\]

Second operation stage

\[
\begin{align*}
    i''_{C,1,A} &= \frac{1}{4} i_g \\
    i''_{C,2,A} &= -\frac{1}{4} i_g \\
    i''_{C,3,A} &= i''_{D,3,A} = \frac{1}{2} i_g \\
    i''_{D,1,A} &= \frac{1}{2} i_g \\
    i''_{D,1,b} &= i_g
\end{align*}
\]

Based on (5), the current stress and both RMS and average values in the capacitors and semiconductors can be calculated. These values are determined substituting (5) into (6), as follows:

\[
\begin{align*}
    \langle I_x \rangle_{\text{avg}}^T_s &= \frac{1}{T_s} \left( \int_0^{d T_s} i'_x dt + \int_{d T_s}^{T_s} i''_x dt \right) \\
    \langle I_x \rangle_{\text{rms}}^T_s &= \frac{1}{T_s} \left( \int_0^{d T_s} (i'_x)^2 dt + \int_{d T_s}^{T_s} (i''_x)^2 dt \right) \\
    I_{x,\text{avg}} &= \frac{1}{2\pi} \int_0^{\pi} \langle I_x \rangle_{\text{avg}}^T_s \, d\omega t \\
    I_{x,\text{rms}} &= \sqrt{\frac{1}{2\pi} \int_0^{\pi} \langle I_x \rangle_{\text{rms}}^T_s \, d\omega t}
\end{align*}
\]

Table II lists the average current stress in semiconductors, calculated within of the switching period \( T_s \) and period of the grid voltage \( T_g \).

Table III shows the RMS current stress in the capacitors and semiconductors. The term \( \beta \) is defined as

\[
\beta = \sqrt{1 - M^2}.
\]

Fig. 5 shows the behavior of the normalized RMS currents, weighted by output current, defined as

\[
I_{\text{base}} = \frac{P_o}{V_o}.
\]

Therefore, \( I_x = I_x / I_{\text{base}} \), where \( x \) represents the element involved. The term \( \sum_{i=1}^{M} I_{x,\text{rms}} \) represents the sum of RMS currents in the semiconductors.

C. Inductor Current Ripple

The high-frequency inductor current ripple is directly extracted from the operational stages of the converter.

The envelop of normalized input current through the inductor is determined by

\[
\overline{\Delta i}_{L,\text{pk-pk}} = (1 - d) \cdot d
\]

where \( \overline{\Delta i}_{L,\text{pk-pk}} \) represent the normalized current through the inductor and is defined by

\[
\overline{\Delta i}_{L,\text{pk-pk}} = \Delta i_{L,\text{pk-pk}} \cdot \frac{V_o}{4 \cdot L_b \cdot f_s}.
\]

As in conventional three-level converters, the maximum peak current occurs when \( \omega t = \mathbb{R} \{ \arcsin \left( \frac{1}{2M} \right) \} \), which leads to \( \overline{\Delta i}_{L,\text{pk-pk}} = 0.25, M > 0.5 \). Thus, the inductance value can be calculated according to

\[
L_b = \frac{V_o \cdot T_s}{16 \cdot \Delta i_{L,\text{pk-pk}}}.
\]

The (11) is valid to \( M > 0.5 \) and to all proposed converters.

D. DC-Link Voltage Ripple

Assuming that the capacitors \( C_{j,k}, j \in \{1 \ldots 3\}, k = A, B \), have low capacitance, then the ripple of dc-link voltage is determined by the output capacitors. Thus, the choice of capacitance value of output capacitors \( C_{o,i}, i \in \{A, B\} \), is made according to the ripple value. Therefore

\[
\Delta V_{C_o} = \frac{2 \cdot P_o \cdot (C_{o,A} + C_{o,B})}{2 \pi \cdot f_g \cdot V_o \cdot C_{o,A} \cdot C_{o,B}}
\]

where \( \Delta V_{C_o} \) represents the ripple across the dc-link voltage. Each output capacitor has half of the ripple. Therefore

\[
C_{o,i} \geq \frac{2 \cdot P_o}{\pi \cdot f_g \cdot V_o \cdot \Delta V_{C_o}}, \quad i \in \{A, B\}.
\]
TABLE III
RMS VALUE IN ALL COMPONENTS

<table>
<thead>
<tr>
<th>Comp. ( k ) ( k = A, B )</th>
<th>RMS value within ( T_s ) ( \langle I_{\text{op}} \rangle_{r_{\text{rms}}} )</th>
<th>Average value within ( T_s ) ( \langle I_{\text{op}} \rangle_{r_{\text{rms}}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{1,k} )</td>
<td>( \frac{i_g}{\pi} \sqrt{\frac{1-d}{a}} )</td>
<td>( I_{p,k} \sqrt{\frac{m}{\pi}} \sqrt{\frac{\beta}{m}} )</td>
</tr>
<tr>
<td>( C_{2,k} )</td>
<td>( \frac{i_g}{\pi} \sqrt{\frac{1-d}{a}} )</td>
<td>( I_{p,k} \sqrt{\frac{m}{\pi}} \sqrt{\frac{\beta}{m}} )</td>
</tr>
<tr>
<td>( C_{3,k} )</td>
<td>( \frac{i_g}{\pi} \sqrt{\frac{1-d}{a}} )</td>
<td>( I_{p,k} \sqrt{\frac{m}{\pi}} \sqrt{\frac{\beta}{m}} )</td>
</tr>
<tr>
<td>( S_{i,A} )</td>
<td>( \frac{1}{2\pi} \sqrt{\frac{1}{\pi}} )</td>
<td>( I_{s,k} \sqrt{\frac{m}{\pi}} \sqrt{\frac{\beta}{m}} )</td>
</tr>
<tr>
<td>( D_{1,k} )</td>
<td>( \frac{i_g (1-d)}{\sqrt{1-d}} \sqrt{\frac{1}{\pi}} )</td>
<td>( I_{s,k} \sqrt{\frac{m}{\pi}} \sqrt{\frac{\beta}{m}} )</td>
</tr>
<tr>
<td>( D_{2,k} )</td>
<td>( \frac{i_g (1-d)}{\sqrt{1-d}} \sqrt{\frac{1}{\pi}} )</td>
<td>( I_{s,k} \sqrt{\frac{m}{\pi}} \sqrt{\frac{\beta}{m}} )</td>
</tr>
</tbody>
</table>

III. CONTROL STRATEGY

Suitable PWM control scheme for operation as PFC to proposed converters are shown in Fig. 6. Three voltages and one current to obtain a good performance are measured. The input voltage \( v_g \) is used to generate the shape current reference and also to feedforward loop. The partial output voltages \( v_o \), and input current \( i \), are measured and processed by the output voltage balancing loop, it should maintain the dc-link voltage stable. The load current is used to generate the shape current reference. The input current is compared with the reference generating an error signal. This error goes through to a controller which, added to the feedforward signal, produces the modulation signal \( m \) which is synthesized by the PWM modulator. Also, an output voltage balancing loop is inserted, whose goal is to generate small average values in input current to ensure that partial output voltages have the same average value.

A. Current-Loop Control

To model the output voltage, it is assumed that capacitors \( C_{o,A} \) and \( C_{o,B} \) do not have dynamic (large capacitance), such that it can be represented by a voltage source. Thus, the linear model that depicts the modulating signal \( m \) with input current \( i_g \) in the frequency domain is given by

\[
\frac{i_g(s)}{m(s)} = \frac{V_o}{4 \cdot s \cdot L_b}.
\]

B. Voltage-Loop Control

To model the output voltage, it is assumed that capacitors \( C_{o,A} \) and \( C_{o,B} \) have much higher capacitance than capacitors \( C_{j,k}, j \in \{1, 2, 3\}, k = A, B \). These capacitors shall provide a low impedance path to 120 Hz ripples in instantaneous power and low ripple in dc-link voltage. Given these considerations, the small signal model that depicts variations of the output voltage with the conductance signal is provided by

\[
\frac{\tilde{v}_o(s)}{\tilde{g}_m(s)} = \frac{V_o^2}{4V_o} \frac{R_o}{\left( \frac{1}{2} s L_b C_o \right)^2 + 1}
\]

where \( C_o = C_{o,A} || C_{o,B} \) and \( R_o \) is the resistance of the output load.

In order to validate the mathematical models, in Fig. 8 the behavior of the output voltage, partial output voltages \( v_{op} \) and \( v_{on} \), and input current \( i_g \) to a step-up in the output voltage.
reference from 1600 to 1700 V are presented. For the simulation capacitors, \( C_{i,k} = 60 \mu\text{F} \) and \( C_{o,k} = 470 \mu\text{F} \), \( j \in \{1 \ldots 3\}, k = A, B \) were employed. One can see an excellent agreement between the theoretical model and the simulation results. The capacitors \( C_{i,k} \) are much smaller than the output capacitors, reducing significantly their influence on the dynamics of the loop voltage. Also, in Fig. 8, it can be seen that the partial output voltages \( v_{op} \) and \( v_{on} \) are balanced around half of the output voltage.

### IV. Simulation and Experimental Results

In order to validate the theoretical analysis and the operation of the proposed three-level ac–dc converters, simulation and experimental results for the Type I are presented in this section. The specifications, both simulation and experimentation, are adopted according to Table IV. From the specifications, the magnitude of the output voltage relative to the input voltage, can be verified where a gain greater than seven times is obtained. Through the output voltage value, it is expected that capacitors and semiconductors are subjected to 400 V, resulting in a fourfold reduction relative the dc-link voltage.

#### A. Considerations for the Design of the Commutated Capacitors \( C_{i,k} \)

During the mathematical analysis, it was considered that the converter operates in the *no charge* mode. However, this operation mode is physically infeasible, due to it requiring high capacitance values. For practical implementation, it is desirable to operate the converter in the *partial charge* mode, since it leads to a good compromise between peak current and capacitance. It can be demonstrated that the performed analysis of the component current stress for operation in *no charge* mode yields to excellent accuracy also for the *partial charge* mode, and therefore, it can be used to design the converter and to predict its behavior.

To choose the capacitances of the commutated capacitors \( C_{i,k} \), it is necessary to take into account the parasitic resistances of the circuit. Nevertheless, for the sake of simplicity, in this paper, only the resistor \( r_{C3} \) of the capacitor \( C_3 \) is considered. However, other parasitic resistances, such as the switch resistances, can affect and define the converter operation mode. Small values of parasitic resistance and capacitance not only increase the peak current, during the commutation, but also the losses in both semiconductors and capacitors. Therefore, once selected the switching frequency, one should choose a combination of capacitances and parasitic resistances that provide at least a *partial charge* mode.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Power, ( P_o )</td>
<td>2500</td>
<td>W</td>
</tr>
<tr>
<td>Input Voltage, ( v_{I_{\text{rms}}} )</td>
<td>220</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage, ( V_o )</td>
<td>1600</td>
<td>V</td>
</tr>
<tr>
<td>Switching frequency, ( f_s )</td>
<td>90</td>
<td>kHz</td>
</tr>
<tr>
<td>Inductance, ( L_b )</td>
<td>300</td>
<td>( \mu\text{H} )</td>
</tr>
<tr>
<td>Capacitance, ( C_{i,k} ), ( k \in {A, B} )</td>
<td>60</td>
<td>( \mu\text{F} )</td>
</tr>
<tr>
<td>Parasitic resistance, ( \tau_{C3} ), ( k \in {A, B} )</td>
<td>300</td>
<td>m( \Omega )</td>
</tr>
<tr>
<td>Capacitance, ( C_{o,k} ), ( k \in {A, B} )</td>
<td>470</td>
<td>( \mu\text{F} )</td>
</tr>
</tbody>
</table>
From the specifications listed in Table IV, the time constant of the simulation results can be determined. Therefore

\[ RC = r_{C3} \cdot C_{3,i} = 300 \, \text{mΩ} \cdot 60 \, \mu\text{F} = 18 \, \mu\text{s} > \frac{1}{90} \, \text{kHz}. \]  

(16)

From (16), it can be verified that the converter operates on the partial-charge mode.

B. Simulation Results

The simulation results of the voltages across the capacitors \( C_{i,A} \), input current \( i_g \), and switched terminal voltage \( v_{ao} \), are shown in Fig. 9. It can be observed that the converter processes sinusoidal current, performing the operation as PFC. Also, the voltage of the switched terminals of converter \( v_{ao} \), has three distinct levels \( \{+V_o/4, 0, -V_o/4\} \). In addition, the ripple voltage of the capacitors around the average value can be seen in the same figure.

The current flowing through capacitors \( C_{i,k} \) and switches \( S_{j,A}, i \in \{1, 2, 3\}, k \in \{A, B\}, j \in \{1, 2\} \) are shown in Fig. 10. The displayed details of the current during one switching cycle are shown, where one can see that the converter operates in partial charge mode.

C. Experimental Results

In order to verify and validate the introduced concepts, a Type I prototype was built with the specifications contained in Table IV.

All diodes SiC technology were employed (IDH16S60C-Infineon) in order to avoid reverse recovery problems in the switches. The capacitors \( C_{i,k}, i \in \{1, 2, 3\}, k \in \{A, B\} \), film capacitors were employed (B32778G8606k 60uF 800V-Epcos) since they have low resistance and low parasitic inductance, which leads to a good performance in high frequency. The output capacitors \( C_{o,k} \) electrolytic technologies were already used (B43504-A9477-M 470 uF 450 V). For switches CoolMOS technology was employed (IPW65R080CFD 650 V-Infineon) because of their low switching losses. The digital signal processor TMS320F28335-DSP Texas instruments was used to implement the control strategy shown in Fig. 6.

The experimental results of the converter operating at rated condition are shown in Fig. 11. The waveform of the partial output voltages \( v_{op} \) and \( v_{on} \), input current \( i_g \), and switched terminal voltage \( v_{ao} \) are shown. It can be seen that the partial output voltages are perfectly balanced around 800 V, proving that the converter is able to regulate the output voltage. Another important result is the input current, where it can verify the operation as PFC. Also, the switched terminal voltage of the converter, alternating in the levels \( +400, 0, -400 \, \text{V} \), are shown, confirming the three-level operation.

The voltage across the capacitors \( C_{1,A} \) and \( C_{2,A} \), input current \( i_g \), and switch current on the \( S_{2,A} \) are shown in Fig. 12. It is observed that the voltages of the capacitors are equalized around 400 V. All semiconductors are subject to these voltages, and so, it is important to be equalized. The current flow through in the switch was measured with the use of a Rogowski probe (CWT015 PEM). The measurement of current...
in switched-capacitor circuits is critical since it cannot insert loops in the circuit, otherwise it can change the parasitic inductance and consequently, the operation of the converter. The probe used has an inferior widthband of 116 Hz, attenuating the frequency of 60 Hz present in the current of switch. Because of this fact, the current has a low frequency oscillation caused by the probe (see Fig. 12); however, it may be ignored for analysis.

Fig. 13 shows the behavior of partial and dc-link voltages, input current and voltage grid during a disturbance in the output load. It can be seen that the voltages after the step-up returns to the rated value and are equally balanced.

In Fig. 14, the behavior of the voltage across the capacitors \( C_{1,k} \) during a disturbance in the output load is shown. The voltages remain balanced and close to the rated value even after the disturbance. As a consequence, high peak currents are avoided in the capacitors during the switching, when two capacitors are connected in parallel.

In order to quantify the losses, tests of efficiency of the proposed structure were performed, employing the power analyzer Yokogawa WT500. The tests were carried out using the converter operating for various load ranges. To evaluate the power losses with the frequency variation, tests were performed at frequencies from 50 to 90 kHz in steps of 10 kHz. The efficiency curves are shown in Fig. 15. In the figure, it can be seen that the efficiency increases with decreasing frequency, where the maximum efficiency was 97.91% at 50 kHz. Another important aspect is that the efficiency curve remains above 96% for the entire load range measurement, which proves the high performance of this kind of structure.

The curve losses of Type I as a function of output power, for two frequencies, are shown in Fig. 16. One can observe that the losses are represented by quadratic equations, which is described by three coefficients, as proposed by [35].

V. EXTENSION OF THE STAGES AND GENERALIZATION

The proposed family has a diode–capacitor multiplier cell with four stages. However, this cell can be extended to \( n \) stages so that the voltage gain can be expanded. In Fig. 17, two generic cells with the extension of stages are shown. The cells are named cell A and cell B. Each cell has a subcell switching, which can be reconfigured generating three converters. The A cell can produce the converters Type I—realization I, Type II—realization II, and
The proposed converters have three-level operation and low number of switches. All switches are subjected to one-fourth of the output voltage, yielding low switching losses. Also, due to the reduced number of semiconductors in the path of current, the converters have low conduction losses. In addition, the simulation and experimental results show that the family has input current with low harmonic distortion and regulated output voltage. Through the experimental results, it was shown that the family has high efficiency, where it was observed that the Type I reached maximum efficiency of 97.91%.

In summary, the proposed converters are suitable for unidirectional applications where the output voltage must be greater than 1000 V, where conventional three-level converters do not exhibit good performance. The proposed family is a solution instead of employing passive voltage multipliers and five-level converters.

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REFERENCES


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