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Input-series and output-series connected modular single-switch flyback converter operating in the discontinuous conduction mode

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Abstract: This study proposes a modular isolated dc–dc converter, based on the input-series and output-series connection of flyback converters operating in discontinuous conduction mode, as an alternative to provide higher voltage capability for medium-voltage applications (1–10 kV), from low-voltage semiconductors and passive components. The proposed architecture allows the modular system to operate with a simplified control scheme thanks to an intrinsic voltage-balancing mechanism. The voltage-balancing mechanism is investigated by theoretical analysis, both for steady-state and dynamic operations. A small-signal ac modelling of the architecture is developed to design the total output-voltage controller. To experimentally verify the proposed technique, a laboratory prototype system with three single-switch flyback converters, with 3 kW output power, 600 V dc input and output voltages, and 40 kHz of switching frequency was built.

1 Introduction

High-frequency isolated dc–dc converters for low- and medium-voltage applications have been in much demand in the past years, for example, in medium voltage dc transmission [1], distribution [2, 3] systems, and in dc micro-grids [4]. Other applications, as renewable energy systems, auxiliary power supplies, and energy storage systems have also been employing medium static-voltage converters [5, 6].

Even though there is continuous progress in the high-voltage high-power fully controlled semiconductors [7, 8], new strategies are necessary to meet the voltage requirements of the systems, such as (a) series connection of power devices [9, 10], (b) multilevel topologies [11–14], and (c) modular converter [15–27]. Connecting devices in series is the direct way to reach higher nominal voltages; however, it makes fail to achieve high efficiency and high-power density. Although the multilevel converters are able to attempt the high-voltage requirements using low-voltages rating switches, their manufacture is not standardised and each application requires a new design. The modular converters provide standard and scalable design to meet different voltage specifications with reduced voltage across the switches. On the other hand, the equal power-distribution among the converters can be considered as a drawback.

The integration of modular power converters can be classified into four architectures on the basis of their connection forms, namely input-parallel output-parallel, input-parallel output-series, input-series output-parallel, and input-series output-series (ISOS) [21].

For high and medium voltages on both sides of dc–dc conversion, ISOS connection is the most suitable combination of modular power-system architecture [16]. The challenge of modular converters in ISOS connection (Fig. 1) is proper voltage-balancing among the modules. Depending on the topology and operation mode of the converter, the voltage-sharing can be achieved by an intrinsic voltage-balancing mechanism or by additional control loops. In [15], Giri Deshang *et al.* proposed a three-loop control scheme to achieve equal voltage sharing of two forward converters. An individual output voltage loop-control and an individual inner current loop-control are proposed to the two-transistor forward converter by Deshang *et al.* [24]. Wu and Guangjiang [26] propose a decentralised voltage sharing control strategy that each module requires a total output voltage loop and an input voltage loop. A duty cycle exchanging control, incorporating an individual output voltage loop and an inner current loop, is implemented by Deshang *et al.* [23] to achieve input and output voltages sharing for ISOS connected two phase-shifted-full bridge.

The ISOS converter based on the intrinsic voltage-balancing mechanism is more attractive for using the common-duty-ratio and share the same controller [16, 27]. Fernandez *et al.* [20] and Merwe and Mouton [19] suggest that the stable operation in ISOS systems is provided by the losses. The intrinsic voltage-balancing mechanism is not natural to all the converters, thus it has to be checked for each structure.

This paper aims to present the self-balance of the input and output voltages across the individual modules in discontinuous conduction mode (DCM) operation, without voltage loop-control scheme, as an attribute of the single-switch flyback converter in ISOS connection. This topology is proposed as an alternative to the previous modular converters for lower power applications.

2 Proposed connection and theoretical analysis

2.1 Proposed ISOS connection based on the flyback converters operating in DCM

The circuit of the proposed connection is shown in Fig. 1. A key advantage of ISOS-connected modular flyback converters in DCM is its ability to operate with a common pulse width modulator (PWM); thanks to the natural voltage-balancing mechanism. To clarify the choice of DCM operation as the required condition to

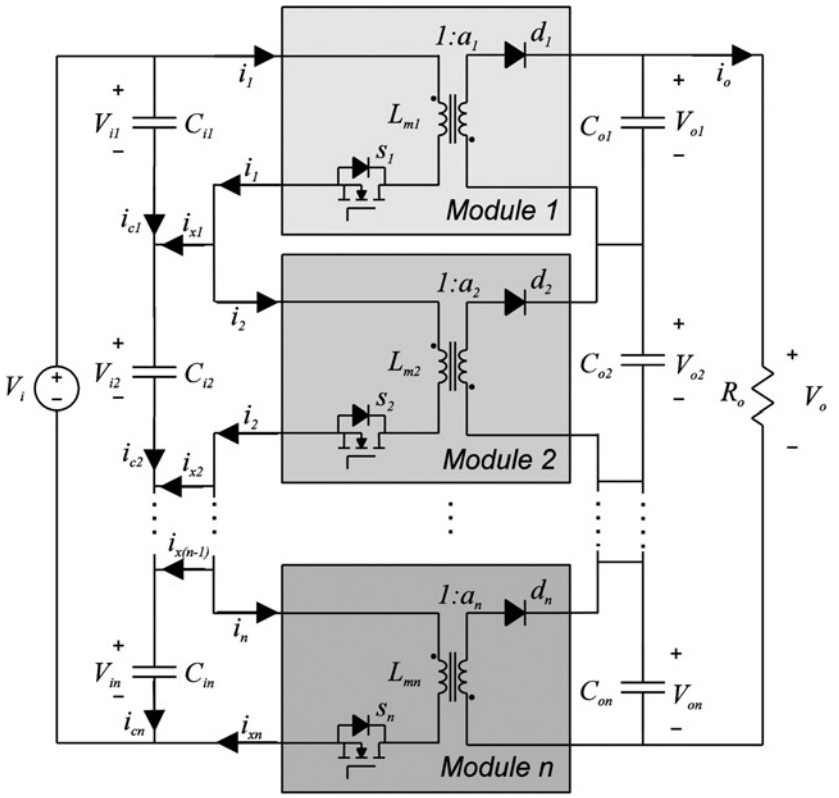

Fig. 1 *Flyback converters in ISOS connection*

achieve voltage-sharing between the modules, the well-known output characteristics of the flyback converter will be included in this study.

2.2 Static output characteristics

The ideal flyback converter operating in the DCM has three topological stages in a switching period, which are represented by the equivalent circuits presented in Fig. 2*a*. The corresponding waveforms are shown in Fig. 2*b*.

Considering the magnetising inductance voltage and diode current presented in Fig. 2*b*, the expressions

$$\frac{V_{\mathrm{i}} \times D}{f_{\mathrm{s}}} = a \times V_{\mathrm{o}} \times t_2 \tag{1}$$

and

$$I_{\mathrm{o}} = I_{D\mathrm{med}} = \frac{a \times V_{\mathrm{i}} \times D \times t_2}{2 \times L_{\mathrm{m}}} \tag{2}$$

are obtained. The duty cycle (D) is defined as

$$D = \frac{t_1}{T_S} \tag{3}$$

By algebraic manipulation of (1) and (2), the dc voltage ratio of the converter in DCM operation (G_{DCM}) is derived and represented as follows

$$G_{\mathrm{DCM}} = D^2 \times \frac{V_{\mathrm{i}}}{2 \times L_{\mathrm{m}} \times f_{\mathrm{s}} \times I_{\mathrm{o}}}. \tag{4}$$

Expression (4) can be rewritten as

$$G_{\mathrm{DCM}} = \frac{D}{\overline{I_{\mathrm{o}}}}. \tag{5}$$

where $\overline{I_{\mathrm{o}}}$ is the per-unit current given by the following equation

$$\overline{I_{\mathrm{o}}} = \frac{2 \times L_{\mathrm{m}} \times f_{\mathrm{s}} \times I_{\mathrm{o}}}{D \times V_{\mathrm{i}}}. \tag{6}$$

As it is well known, the dc voltage ratio in continuous conduction mode (CCM) operation (G_{CCM}) is defined as

$$G_{\mathrm{CCM}} = a \times \frac{D}{1 - D} \tag{7}$$

The boundary between DCM and CCM operation is given by the following equation

$$G_{\mathrm{DCM}} = G_{\mathrm{CCM}} \tag{8}$$

or

$$D = 1 - \overline{I_{\mathrm{o}}} \tag{9}$$

From (5), (7), and (9), the output characteristics of the flyback converter is plotted, as shown in Fig. 3.

A slight difference in the parameters of the converters that compose the module sets different quiescent operation point to each module. In the case of CCM operation, a difference in the quiescent operation points among the modules results in different current ratios to each module. Different input- and output-current ratios yield an unbalanced voltage at input and output port of each module that results in an unstable operation.

On the other hand, the drop-voltage characteristic (loss-free resistor behaviour) from the DCM operation curves in Fig. 3 makes each module equalise the quiescent operation point according to the load current, even under slight differences in the parameters, prompting the system to equilibrium.

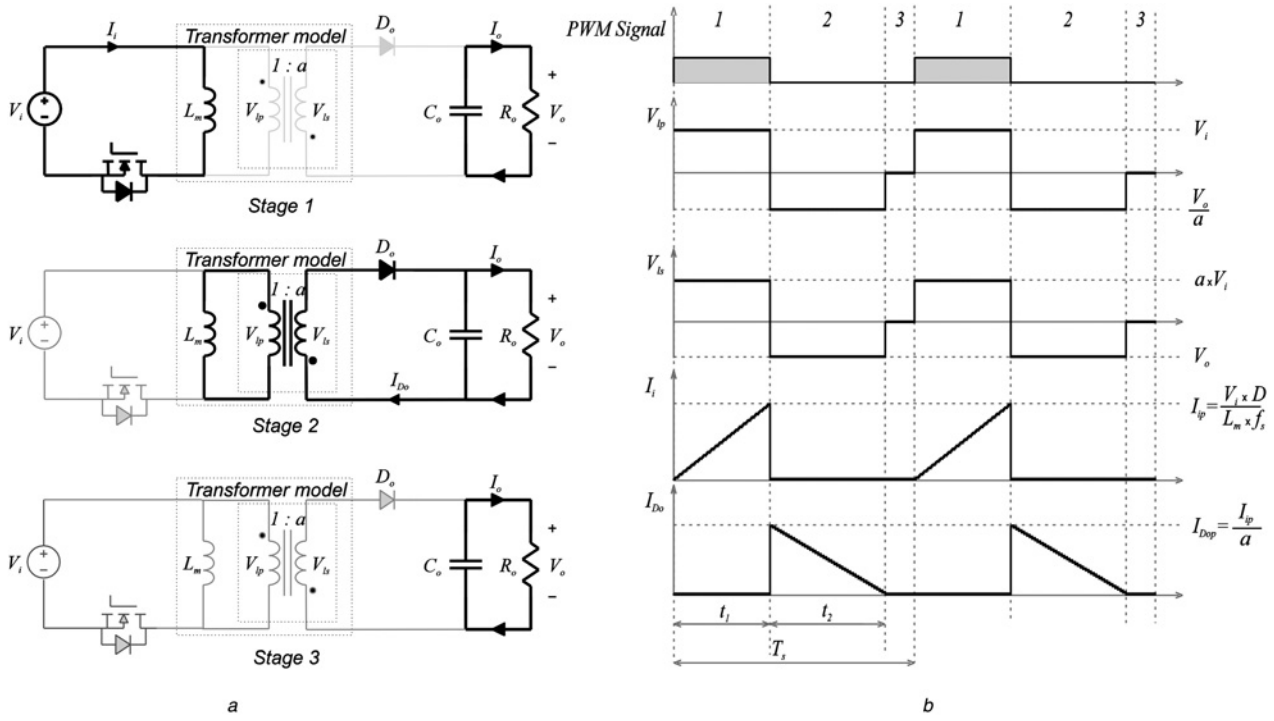

Fig. 2 *Flyback converter in DCM operation*

a Equivalent circuits for a switching period
b Main waveforms used for analysis

2.3 Input-voltage analysis in DCM operation

The input-voltage balance in ISOS connection of the flyback converters in DCM operation is analysed by the simplified circuit shown in Fig. 1.

An unbalancing input voltage between two adjacent modules causes the circulation of unequal input currents in these modules designated by i_x

$$\begin{aligned} i_{x1} &= i_1 - i_2 \\ i_{x2} &= i_2 - i_3 \\ &\vdots \\ i_{x(n-1)} &= i_{(n-1)} - i_{(n)} \end{aligned} \quad . \tag{10}$$

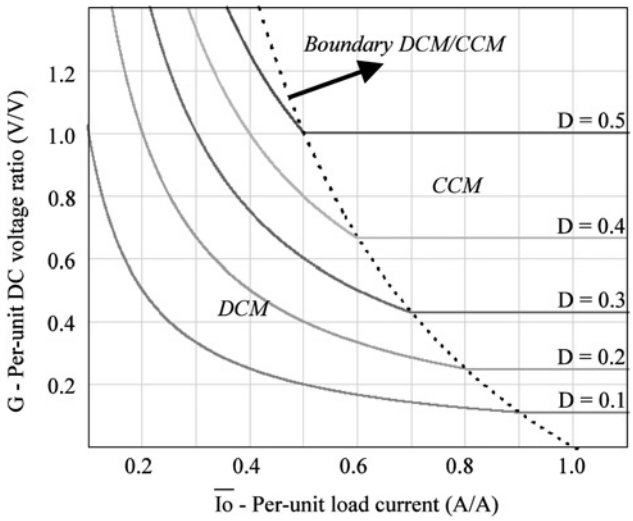

Fig. 3 *Static output characteristics of the flyback converter*

To simplify the analysis, the following parameters are considered to be identical

$$\begin{aligned} L_{\mathrm{m1}} = L_{\mathrm{m2}} = \cdots = L_{\mathrm{m}(n)} = L_{\mathrm{m}} \\ C_{\mathrm{i1}} = C_{\mathrm{i2}} = \cdots = C_{(\mathrm{in})} = C_{\mathrm{i}} \\ D_1 = D_2 = \cdots = D_{(n)} = D \end{aligned} \quad . \tag{11}$$

The average values of the input current on each module can be derived from the waveform of current i_i shown in Fig. 2*b*, and are given as

$$\begin{aligned} i_1 &= \frac{V_{\mathrm{i1}} \times D^2}{2 \times L_{\mathrm{m}} \times f_{\mathrm{s}}} \\ i_2 &= \frac{V_{\mathrm{i2}} \times D^2}{2 \times L_{\mathrm{m}} \times f_{\mathrm{s}}} \\ &\vdots \\ i_n &= \frac{V_{\mathrm{in}} \times D^2}{2 \times L_{\mathrm{m}} \times f_{\mathrm{s}}} \end{aligned} \tag{12}$$

Substituting (12) in (10) yields

$$i_{x(n-1)} = \left(V_{\mathrm{i}(n-1)} - V_{\mathrm{i}(n)}\right) \times \frac{D^2}{2 \times L_{\mathrm{m}} \times f_{\mathrm{s}}}. \tag{13}$$

A disturbance in the input voltage (ΔV_{i}) is introduced with the aim of analysing the natural voltage-balance mechanism. The input voltage

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on each module is represented by the following equation

$$\begin{aligned} V_{\mathrm{i}1} &= \frac{V_{\mathrm{i}}}{n} + k_1 \cdot \Delta V_{\mathrm{i}} \\ V_{\mathrm{i}2} &= \frac{V_{\mathrm{i}}}{n} + k_2 \cdot \Delta V_{\mathrm{i}} \\ &\vdots \\ V_{\mathrm{in}} &= \frac{V_{\mathrm{i}}}{n} + k_{(n)} \cdot \Delta V_{\mathrm{i}} \end{aligned} \tag{14}$$

The constants k_n in (14) define the initial fraction of voltage disturbance that appears on each input-voltage module from the total positive disturbance (V_{i}). To meet Kirchhoff's voltage law, the sum of disturbance voltages on the input of each module is equal to zero. Hence

$$V_{\mathrm{i}1} + V_{\mathrm{i}2} + \ldots + V_{\mathrm{i}(n)} = V_{\mathrm{i}} \tag{15}$$

and

$$\left(k_1 + k_2 + \ldots + k_{(n)}\right) \times \Delta V_{\mathrm{i}} = 0. \tag{16}$$

Replacing (14) in (13) gives

$$i_{x(n-1)} = \left(k_{(n-1)} - k_{(n)}\right) \times \frac{\Delta V_{\mathrm{i}} \cdot D^2}{2.L_{\mathrm{m}} \cdot f_{\mathrm{s}}}. \tag{17}$$

The current $i_{x(n-1)}$ is shared between the capacitors upstream and downstream, as presented by the following equation

$$i_{x(n-1)} = i_{\mathrm{c}(n-1)} - i_{\mathrm{c}(n)}. \tag{18}$$

The currents through the capacitors of the last two modules are given by the following equation, respectively:

$$\begin{aligned} i_{\mathrm{c}(n-1)} &= C_{\mathrm{i}} \frac{\mathrm{d}V_{(n-1)}}{\mathrm{d}t} \\ i_{\mathrm{c}(n)} &= C_{\mathrm{i}} \frac{\mathrm{d}V_{(n)}}{\mathrm{d}t} \end{aligned}. \tag{19}$$

Replacing (14) in (19) results in

$$\begin{aligned} i_{\mathrm{c}(n-1)} &= k_{(n-1)} \times C_{\mathrm{i}} \frac{\mathrm{d}\Delta V_{\mathrm{i}}}{\mathrm{d}t} \\ i_{\mathrm{c}(n)} &= k_{(n)} \times C_{\mathrm{i}} \frac{\mathrm{d}\Delta V_{\mathrm{i}}}{\mathrm{d}t} \end{aligned}. \tag{20}$$

Replacing (17) and (20) in (18) gives

$$\frac{\mathrm{d}\Delta V_{\mathrm{i}}}{\mathrm{d}t} = -\frac{\Delta V_{\mathrm{i}} \times D^2}{2 \times L_{\mathrm{m}} \times f_{\mathrm{s}} \times C_{\mathrm{i}}}. \tag{21}$$

Applying the Laplace transform in (21) yields

$$s \times \Delta V_{\mathrm{i}}(s) - \Delta V_{\mathrm{i}}(0) = -\frac{D^2}{2 \times L_{\mathrm{m}} \times f_{\mathrm{s}} \times C_{\mathrm{i}}} \times \Delta V_{\mathrm{i}}(s) \tag{22}$$

or

$$\Delta V_{\mathrm{i}}(s) = \frac{\Delta V_{\mathrm{i}}(0)}{s + K}. \tag{23}$$

where the constant K is given by the following equation

$$K = \frac{D^2}{2 \times L_{\mathrm{m}} \times f_{\mathrm{s}} \times C_{\mathrm{i}}}. \tag{24}$$

Applying the final value theorem in (23) as presented by the following equation

$$\Delta V_{\mathrm{i}}(\infty) = \lim_{s \to 0} s \times \Delta V_{\mathrm{i}}(s) = \lim_{s \to 0} s \times \frac{\Delta V_{\mathrm{i}}(0)}{s + K} = 0 \tag{25}$$

makes it clear that disturbances go to zero, prompting the system to equilibrium.

The time evolution of the input voltage on each module is obtained by applying inverse Laplace transform in (23) and replacing the result in (14). The results obtained are written as

$$\begin{aligned} V_{\mathrm{i}1} &= \frac{V_{\mathrm{i}}}{n} + k_1 \times \Delta V_{\mathrm{i}}(0) \times \mathrm{e}^{-K \times t} \\ V_{\mathrm{i}2} &= \frac{V_{\mathrm{i}}}{n} + k_2 \times \Delta V_{\mathrm{i}}(0) \times \mathrm{e}^{-K \times t} \\ &\vdots \\ V_{\mathrm{in}} &= \frac{V_{\mathrm{i}}}{n} + k_{(n)} \times \Delta V_{\mathrm{i}}(0) \times \mathrm{e}^{-K \times t} \end{aligned}. \tag{26}$$

To verify the theoretical analysis, three modules of flyback converters in ISOS connection operating in the DCM were simulated. The voltage disturbance parameters are presented in Table 1. Other parameters are listed in Table 3.

The simulation results are illustrated in Fig. 4 and shown that there is a natural voltage-balancing in the input voltages, as proposed in (26).

From (26) it is defined the constant time as

$$\tau = \frac{1}{K} \tag{27}$$

or

$$\tau = \frac{2 \times L_{\mathrm{m}} \times f_{\mathrm{s}}}{D^2} \times C_{\mathrm{i}} \tag{28}$$

The time constant provides an insight into how strong is the voltage-balancing mechanism. It is observed in (28) that the parameters are concerning the drop-voltage behaviour obtained from (4).

2.4 Input-voltage analysis in CCM operation

To demonstrate that the intrinsic self-balancing mechanism is not achieved in CCM operation, an analysis of the input-voltage sharing is presented.

The idealised output characteristics behaviour of the flyback converter operating in the CCM is not affected by the load conditions as observed in Fig. 4 (losses are not involved). The operation point is established by the duty cycle (D) and the transformer turns ratio parameters (a). In the case of the converters in ISOS connection, a slight difference in these parameter sets unequal operation points to each converter. As a result, the voltages among the converters become unbalanced and the operation unstable.

The input-voltage analysis of two flyback converters in ISOS connection (Fig. 5) operating in the CCM is presented as follows:

Table 1 Voltage disturbance included for analysis of self-balancing mechanism

Symbol	Parameter	Value
$\Delta V_{\mathrm{i}}(0)$	total input voltage disturbance	100 V
K_1	weighting of disturbance in input voltage of module 1	0.3
K_2	weighting of disturbance in input voltage of module 2	0.2
K_3	weighting of disturbance in input voltage of module 3	−0.5

Table 2 Parameters for input-voltage analysis of flyback converters in ISOS connection operating in CCM

Symbol	Parameter	Value
V_i	total input voltage	400 V
$V_{i1,2}(0^+)$	initial input voltage of each module	200 V
L_m	magnetising inductance	65 μH
$D_{1,2}$	duty cycle of each module	0.35
$C_{i1,2}$	capacitor on input of each module	660 μF
a_1	transformer turns ratio module 1	1.5
a_2	transformer turns ratio module 2	1.4
f_s	switching frequency	40 kHz
i_o	output current	20 A

Table 3 Prototype design parameters and main components

Symbol	Parameter	Value
n	number of modules	3
V_i	total input voltage	600 V
V_o	total output voltage	600 V
L_m	magnetising inductance	65 μH
C_o	capacitor on output of each module	3 × 220 μF/250 V B43501-D2227 (Epcos)
C_i	capacitor on input of each module	3 × 220 μF/250 V B43501-D2227 (Epcos)
S	switches stress	450 V(peak)/5.2 A (average) IPW60R070C6 (Infineon)
d	diodes stress	467 V(peak)/4.7 A (average) STPSC806 (ST Microelectronics)
a	transformer turns ratio	1.33
f_s	switching frequency	40 kHz
P_o	output power	3 kW

Assuming that

$$\begin{aligned} a_1 &\neq a_2 \\ D_1 &\neq D_2 \end{aligned} \tag{29}$$

equation (7) can be rewritten as

$$\begin{aligned} G_{\mathrm{CCM1}} &= a_1 \times \frac{D_1}{1-D} \\ G_{\mathrm{CCM2}} &= a_2 \times \frac{D_2}{1-D} \end{aligned} \tag{30}$$

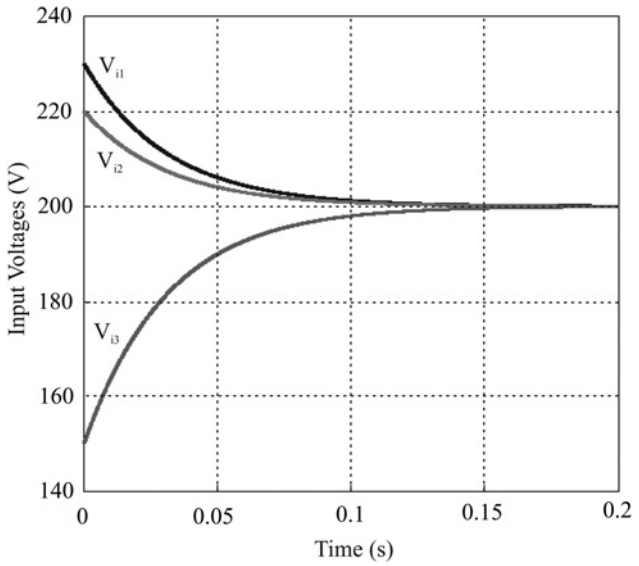

Fig. 4 *Input voltage response on each module from simulation results*

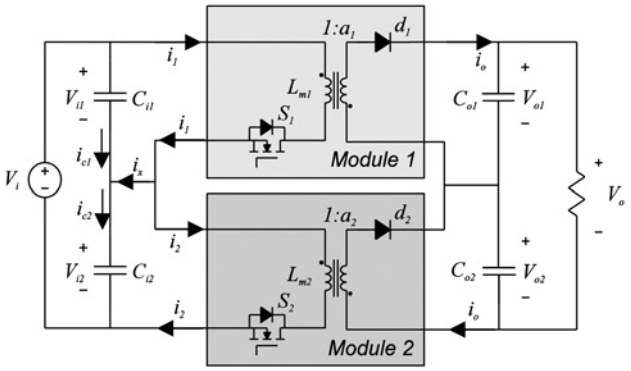

Fig. 5 *Two flyback converters in ISOS connection*

and resulting in

$$G_{\mathrm{CCM1}} \neq G_{\mathrm{CCM2}}. \tag{31}$$

The different operation points set unequal input average current to each module, as demonstrated in (32) and (33). The same output current (i_o) has been considered in both modules

$$\begin{aligned} G_{\mathrm{CCM1}} &= \frac{i_1}{i_o} \\ G_{\mathrm{CCM2}} &= \frac{i_2}{i_o} \end{aligned} \tag{32}$$

$$i_1 \neq i_2 \tag{33}$$

Replacing (30) in (32) yields

$$\begin{aligned} i_1 &= a_1 \times \frac{D_1 \times i_o}{1-D} \\ i_2 &= a_2 \times \frac{D_2 \times i_o}{1-D} \end{aligned} \tag{34}$$

The inequality value of i_1 and i_2 is given by the following equation

$$i_x = i_1 - i_2 \tag{35}$$

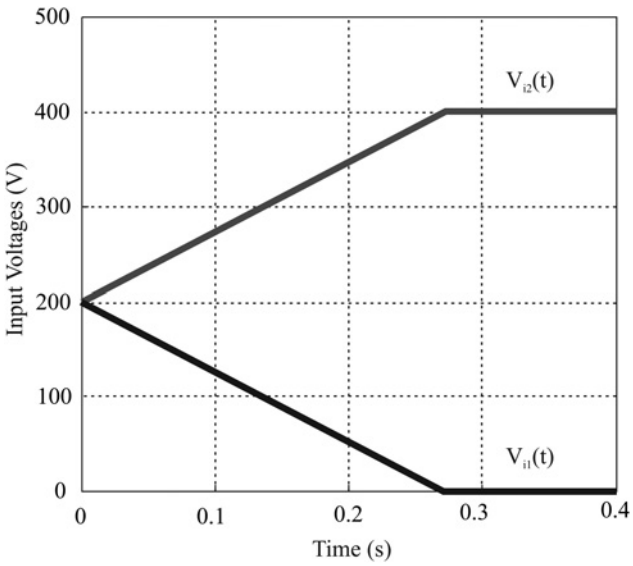

Fig. 6 *Input-voltage behaviour from simulation results*

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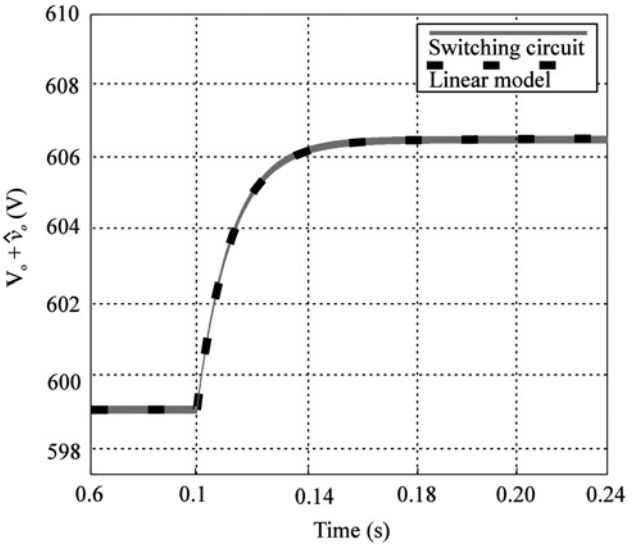

Fig. 7 *Open-loop response of output voltage to step change in duty cycle*

and substituting (34) in (35) results in

$$i_x = \left[\left(\frac{a_1 \times D_1}{1 - D_1}\right) - \left(\frac{a_2 \times D_2}{1 - D_2}\right)\right] \times i_o. \tag{36}$$

The current i_x is shared through the input capacitors as presented by the following equation

$$\begin{aligned} i_{c1} &= -\frac{i_x}{2} \\ i_{c2} &= \frac{i_x}{2} \end{aligned}. \tag{37}$$

The equations to the input-voltage capacitors are expressed as

$$\begin{aligned} v_{i1}(t) &= v_{i1}(o^+) - \frac{i_x}{2 \times C_{i1}} \times t \\ v_{i2}(t) &= v_{i2}(o^+) + \frac{i_x}{2 \times C_{i2}} \times t \end{aligned}. \tag{38}$$

Finally, the input-voltage behaviour of each module is found by substituting (36) in (38)

$$\begin{aligned} v_{i1}(t) &= v_{i1}(o^+) - \left[\left(\frac{a_1 \times D_1}{1 - D_1}\right) - \left(\frac{a_2 \times D_2}{1 - D_2}\right)\right] \times \frac{i_o}{2 \times C_{i1}} \times t \\ v_{i2}(t) &= v_{i2}(o^+) + \left[\left(\frac{a_1 \times D_1}{1 - D_1}\right) - \left(\frac{a_2 \times D_2}{1 - D_2}\right)\right] \times \frac{i_o}{2 \times C_{i2}} \times t \end{aligned} \tag{39}$$

Considering that $v_{c1}(t)$ and $v_{c2}(t)$ are clamped by the total input voltage, it can be concluded that with a slight difference in the transformer turns ratio or duty cycle, it makes the input voltage of one module increase to total input voltage and the input voltage of another module decrease to zero voltage, which results in an unstable operation.

The circuit of Fig. 5 (two modules in series connection) was simulated under a slight difference in the transformer turns ratio. The parameters to simulation are presented in Table 2. The results shown in Fig. 6 are in accordance with the present analysis and make clear that the voltage self-balance mechanism is not achieved in CCM operation.

2.5 Small-signal ac modelling in DCM operation

The control-to-output voltage transfer function for a single flyback converter operating in the DCM is obtained from the averaged switch modelling approach as presented in [28], and it is given by

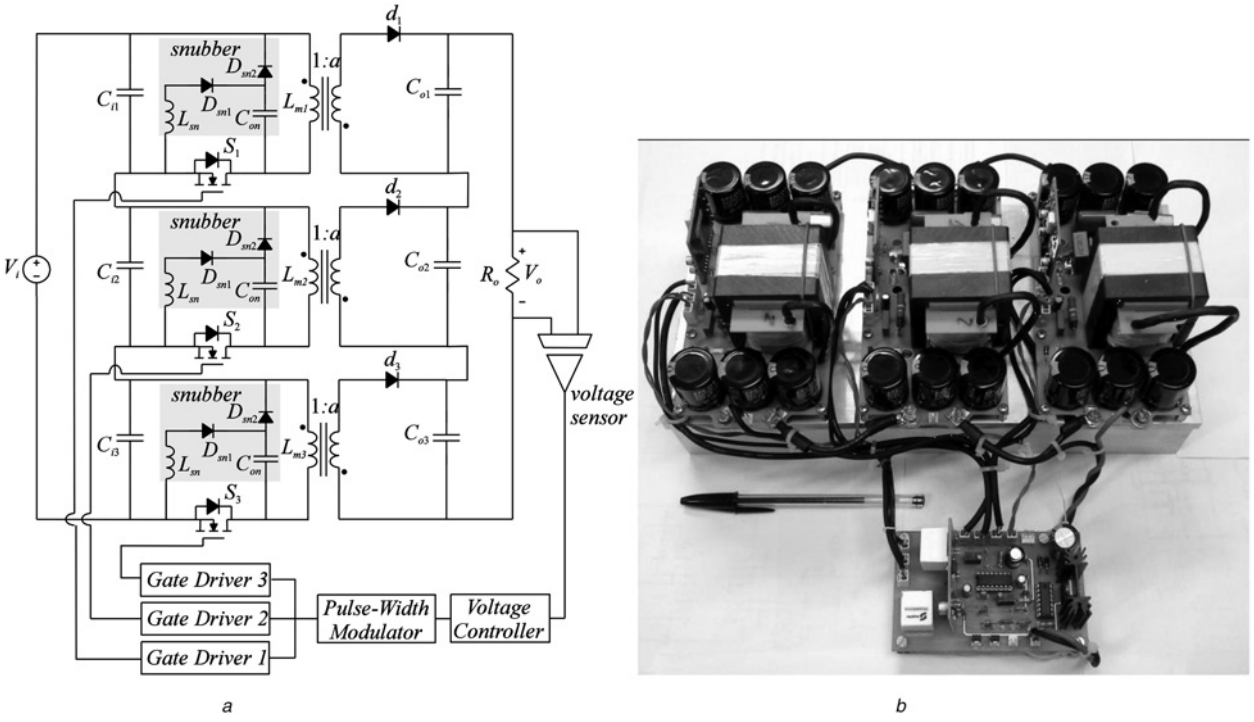

Fig. 8 *Implemented laboratory prototype*

a Simplified schematic including control blocks
b Photograph

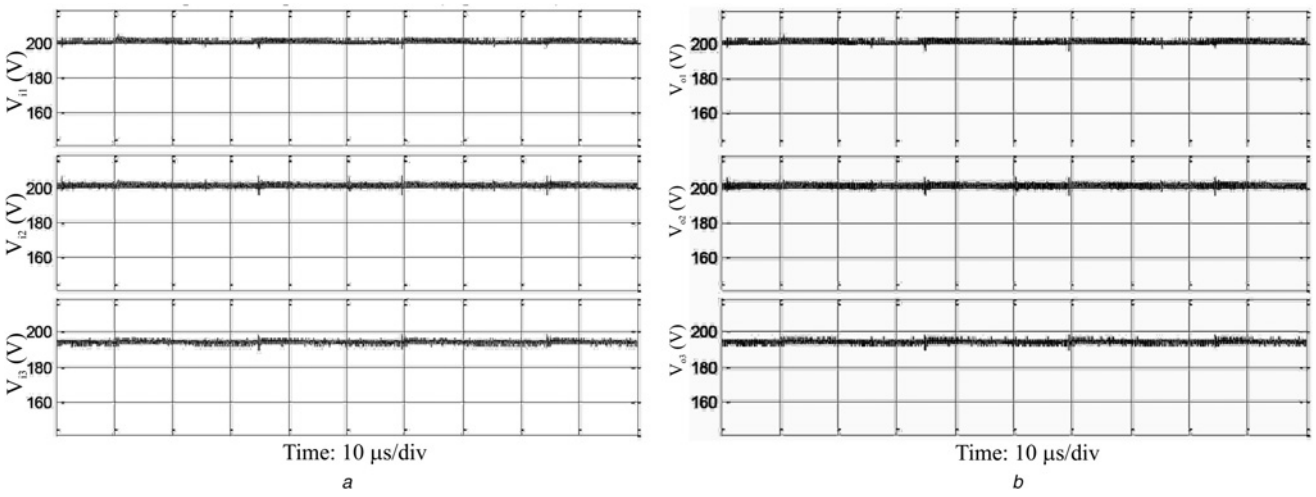

Fig. 9 *Voltage-sharing between the modules in steady-state operation*

a Voltages on input port of each module
b Voltages on output port of each module

Table 4 Measured parameters

Parameter	Module 1	Module 2	Module 3
number of modules	65.7 µH	65.8 µH	64.4 µH
input voltage	202.6 V	203.4 V	196.3 V
output voltage	200.7 V	201.5 V	196.9 V
diode voltage (peak)	499.4 V	486.1 V	481.9 V
diode current (average)	4.3 A	4.6 A	4.2 A
switch voltage (peak)	440.6 V	445.5 V	439.9 V
switch current (average)	5.4 A	5.6 A	5.4 A

the following equation

$$\frac{\hat{v}_o}{\hat{d}}\Big|_{\hat{v}_i=0} = \frac{(V_o/D)}{1 + s \times (R_o \times C_o/2)}. \tag{40}$$

In ISOS connection, the control-to-output voltage transfer function can be derived by similar analysis. The full dc output voltage is defined as the sum of the output voltages of all modules ($\hat{v}_{o1}, \hat{v}_{o2}, \ldots, \hat{v}_{on}$), and thus it is given by the following equation

$$\begin{aligned}\frac{\hat{v}_o}{\hat{d}}\Big|_{\hat{v}_i=0} &= \frac{\hat{v}_{o1}}{\hat{d}_1} + \frac{\hat{v}_{o2}}{\hat{d}_2} + \cdots + \frac{\hat{v}_{on}}{\hat{d}_n}\Big|_{\hat{v}_i=0} \\ \frac{\hat{v}_o}{\hat{d}}\Big|_{\hat{v}_i=0} &= \frac{(V_{o1}/D_1)}{1 + s(R_{o1} \times C_{o1}/2)} + \frac{(V_{o2}/D_2)}{1 + s(R_{o2} \times C_{o2}/2)} \\ &\quad + \cdots + \frac{(V_{on}/D_n)}{1 + s(R_{on} \times C_{on}/2)}\end{aligned}. \tag{41}$$

Finally, the control-to-output voltage transfer function obtained for DCM operation of flyback converters in ISOS connection is written as

$$\frac{V_o(s)}{D(s)} = \frac{(V_o/D)}{1 + s \times (R_o \times C_o/2 \times n)} \tag{42}$$

considering

$$\begin{aligned} V_{o1} = V_{o2} = \ldots = V_{o(n)} = V_o \\ R_{o1} = R_{o2} = \ldots = R_{o(n)} = R_o \\ C_{o1} = C_{o2} = \ldots = C_{o(n)} = C_o \\ D_1 = D_2 = \ldots = D_{(n)} = D \end{aligned}. \tag{43}$$

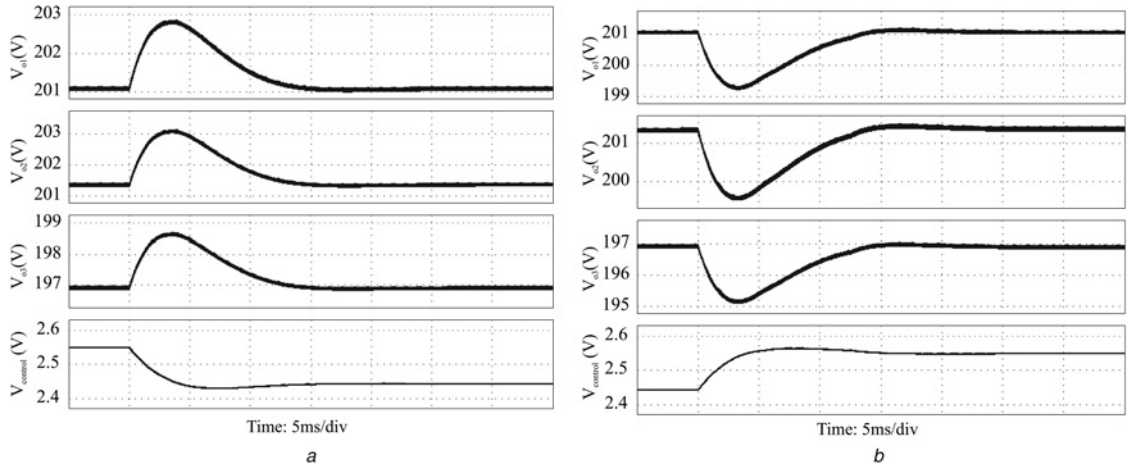

Fig. 10 *Load transient response*

a Step load from 100 to 76.5%
b Step load from 76.5 to 100%

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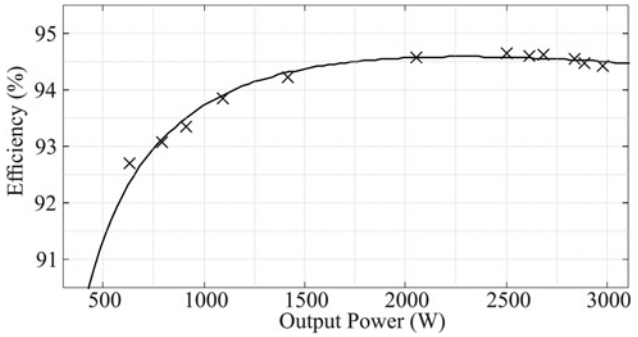

Fig. 11 *Measured efficiency of DCM flyback converter in ISOS connection with three modules*

Table 5 Theoretical losses and efficiency

Component	Losses
transformer	21,708 W
mosfet IPW60R070C6	85,356 W
diode STPSC806	68,238 W
total losses	175,302 W
efficiency	94.15%

To evaluate the obtained model, the circuit of Fig. 1 and the control-to-output transfer function (42) were simulated, considering a disturbance on the duty cycle and the number of modules equal to three ($n = 3$).

In Fig. 7, it is seen that the results with model (42) and the original circuit are very close, which validates the theoretical model. The parameters used for simulation are given in Table 3.

3 Experimental results

To experimentally evaluate the operation and analysis of the proposed connection, a prototype was designed and implemented regarding the specifications given in Table 3. A regenerative snubber circuit was included in the laboratory prototype to prevent over-voltages across the switches and reduce the commutation losses.

The total output voltage is controlled by a proportional integrative (PI) compensator with a filter whose transfer function is given by the following equation

$$C(s) = K_v \times \frac{s+z}{s \times (s+p)}. \tag{44}$$

The compensator was designed to meet a crossover frequency of loop gain at 120 Hz and the phase margin in 65°.

Fig. 8*a* shows the simplified schematic of prototype including the control blocks. A photograph of the implemented prototype is shown in Fig. 8*b*.

In Fig. 9*a*, a proper distribution of the input voltages can be observed among the modules. The total input voltage of 600 V was shared among the input voltages of each module (close to 200 V). Similar behaviour was obtained in output voltages, as predicted by the theoretical analysis.

Table 4 shows the main measured parameters. Differences in magnetising inductance among the modules do not cancel the self-balance characteristic of the structure; these only provide a slight difference in the voltages and currents, as seen in Table 4.

The dynamic responses for a step load from 100 to 76.5% are represented in Fig. 10*a*. The output-voltage controller sets the signal control ($V_{control}$) prompting the converter to the quiescent operation point. Similar results for a step load from 76.5 to 100% are presented in Fig. 10*b*. The curves of individual output voltages serve to prove that the balance of input and output voltages is also naturally achieved for dynamic operation without additional control.

The measured efficiency of the proposed connection is shown in Fig. 11 as a function of the output power, which reaches the maximum value, equal to 94.62% at 2.5 kW. At full power (3 kW), the efficiency was 94.30% and it is close to the theoretical efficiency presented in Table 5.

4 Conclusion

The modular ISOS connection of dc–dc flyback converters operating in the DCM was presented. A theoretical analysis enlightens the ability of the proposed architecture to provide self-balance of the input and output voltages across the individual modules. The voltage self-balance is achieved only in DCM operation; thanks to the drop-voltage behaviour observed in the output characteristics of the flyback converter. It was demonstrated by theoretical analysis that the CCM operation does not provide natural voltage-sharing.

In comparison with other dc–dc converter topology, particularly the full-bridge converter, the modular flyback converter is more suitable for lower power applications, just like the traditional topology (non-modular).

From the theoretical and experimental studies presented in this paper, the following conclusions can be drawn:

(i) Attempts to minimise the voltage stress across the switching devices succeeded;
(ii) Only a single PWM command to the switches is necessary;
(iii) The electrical circuit design of converters is standardised (flyback operating in DCM);
(iv) The total output voltage can be easily controlled by a PI controller;
(v) Efficiency matches with an isolated dc–dc converter;
(vi) It is an alternative to increase the voltage range of flyback converter applications.

All the predicted results have been fully verified with 600 V dc input and 600 V dc output voltages and 3 kW laboratory prototype.

5 References

1 Aboushady, A.A., Ahmed, K.H., Finney, S.J., *et al.*: 'Performance analysis of a new modular nano-crystalline core transformer based converter for medium voltage dc transmission applications'. Fifth IET Int. Conf. on Power Electronics, Machines and Drives (PEMD 2010), 2010, pp. 1–6
2 Prabhala, V.A.K., Baddipadiga, B.P., Ferdowsi, M.: 'DC distribution systems – an overview'. Int. Conf. on Renewable Energy Research and Application (ICRERA), 2014, 2014, pp. 307–312
3 Bathurst, G., Hwang, G., Tejwani, L.: 'MVDC – the new technology for distribution networks'. Eleventh IET Int. Conf. on AC and DC Power Transmission, 2015, pp. 1–5
4 Carminati, M., Grillo, S., Piegari, L., *et al.*: 'Ground fault analysis of low voltage DC micro-grids with active front-end converter'. Third Renewable Power Generation Conf. (RPG 2014), 2014, pp. 1–6
5 Daoud, M.I., Abdel-khalik, A.S., Elserougi, A., *et al.*: 'Medium voltage flywheel energy storage system employing dual three-phase induction machine with machine-side series-connected converters'. Seventh IET Int. Conf. on Power Electronics, Machines and Drives (PEMD 2014), 2014, pp. 1–6
6 Engel, S.P., Stieneker, M., Soltau, N., *et al.*: 'Comparison of the modular multilevel DC converter and the dual-active bridge converter for power conversion in HVDC and MVDC grids', *IEEE Trans. Power Electron.*, 2015, **30**, pp. 124–137
7 Glaser, J.S., Nasadoski, J.J., Losee, P.A., *et al.*: 'Direct comparison of silicon and silicon carbide power transistors in high-frequency hard-switched applications'. Twenty-Sixth Annual IEEE Applied Power Electronics Conf. and Exposition (APEC), 2011, 2011, pp. 1049–1056
8 Storasta, L., Rahimo, M., Haefner, J., *et al.*: 'Optimized power semiconductors for the power electronics based HVDC breaker application'. Proc. PCIM Europe 2015, Int. Exhibition and Conf. for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2015, pp. 1–7
9 Piazzesi, A., Meysenc, L.: 'Series connection of 3.3 kV IGBTs with active voltage balancing'. IEEE 35th Annual Power Electronics Specialists Conf., 2004, PESC 04, 2004, vol. 2, pp. 893–898
10 Ting, L., Zhengming, Z., Hualong, Y., *et al.*: 'Parameter design of a three-level converter based on series-connected HV-IGBTs', *IEEE Trans. Ind. Appl.*, 2014, **50**, pp. 3943–3954

11 Rodrigues, J.P., Mussa, S.A., Barbi, I., *et al*.: 'Three-level zero-voltage switching pulse-width modulation DC–DC boost converter with active clamping', *IET Power Electron.*, 2010, **3**, pp. 345–354
12 Deore, S.R., Darji, P.B., Kulkarni, A.M.: 'Switching function analysis of half- and full-bridge modular multi-level converters for HVDC applications', *IET Gener. Transm. Distrib.*, 2013, **7**, pp. 1344–1356
13 Babaei, E., Kangarlu, M.F., Sabahi, M.: 'Extended multilevel converters: an attempt to reduce the number of independent DC voltage sources in cascaded multilevel converters', *IET Power Electron.*, 2014, **7**, pp. 157–166
14 Nademi, H., Norum, L.: 'Analytical circuit oriented modelling and performance assessment of modular multilevel converter', *IET Power Electron.*, 2015, **8**, pp. 1625–1635
15 Giri, R., Ayyanar, R., Ledezma, E.: 'Input-series and output-series connected modular DC–DC converters with active input voltage and output voltage sharing'. Nineteenth Annual IEEE Applied Power Electronics Conf. and Exposition, 2004. APEC '04, 2004, 3, pp. 1751–1756
16 Bottion, A.J.B., Barbi, I.: 'Input-series and output-series connected modular output capacitor full-bridge PWM DC–DC converter', *IEEE Trans. Ind. Electron.*, 2015, **62**, pp. 6213–6221
17 Mohammadpour, A., Parsa, L., Todorovic, M.H., *et al*.: 'Series-input parallel-output modular-phase DC/DC converter with soft-switching and high-frequency isolation', *IEEE Trans. Power Electron.*, 2016, **31**, pp. 111–119
18 Qian, T., Lehman, B.: 'Buck/half-bridge input-series two-stage converter', IET *Power Electron.*, 2010, **3**, pp. 965–976
19 van der Merwe, J.W., du T Mouton, H.: 'An investigation of the natural balancing mechanisms of modular input-series-output-series DC–DC converters'. IEEE Energy Conversion Congress and Exposition (ECCE), 2010, 2010, pp. 817–822
20 Fernandez, C., Zumel, P., Sanz, M., *et al*.: 'Combination of DCM and CCM DC/DC converters for input-series output-series connection'. Twenty-Ninth Annual IEEE Applied Power Electronics Conf. and Exposition (APEC), 2014 , 2014, pp. 2054–2060
21 Sedaghati, F., Hossein Hosseini, S., Sabahi, M., *et al*.: 'Analysis and implementation of a modular isolated zero-voltage switching bidirectional dc–dc converter', *IET Power Electron.*, 2014, **7**, pp. 2035–2049
22 Sedaghati, F., Hosseini, S.H., Sabahi, M., *et al*.: 'Extended configuration of dual active bridge DC–DC converter with reduced number of switches', *IET Power Electron.*, 2015, **8**, pp. 401–416
23 Deshang, S., Kai, D., Xiaozhong, L.: 'Duty cycle exchanging control for input-series-output-series connected two PS-FB DC–DC converters', *IEEE Trans. Power Electron.*, 2012, **27**, pp. 1490–1501
24 Deshang, S., Zhiqiang, G., Tianmei, L., *et al*.: 'A general control strategy for input-series-output-series modular DC/DC converters', *IEEE Trans. Power Electron.*, 2014, **29**, pp. 3766–3775
25 Kiwoo, P., Zhe, C.: 'Control and dynamic analysis of a parallel-connected single active bridge DC–DC converter for DC-grid wind farm application', *IET Power Electron.*, 2015, **8**, pp. 665–671
26 Wu, C., Guangjiang, W.: 'Decentralized voltage-sharing control strategy for fully modular input-series-output-series system with improved voltage regulation', *IEEE Trans. Ind. Electron.*, 2015, **62**, pp. 2777–2787
27 Qiwei, L., Zijing, Y., Shuai, L., *et al*.: 'Research on voltage sharing for input-series-output-series phase-shift full-bridge converters with common-duty-ratio'. IECON 2011 – 37th Annual Conf. on IEEE Industrial Electronics Society, 2011, pp. 1548–1553
28 Erickon, R.W., Maksimovic, D.: 'Fundamentals of power electronics' (Springer, US, 2001, 2nd edn.)