A Three-Phase Multilevel Hybrid Switched-Capacitor PWM PFC Rectifier for High-Voltage-Gain Applications

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Abstract—In this paper, a three-phase multilevel power factor correction rectifier using the hybrid switched-capacitor concept is proposed. The converter is suitable for high-voltage-gain applications from conventional three-phase low-voltage sources. The three-level voltage operation reduces the weight and bulk of the magnetic devices. The main advantages of the proposed converter are low number of active switches, high voltage gain, sinusoidal currents, low voltage stress across all components, and simple control. Both steady-state and dynamic analyses are investigated. Experimental results for a 7500-W/220-V-to-1600-V laboratory prototype with maximum efficiency of 97.78% are presented and discussed.

Index Terms—High voltage gain, hybrid switched-capacitor, low voltage stress, power factor correction (PFC), three-level voltage, three-phase, voltage multiplier.

I. INTRODUCTION

APPLICATIONS that require high-voltage-gain converters are often reported in the specialist literature. These applications include lasers, radars, X-ray, and other medical equipment [1]–[3]. In these cases, the power flow is unidirectional and the conventional grid is the main source, being the load supplied through a high dc-link voltage. Because of this, a high-voltage ac–dc power conversion is necessary.

For low-power levels, single-phase voltage multiplier circuits are often employed due to robustness and simple operation [4]–[6]. With the increase of the power load, the use of three-phase converters becomes necessary. However, mechanisms should be provided to reduce the voltage stress across the components and increase the ac current quality.

In [3], a three-phase symmetrical multistage voltage multiplier has been presented. This converter merges three voltage multiplier cells connected to isolated three-phase voltage source to achieve high gain conversion. It has the advantage that all semiconductors are subjected to low voltage, which allows the operation with high dc-link voltage. As a drawback, the capacitors operate at the grid frequency, leading to an increase of the bulk and weight of the conversion system. Moreover, the ac currents have high harmonic distortion due to absence of active control.

Because of related problems, in [7], a three-phase step-up multiplier with a switching device is proposed. It comprises a three-phase diode bridge connected to a boost converter and a voltage multiplier cell. The voltage gain can be increased by just adding diode–capacitor cells. The active switch is subjected to low voltage and the capacitors operating at high frequency. In contrast, the ac currents do not have the shape of the input voltages; thus, the unitary power factor is not possible.

In order to increase the ac current quality, three-level pulse width modulation (PWM) rectifiers have become an interesting alternative to three-phase applications [8]–[13]. They feature high performance for power factor correction (PFC) operation, high efficiency, and high power density. On the other hand, these converters are suitable for low dc-link voltage (lower than 1000 V). To higher dc-link voltages, converters with four and five levels are more attractive [14], [15]. However, the number of active switches and voltage sensors is increased substantially, raising the cost and complexity of the system.

Recently, a three-phase-to-single-phase matrix converter with PFC operation has been proposed in [16]. The ac output voltage of the matrix converter is connected to a single voltage multiplier, from which a high voltage gain is achieved. Furthermore, the currents have sinusoidal shape, resulting in a power factor nearly unity. A drawback of this concept is the high number of active switches required for power conversion.

Due to troubles related to listed topologies, a three-phase multilevel PFC rectifier for high-voltage-gain applications is proposed in this paper. This new topology integrates a three-level boost PFC converter with a diode–capacitor cell, resulting in a hybrid concept1 with high-voltage-gain conversion and PFC operation, simultaneously. This paper is organized as follows. In Section II, a description of the operational stages is presented and discussed. In Section III, a steady-state analysis is derived. The control strategy and system modeling will be described in Section IV. Finally, in Section V, experimental results are presented in order to evaluate the performance and advantages of the proposed solution.

II. OPERATION PRINCIPLE OF THE PROPOSED CONVERTER

A. Features of the Proposed Converter

The proposed converter is shown in Fig. 1. The topology comprises six active switches,2 18 fast diodes, six slow diodes, and 12 capacitors. It presents the PFC operation and has gain twice of

1This terminology has been used in [17]–[20].

2In Fig. 1, the active switches are represented by insulated-gate bipolar transistors, but other switching devices such as MOSFETs, integrated-gate commutated thyristors can be used in the power circuit.
the conventional three-level rectifiers. All components are subjected to one-fourth of the output voltage \( V_o \), having, therefore, considerable reduction of the switching losses, enabling the use of low-voltage devices. The voltage across the capacitors \( C_{i,j}^k \), \( i \in \{1, 2, 3\}, j \in \{A, B\}, k \in \{a, b, c\} \), has the self-regulation ensured by the PWM modulator, and therefore, the use of the voltage sensors is not necessary for these capacitors. For the output voltage regulation, two voltage sensors are necessary. At switching terminals \( a, b, c \), three-level voltages can be generated leading to reduction of bulk of the magnetics devices, increasing the current quality and power density. The capacitors \( C_{o,j} \) are connected to load and they must meet hold-up time requirements.

B. Principle of Operation and Switching States

Through of the sign of the currents and state of the switches, the topological stages can be determined. In total, there are 25 possible states. In this paper, only six topological stages will be described. In Fig. 2, the switching states valid to \( i_{g,a} > 0 \), \( i_{g,b} < 0 \), \( i_{g,c} < 0 \), and \( i_{g,c} > i_{g,b} \) are depicted. For simplicity, the input ac voltage sources \( v_{g,k} \), \( k \in \{a, b, c\} \), inductors \( L_b \), and load resistance \( R_L \) are omitted in the figure.

In the following, the basic principle of operation of the three-phase hybrid PFC rectifier is explained based on some simplifying assumptions:

1) the converter operates in the steady state;
2) the voltage across the capacitors \( v_{C_{i,j}} \), \( v_{C_{1,j}} \), is ripple-free and approximately equal to \( \frac{V_o}{3} \);
3) the voltage \( v_{C_{3,j}} \) is simultaneously slightly higher than \( v_{C_{1,j}} \) and slightly lower than \( v_{C_{2,j}} \);
4) all components are ideal;
5) the grid voltages and input currents are assumed with sinusoidal shape, ripple-free, balanced, and same phase angle;
6) the converter operates in continuous conduction mode;
7) the capacitance of \( C_{o,j} \) is much larger than \( C_{i,j}^k \);
8) the converter operates in no-charge mode NC, definition given by Ben-Yaakov [21];
9) the switching frequency \( f_s \) should be much higher than the grid frequency \( f_g \). (Grid phase voltages are approximately constant within a pulse period.)

Basically, the principle operation of the proposed converter is similar to that of the converters proposed in [20], [22], and [23]. For example, in Fig. 2(a), when the switches \( S_{1,A}^o \), \( S_{2,A}^o \), and \( S_{2,A}^o \) are turned ON, the capacitor \( C_{1,A}^o \) is connected to capacitor \( C_{3,A}^o \) through the diode \( D_{1,A}^o \), where, as a result, \( C_{o,A}^0 \) transfers charge to \( C_{3,A}^o \). Simultaneously, the capacitors \( C_{3,B}^o \) and \( C_{3,B}^o \) are connected to the capacitor \( C_{1,B}^o \) by the switches \( S_{2,A}^o \) and \( S_{2,A}^o \). In other words, a switched-capacitor stage is performed [cf., Fig. 2(a)]. The phase voltages related to this stage are

\[
\begin{align*}
v_{a,o} &= 0 \\
v_{b,o} &= 0 \\
v_{c,o} &= 0.
\end{align*}
\] (1)

This topological stage will be called \( \nabla_0 \). Hence, the phase voltages, for this stage, will be mapped as

\[
\nabla_0 = (0, 0, 0).
\] (2)

When the switch \( S_{1,A}^o \) is turned OFF and the remaining switches are in the same previous conditions, the converter shifts its operation stage as shown in Fig. 2(f). In this situation, the storage energy in the inductor \( L_b \) is transferred to the capacitors \( C_{3,A}^o \) and \( C_{1,A}^o \). Thus, the capacitors \( C_{3,A}^o \) and \( C_{1,A}^o \) are connected to the same potential through the diodes \( D_{1,A}^o \) and \( D_{1,A}^o \). As a consequence, the generated voltages related to this topological stage are

\[
\begin{align*}
v_{a,o} &= + \frac{V_o}{4} \\
v_{b,o} &= 0 \\
v_{c,o} &= 0.
\end{align*}
\] (3)

where the combination of these voltages results in the following mapping:

\[
\nabla_5 = (1, 0, 0).
\] (4)

Another topological stage can be seen in Fig. 2(d). In this case, the switches \( S_{1,A}^o \), \( S_{2,A}^o \), and \( S_{3,A}^o \) are turned OFF. In this time interval, the stored energy in the inductor \( L_b \), corresponding to phase \( a \), is transferred to capacitors \( C_{3,A}^o \) and \( C_{2,A}^o \) and to the load. Simultaneously, the capacitors \( C_{3,B}^o \) and \( C_{3,B}^o \) are discharged by the currents \( i_{g,b} \) and \( i_{g,c} \), respectively. The switching state related to this particular stage is denoted by \( \nabla_3 \). The phase
Fig. 2. Topological stages of the proposed three-phase converter valid to $i_{g,a} > 0$, $i_{g,b} < 0$, $i_{g,c} < 0$, and $i_{g,c} > i_{g,b}$: (a) state $\mathbf{V}_0 = (0, 0, 0)$; (b) state $\mathbf{V}_1 = (0, -1, 0)$; (c) state $\mathbf{V}_2 = (0, -1, -1)$; (d) state $\mathbf{V}_3 = (1, -1, -1)$; (e) state $\mathbf{V}_4 = (1, -1, 0)$; (f) state $\mathbf{V}_5 = (1, 0, 0)$. 
TABLE I
SWITCHING STATES OF THE PROPOSED CONVERTER, VALID TO $i_{g,a} > 0$, $i_{g,b} < 0$, $i_{g,c} < 0$, and $i_{g,c} > i_{g,b}$

<table>
<thead>
<tr>
<th>Vector</th>
<th>Currents sign</th>
<th>Command</th>
<th>Phase voltages</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_0$</td>
<td>+ - -</td>
<td>ON</td>
<td>$v_{a,0}$</td>
</tr>
<tr>
<td>$V_1$</td>
<td>+ - -</td>
<td>ON</td>
<td>$v_{b,0}$</td>
</tr>
<tr>
<td>$V_2$</td>
<td>+ - -</td>
<td>ON</td>
<td>$v_{c,0}$</td>
</tr>
<tr>
<td>$V_3$</td>
<td>+ - -</td>
<td>ON</td>
<td>$v_{d,0}$</td>
</tr>
<tr>
<td>$V_4$</td>
<td>+ - -</td>
<td>ON</td>
<td>$v_{e,0}$</td>
</tr>
<tr>
<td>$V_5$</td>
<td>+ - -</td>
<td>ON</td>
<td>$v_{f,0}$</td>
</tr>
</tbody>
</table>

Thus, the switching state for this topological stage is

$$V_3 = (1, -1, -1).$$

The other switching stages have similar operation and, therefore, will not be explored herein. The topological stages shown in Fig. 2 are listed in Table I. The remaining voltage vectors, related to switching states, are not listed in the table, but they can be found by easily knowing the sign of the input currents and the state of the switches.

It can be noted in all operation stages that the maximum voltage stress on the each device is $V_g/4$. As previously mentioned, this feature enables the use of semiconductors with lower voltage ratings.

In order to illustrate the principle of the operation of the proposed converter, Fig. 3 shows the details of the behavior of the currents through the commutation capacitors, input inductors, and power switches, valid to NC operation mode. Details of the switching states sequence.

C. Modulation Strategy

The continuous modulation strategies used in conventional three-phase three-level PWM rectifiers may also be employed in the proposed converter, e.g., space-vector modulation variations. In this paper, for simplicity, the carrier-based SPWM strategy is considered. The PWM modulator scheme is shown in Fig. 5. The modulating signal $m_k$ is compared with the sawtooth signal $v_{carried}$. As a result, the PWM signals are generated to the switches $S_{1,A}$ and $S_{2,A}$, $k \in \{a, b, c\}$. Each switch operates during half cycle of the grid voltage, and it depends on the sign of the input currents [cf., Fig. 5].

In conventional unidirectional PWM rectifiers, the phase voltages $v_{k,o}$, $k \in \{a, b, c\}$, relative to node $o$, in the proposed converter depend not only on the switching state of the active switches, but also on the sign of the current corresponding to

![Fig. 3. Main waveforms of the currents flowing through the commutation capacitors, input inductors, and power switches, valid to NC operation mode. Details of the switching states sequence.](image)

![Fig. 4. Vectorial map of the three-level converter. (a) Space distribution of the switching states on the plan abc. (b) Representation of the projection of the switching states on the plan $\alpha\beta$.](image)
phase \( k \). Thus, the phase voltages of the converter are defined as

\[
v_{k,o} = \begin{cases} \frac{V_o}{4} \text{sign} \{i_{g,k}\}, & \text{if } S_{j,A}^k = \text{turned-off} \\ 0, & \text{if } S_{j,A}^k = \text{turned-on} \end{cases}
\]

(7)

where \( k \in \{a, b, c\}, \ j = 1 \) if \( \text{sign} \{i_{g,k}\} > 0 \) and \( j = 2 \) if \( \text{sign} \{i_{g,k}\} < 0 \).

The grid voltages and input currents are defined as

\[
v_{g,k} = V_{g, pk} \sin(\omega t + \phi_k)
\]

(8)

\[
i_{g,k} = I_{g, pk} \sin(\omega t + \phi_k)
\]

(9)

where \( V_{g, pk} \) and \( I_{g, pk} \) represent the peak grid voltage and peak input current, respectively.

Neglecting the voltage drop on the inductors \( L_o \), \( v_{g,k} \approx v_{k,o} \), the static gain can be derived from (7) as

\[
G = \frac{V_o}{v_{g,k}} = \frac{4}{(1 - d_k)}.
\]

(10)

The duty cycles are obtained by substituting (8) into (10). Thus

\[
d_k = 1 - 2M \left[ \sin(\omega t + \phi_k) \right] \quad k \in \{a, b, c\}
\]

(11)

where \( M \) and \( \omega t \) represent the modulation index and angular frequency of the grid, respectively. The angle \( \phi_k \) corresponds to \( \phi_a = 0 \text{ rad}, \ \phi_b = -\frac{2\pi}{3} \text{ rad}, \ \phi_c = \frac{2\pi}{3} \text{ rad} \). The modulation index \( M \) is defined as

\[
M = \frac{4 \cdot V_{g, pk}}{V_o}.
\]

(12)

The modulating signal \( m_k \) and duty cycle \( d_k \) are related by \( d_k = \frac{m_k}{V_{g, pk}} \), where \( V_{g, pk} \) denotes the peak of the sawtooth signal.

The maximal utilization of the output voltage can be achieved with the use of space vector variations SV-PWM, such as reported in [24], [25]. Furthermore, benefits concerning the power losses on the power switches, common-mode voltage, and total harmonic distortion (THD) line currents may be obtained with such techniques. However, these modulation methods will not be explored herein.

In Section IV-C, a zero-sequence signal will be added to the modulation signals \( m_k \) so as to accomplish the voltage balancing of the partial output voltages.

III. STEADY-STATE ANALYSIS

In this section, some issues regarding the design and the practical realization of the proposed unidirectional hybrid rectifier will be discussed. The assumptions adopted in the previous section are also valid in this section.

A. Current Stresses

For simplicity, the current stresses on the components of the topology can be extracted considering only a single-phase cell. Thus, there are two operation stages.

The instantaneous currents flowing through the components, corresponding to first and second operation stage of a single-phase cell, are listed as

\[
\begin{align*}
&\text{First operation stage} \\
&i_{C_{1,i}} = -\frac{i_g(1-d_k)}{T} - \frac{i_o}{T} \\
&i_{C_{2,i}} = \frac{i_o(1-d_k)}{T} \\
&i_{D_{2,i}} = -\frac{i_o}{T} \\
&i_{S_{1,i}} = \frac{i_g}{T} \\
&i_{D_{1,i}} = \frac{i_o}{T}
\end{align*}
\]

(13)

From (13), the rms and average current stress through the capacitors and semiconductors can be calculated. These expressions are determined by substituting (13) into (14) to following assumptions:

\[
\begin{align*}
&\{ \phi = 0 \land \delta = \frac{\pi}{3} \forall x \in \{S_{j,A}^k, D_{j,b}^k, C_{3,j}^k\} \} \\
&\{ \phi = \frac{\pi}{6} \land \delta = \frac{2\pi}{3} \forall x \in \{C_{1,j}^k, C_{2,j}^k\} \}, \text{ where} \\
in \{1, 2\}, \ j \in \{A, B\}, \text{ and } k \in \{a, b, c\}.
\end{align*}
\]

\[
\begin{align*}
&\left\langle x \right\rangle_{\text{avg}} = \frac{1}{T_x} \int_0^{T_x} x dt \\
&\left\langle x \right\rangle_{\text{rms}} = \sqrt{\frac{1}{T_x} \int_0^{T_x} x^2 dt}
\end{align*}
\]

(14)

The symbols \( \left\langle x \right\rangle_{\text{avg}} \) and \( \left\langle x \right\rangle_{\text{rms}} \) in (14), denote the average and rms value of \( x \), respectively, calculated within the time period \( T_x \), where \( x \) is the component semiconductor or capacitor in analysis. Similarly, \( I_{x,\text{avg}} \) and \( I_{x,\text{rms}} \) represent the average and rms value of \( x \) calculated within the grid period, respectively.

In Table II, analytical expressions to determine the average and rms values of the current stresses on the semiconductors, valid to SPWM modulation, are listed. In Table III, the rms
TABLE II

Summary of the Analytical Approximations for the Average and RMS Current Values of the Power Semiconductors:

\[ i \in \{1, 2\}, \quad j \in \{A, B\}, \quad k \in \{a, b, c\} \]

<table>
<thead>
<tr>
<th>Comp. (x)</th>
<th>(\langle x \rangle^{\text{avg}}_{I_x})</th>
<th>(I_x^{\text{rms}})</th>
<th>(\langle x \rangle^{\text{rms}}_{I_x})</th>
<th>(I_x^{m.s.})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\bar{S}_{1,j}^k)</td>
<td>(i_{s,k} \left(\frac{1}{2} + 1\right))</td>
<td>(\frac{I_{g,k}}{2} (8 - M \pi))</td>
<td>(i_{s,k} \left(\frac{1}{2} - d\right))</td>
<td>(2I_s \left(3 + \left(\frac{M}{1 - M^2}\right)\right))</td>
</tr>
<tr>
<td>(D_{1,j}^k)</td>
<td>(i_{s,k} \left(\frac{1}{2} + 1\right))</td>
<td>(\frac{I_{g,k}}{2} - M)</td>
<td>(i_{s,k} \left(\frac{1}{2} - d\right))</td>
<td>(\frac{1}{3} \left(3 + 12 \left(\frac{M}{1 - M^2}\right)\right))</td>
</tr>
<tr>
<td>(D_{2,j}^k)</td>
<td>(i_{s,k} \left(\frac{1}{2} + 1\right))</td>
<td>(\frac{I_{g,k}}{2} - M)</td>
<td>(i_{s,k} \left(\frac{1}{2} - d\right))</td>
<td>(\frac{1}{3} \left(3 + 12 \left(\frac{M}{1 - M^2}\right)\right))</td>
</tr>
<tr>
<td>(D_{3,j}^k)</td>
<td>(i_{s,k} \left(\frac{1}{2} + 1\right))</td>
<td>(\frac{I_{g,k}}{2} - M)</td>
<td>(i_{s,k})</td>
<td>(\frac{1}{3} \left(3 + 12 \left(\frac{M}{1 - M^2}\right)\right))</td>
</tr>
</tbody>
</table>

TABLE III

Analytical Approximations for the RMS Current Values of the Capacitors:

\[ i \in \{1, 2\}, \quad j \in \{A, B\}, \quad k \in \{a, b, c\}, \gamma = \frac{M + \sqrt{\frac{1}{1 - M^2}}}{\sqrt{1 - M^2}}, \lambda = \frac{\sqrt{M + \sqrt{\frac{1}{1 - M^2}}} + 1}{\sqrt{1 - M^2}} \]

\[
I_{C,j}^{\text{rms}} = \frac{I_s}{3\sqrt{2}} \left(\frac{-\left(M^2 - 1\right)\left(M M + 2\left(3 \coth^{-1} \sqrt{\lambda}\right) + 3 \sqrt{3} + 4 \lambda + 12 \sqrt{3} + 8 \lambda + 24 \lambda - 16 \lambda^2\right)}{M^4 (M^2 - 1)}\right)
\]

\[
I_{C,j}^{\text{rms}} = \frac{I_s}{3\sqrt{2}} \left(\frac{-\left(M^2 - 1\right)\left(3 M + 2\left(3 \coth^{-1} \sqrt{\lambda}\right) + 3 \sqrt{3} + 4 \lambda + 12 \sqrt{3} + 8 \lambda + 24 \lambda - 16 \lambda^2\right)}{M^4 (M^2 - 1)}\right)
\]

\[
I_{C,j}^{\text{rms}} = \frac{I_s}{3\sqrt{2}} \left(\frac{-\left(M^2 - 1\right)\left(M M + 2\left(3 \coth^{-1} \sqrt{\lambda}\right) + 3 \sqrt{3} + 4 \lambda + 12 \sqrt{3} + 8 \lambda + 24 \lambda - 16 \lambda^2\right)}{M^4 (M^2 - 1)}\right)
\]

currents expressions of all capacitors of the proposed topology are listed. The analytical expressions in Tables II and III are obtained by solving (14) and are valid to the no-charge operation mode (NC). However, as shown in [20] and [21], they also provide good approximation to partial-charge mode (PC), and thus, its use can be applied in the dimensioning and thermal design of the power devices.

Fig. 6 illustrates the behavior of the rms current stresses on the main components of the proposed topology as a function of modulation index \(M\). The curves are normalized by average output current \(I_o\), where \(I_{x}^{\text{rms}} = I_x^{\text{rms}} / I_o, \quad x \in \{S_{1,A}, D_{1,j}^k, C_{i,j}^k, C_{o,j}^k\}, \quad k \in \{a, b, c\}, \quad j \in \{A, B\}\). It can be seen that the active switches \(S_{1,A}\) have current stress slightly larger than other devices. This is caused because \(S_{1,A}\) conducts at the same time the input current \(i_{s,k}\) and the current through the capacitor \(C_{i,j}^k, j = A \text{ if } i = 1 \text{ and } j = B \text{ if } i = 2\).

B. Selection of the Commutated Capacitors \(C_{i,j}^k\)

The current that flows through the commutation capacitors during the switched-capacitor stages is limited by the parasitic resistances present in the circuit. In general, the commutation capacitors \(C_{i,j}^k, i \in \{1, 2, 3\}, \quad j \in \{A, B\}, \quad k \in \{a, b, c\}\), should be chosen so that the combination between parasitic resistances and capacitance values results in the time constant \(\tau\) that ensures the partial-charge (PC) or no-charge (NC) operation. Usually, the NC mode is more convenient for mathematical analysis, because it simplifies the analytical expressions. However, it leads to high operation frequency and large capacitances [20], [26]. For practical applications, the PC mode is more suitable, because it results in a good tradeoff between switching frequency and capacitance value [26]. A simple rule for determining the capacitance value of \(C_{i,j}^k\) is to calculate the higher commutation time when two or more capacitors are in parallel and ensure that it is lower than \(\tau\). Thus

\[
\tau = r_p \cdot C_{i,j}^k > \frac{M}{I_s}
\]

where \(r_p\) represents the sum of all parasitic resistances present in the path of the current during the commutation between two or more capacitors in parallel, e.g., on-resistance of switches, series resistance of capacitors, PCB trace resistance, etc.
Fig. 6. Behavior of the normalized current stresses on the main components of the hybrid switched-capacitor PFC rectifier. The curves are plotted as a function of the modulation index $M$.

summary, there is need to know the $r_p$ value and subsequently to apply (15). Typically, this rule results in a capacitance value much lower than that of the output capacitors $C_{o,j}$, $j \in \{A, B\}$.

As previously mentioned, $r_p$ is intrinsic to the component and to the circuit layout. Therefore, any other resistance should not be inserted to the circuit, so as to change the operation mode of the converter. Although $r_p$ is necessary for the correct operation of the converter, due to its low resistance value, it has low impact on the overall system efficiency.

C. Output Capacitor $C_{o,j}$

Basically, the choice of the output capacitor must meet two requirements: energy storage and system stability. For the first statement, extreme cases are considered for simplicity. In [27], a hold-up time criterion is presented for the selection of output capacitors as

$$C_{o,j} = \frac{P_o}{V_o \cdot \Delta v_{o, dip}} \Delta t_{hold-up} \quad (16)$$

where a maximum output voltage dip $\Delta v_{o, dip}$ for the case of a failure of grid voltages during a time interval $\Delta t_{hold-up}$ should be set. Equation (16) can also be used in the proposed converter for choosing $C_{o,j}$, $j \in \{A, B\}$.

Another selection criterion for the capacitor value is meet the current stress. The rms current stress is very important for the capacitor selection because it determines the number of capacitors required to be connected in parallel and allows a correct thermal design. The rms current stress on the output capacitors is listed in Table III and can be used for the selection of $C_{o,j}$.

IV. Control Strategy and System Modeling

In principle, any control strategy used in conventional uni-directional three-level PWM rectifiers may be extended for the proposed converter. Due to simplicity and acceptance in the literature, the synchronous reference frame control strategy is employed in this paper. The control scheme and the block diagram are shown in Figs. 7 and 8, respectively. It can be seen that both are similar to schemes presented in [11], [12], [28], and [29], where input currents and input/output voltages are measured to guarantee PFC operation and partial output voltage regulation.

Because there is no connection between the midpoint $o$ and the neutral point $n$, only two currents are necessary to perform the control. The input currents $i_{g,a}$ and $i_{g,b}$ are converted to $i_d$ and $i_q$ components through the transformation block $abc/dq0$. The angle $\omega t$ is synchronized with the positive sequence of the grid voltages, and it is extracted from the PLL block. The grid voltages $v_{g,a}$ and $v_{g,b}$ are also used to feedforward loop of the duty cycles. The current error of the $d$- and $q$-axes is fed to their respective regulators $C_j(s)$, $j \in \{d, q\}$, where the output signals, added to feedforward signals $v_{ff,j}$, generate the modulation signals $m_d$ and $m_q$ [cf., Fig. 8].

Fig. 7. Synchronous reference frame control strategy applied to the proposed converter.

Fig. 8. Control block diagram of the proposed converter.
In order to establish the instantaneous output voltage \( v_o \) regulation, the partial output voltages \( v_{op} \) and \( v_{on} \) are measured. The dc-voltage loop generates the direct axis current reference \( i_d^* \) by means of the difference between \( v_o \) and voltage reference \( V_{o,r} \). The voltage error is fed to the proportional integral regulator \( G_d(s) \), where its output corresponds to \( i_d^* \). For the unity power factor, the quadrature axis current reference should be set to 0.

To ensure that the voltages \( v_{op} \) and \( v_{on} \) have the same average value, an additional dc-voltage balance control loop is required. As a result, a zero-axis modulating signal \( m_0 \) is generated. In Section IV-D, the zero-sequence component will be detailed where a transfer function will be derived.

### A. Current Transfer Function

Assuming that output capacitors \( C_{o,A} \) and \( C_{o,B} \) are modeling as voltage sources, then the dynamic influence of the capacitors \( C_{i,j}^{nk} \), \( i \in \{1, 2, 3\}, j \in \{A, B\} \), \( k \in \{a, b, c\} \) may be ignored\(^3\) for current loop control. Thus, the transfer functions related to \( d \) and \( q \) current components with their respective modulation signals in the frequency domain are

\[
G_d(s) = \frac{i_d(s)}{m_d(s)} = \frac{V_o}{4 \cdot s \cdot L_b} \quad (17)
\]

and

\[
G_q(s) = \frac{i_q(s)}{m_q(s)} = \frac{V_o}{4 \cdot s \cdot L_b} \quad (18)
\]

Assuming that there is no cross coupling between \( d \)- and \( q \)-axes, identical current regulators may be used.

### B. Output Voltage Transfer Function

For the output voltage control, only the dynamics of the capacitors \( C_{o,A} \) and \( C_{o,B} \) are considered. Thus, the linearized model related to small disturbance of output voltage \( \delta v_o \) with small disturbance of direct axis current \( i_d \) in the frequency domain is given by

\[
G_v(s) = \frac{\delta v_o(s)}{i_d(s)} = \frac{R_o \cdot V_d}{2 V_o} \cdot \frac{-L_i L_o \cdot s + 1}{C_o R_o \cdot s + 1} \quad (19)
\]

where \( V_d \) and \( I_d \) correspond to the rated value of the input voltage and input current in synchronism reference frame, respectively. The term \( C_o \) in (19) denotes the equivalent output capacitance, described by \( C_o = (C_{o,A}^{-1} + C_{o,B}^{-1})^{-1} \).

### C. Balancing of the Partial Output Voltages

In proposed converter, as well as in conventional three-level topologies, i.e. VIENN-Types, the partial output voltages do not have naturally equilibrium ensured and an active control mechanism becomes necessary. This unbalance is caused by the parametric imperfections in the components and the presence of local average current into midpoint \( o \). Therefore, the knowledge of the behavior of this current is required. In Fig. 9, a detail of the currents injected in midpoint \( o \) is shown. It can be seen that the midpoint current \( i_{mp} \) is formed by segments of the currents through the switches \( S_{i,A}^k \), \( i \in \{1, 2\} \), \( k \in \{a, b, c\} \).

The local average current injected in the midpoint \( \langle i_{mp} \rangle \) is described as

\[
\langle i_{mp} \rangle = \sum_{k=a,b,c} \langle i_{mp}^k \rangle \quad (20)
\]

where

\[
\langle i_{mp}^k \rangle = \frac{i_{g,k} \cdot (d_k + 1) \cdot \text{sign}(i_{g,k})}{2} \quad (21)
\]

The duty cycles are now defined as

\[
d_k = 1 - M \left| \sin(\omega t + \phi_k) + d_0 \right|, \quad k \in \{a, b, c\} \quad (22)
\]

where \( d_0 \) denotes the zero-sequence component of the duty cycles.

Substituting (9) and (22) into (20) results

\[
\langle i_{mp} \rangle \approx \frac{I_{pk}}{4} \cdot M \cdot \sin(3 \cdot \omega t) - d_0 \cdot I_{pk} \quad (23)
\]

Equation (23) shows that the average midpoint current can be controlled by \( d_0 \). The zero-sequence duty cycle \( d_0 \) is related to its respective modulation signal \( m_0 \) as \( m_0 = d_0/\sqrt{3} \). Thus, the zero-sequence modulation signal that leaves the average midpoint current to zero is

\[
m_0 = \frac{1}{4\sqrt{3}} \cdot M \sin(3 \omega t) \quad (24)
\]

### D. Transfer Function for the Balancing of the Partial Output Voltages

The unbalance voltage on the midpoint \( o \) is defined as

\[
\Delta v_{mp} = \frac{1}{2} (v_{op} - v_{on}) \quad (25)
\]

Since \( v_o = v_{op} + v_{on} \), then the partial output voltages are

\[
v_{op} = \frac{1}{2} v_o - \Delta v_{mp}, \quad v_{on} = \frac{1}{2} v_o + \Delta v_{mp} \quad (26)
\]

The unbalancing at midpoint \( o \) may also be written as

\[
d \frac{\Delta v_{mp}}{dt} = \frac{1}{2} \cdot C_{o,A,B} \langle i_{mp} \rangle \quad (27)
\]
Fig. 10. Implemented 7.5-kW multilevel unidirectional hybrid switched-capacitor three-phase PFC rectifier prototype.

### TABLE IV

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input RMS voltage, ( V_{\text{rms}} )</td>
<td>220 V</td>
</tr>
<tr>
<td>Output voltage, ( V_o )</td>
<td>1600 V</td>
</tr>
<tr>
<td>Grid freq., ( f_s/\text{switching freq.}, f_s )</td>
<td>60 Hz/80 kHz</td>
</tr>
<tr>
<td>Rated output power, ( P_o )</td>
<td>7500 W</td>
</tr>
</tbody>
</table>

### TABLE V

<table>
<thead>
<tr>
<th>Component</th>
<th>Description/value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input inductors, ( L_i )</td>
<td>300 ( \mu )H—Magnetics-77440A7</td>
</tr>
<tr>
<td>Commutation capacitors ( C_{i,j} )</td>
<td>60 ( \mu )F—Epcos—B32778G8606K</td>
</tr>
<tr>
<td>Output capacitors, ( C_{o,j} )</td>
<td>470 ( \mu )F—Epcos B43504-A9477-M</td>
</tr>
<tr>
<td>Semiconductor Device MOSFET</td>
<td>IPW65R080CFD—650 V/43 A</td>
</tr>
<tr>
<td>Semiconductor Device DIODE</td>
<td>IDH16S60C—600 V/16 A</td>
</tr>
</tbody>
</table>

where \( C_{o,A} = C_{o,B} = C_{o,B} \) is assumed. Substituting (23) into (27), and applying the Laplace transformation and extracting the first-order terms, the following relation is obtained:

\[
\Delta \bar{v}_{mp}(s) = \frac{\sqrt{3} \cdot I_{\text{sp}}}{2 \cdot C_{o,A,B}} \cdot \frac{1}{s} \tag{28}
\]

where \( \Delta \bar{v}_{mp}(s) \) and \( \bar{m}_0(s) \) denote small disturbances on the unbalance voltage and zero-sequence signal modulation, respectively.

### V. EXPERIMENTAL RESULTS

In order to verify and validate the introduced concept, a 7.5-kW laboratory prototype has been designed and built, as shown in Fig. 10. The main specifications are given in Table IV. A list of the employed semiconductor devices and passive components is given in Table V. With the intention of avoiding reverse recovery problems, SiC technology for all diodes was employed. For the commutation capacitors \( C_{i,j}, i \in \{1, 2, 3\}, j \in \{A, B\}, k \in \{a, b, c\} \), polypropylene technology was adopted. This technology was employed because it has low parasitic inductance and low intrinsic resistance. The choice of the capacitance values and parasitic resistance values of these capacitors follows the approach presented in Section III-B, such that the PC mode was ensured. The output capacitors \( C_{o,j} \) were selected to meet hold-up time requirements, and because of this, electrolytic technology was used.

Both modulation and control algorithms were realized with the floating point digital signal controller TMS320F28335 DSP Texas instruments. Two input currents \( \{i_{g,a}, i_{g,b}\} \) and four voltages \( \{v_{g,a}, v_{g,b}, v_{op}, v_{om}\} \) were measured by means of Hall effect sensors. The tests were carried out with resistive load.

The performance of some of the main waveforms of the implemented proposed converter operating in steady state and at rated power can be seen in Fig. 11. It is shown that the input currents \( i_{g,k}, k \in \{a, b, c\} \), present sinusoidal shape with low distortion. Small glitches on the currents \( i_{g,k} \) can be seen. These glitches are caused by discontinuity in the modulation signals, generated by the change in the signal of the currents. This phenomenon can be improved with redesign of the controllers or use of another control strategy. In the same figure, the line-to-line voltage terminal of the converter, \( v_{\text{ab}} \), is also shown. The five levels of this voltage corresponding to \( \{+\frac{1}{3}V_o, +\frac{2}{3}V_o, 0, -\frac{1}{3}V_o, -\frac{2}{3}V_o\} \) are displayed. Also, the positive partial output voltage \( v_o \) regulated on the 800 V is shown.

With the purpose of verifying the voltage self-balancing on the commutation capacitors, in Fig. 12, the voltages across the capacitors, corresponding to phase \( c \), \( v_{C1,A}^c, i \in \{1, 2, 3\} \), are...
shown. It is observed that voltages are well balanced with an average value around 400 V, as expected in the previous analysis. The instantaneous voltages across these capacitors must be very close together, in order to avoid current peak during switched-capacitor stages.

Fig. 13 shows the behavior of the current through the inductor $L_b$, corresponding to phase $a$, and through the capacitor $C_a^3$. Also, the partial output voltages $v_{op}$ and $v_{on}$ are shown. In this figure, it may be observed that both voltages are well balanced and are around 800 V, as expected.

In order to observe the dynamic behavior of the partial output voltage control, a test with voltage-balancing loop was performed. The experimental results can be seen in Fig. 14. Initially, the active control is disabled. As a result, a small difference between the output voltages $v_{op}$ and $v_{on}$ can be seen. At a certain time instant, the voltage-balancing active control is enabled. From that instant, through the control action, the partial output voltage rapidly returns to rated value of 800 V. It can be seen that both input currents $i_{g,k}$, $k \in \{a, b, c\}$, and instantaneous output voltage $v_o$ do not have any alteration with the activation of the voltage-balancing loop.

Fig. 15 depicts the dynamic performance of the proposed feedback control, tested for a resistive load steps from 30% to 100% $P_o$. In this figure, the partial output voltages $v_{op}$, $v_{on}$, the output voltage $v_o$, and input currents $i_{g,k}$, $k \in \{a, b, c\}$, are displayed. It is shown that the output voltages, after disturbance, return to rated value, without affecting the quality of the currents. The input current harmonic analysis for the proposed converter operating at rated power is shown in Fig. 16. The graphic presents the harmonic components in percentage of fundamental component. In this analysis a $\text{THD}_{i} = 4.8\%$ was obtained. Finally, the evaluation performance of the efficiency of the proposed converter was realized. The results may be seen in Fig. 17. The tests were carried out employing the power analyzer Yokogawa WT500, where the load range from 20 to 100 of $\%P_o$ has been measured. An efficiency between 96.6% and 97.78% was reached, which demonstrate the feasibility of this concept technology for high-voltage-gain applications.

VI. CONCLUSION

A three-phase hybrid switched-capacitor multilevel PFC PWM rectifier aiming high-voltage-gain applications has been presented in this paper. This topology use, at the same time, the inductive storage and the switched-capacitor concept to achieve fundamental component.
a high voltage conversion and PFC operation, simultaneously. The three-level operation enables the bulk/weight reduction of the magnetic components. The main feature are low number of active switches and the fact of all components are subjected to one-fourth of output voltage, allowing the use of reducedratings power semiconductor devices. A suitable control scheme has been presented, where it can be seen that synchronous reference frame strategy, used in conventional three-level converters, can also be employed in the proposed converter. Transfer functions for the design of the current regulators and voltage regulators were presented. A 7.5-kW/220-Vto 1600-V/80-kHz laboratory prototype has been built and tested, where the efficiency of 97.78% reached demonstrate the feasibility of this concept technology.

In summary, the current topologies, presented in the introduction, have interesting features for high-voltage-gain applications, but do not have at same time high voltage gain, robustness, low number of active switches and sinusoidal-shape currents. Because of this, the proposed concept presented may be an attractive alternative to high voltage gain in three-phase rectification, with low impact to the grid.

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REFERENCES


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