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Design Oriented Analysis of the RCD Voltage Clamp Circuit for the Forward Converter

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ABSTRACT This paper presents a detailed theoretical design oriented analysis of the RCD-type voltage clamp circuit, used to protect the active power semiconductor of the forward converter with demagnetizing winding. The operation of the circuit is described and analysis aimed at the dimensioning of the parameters is presented. The results are validated with the use of numerical examples and computer simulation, and are appropriate for the dimensioning and optimization of the circuit parameters.

INDEX TERMS DC-DC converter, forward converter, RCD voltage clamp circuit.

I. INTRODUCTION
In isolated DC-DC converters, such as flyback and forward ones, the leakage inductance stores energy which causes ringing and overvoltage across the power semiconductors, at the moment they are turned off. This overvoltage is potentially destructive to power semiconductors, if not limited in any way to appropriate values [1], [2].

To limit the maximum instantaneous voltage across the switches, voltage clamp circuits, which play an essential role in power electronics, are employed. These circuits can be passive or active, dissipative or non-dissipative. The conventional RCD clamp circuit, with a resistor, a capacitor and a diode, despite being dissipative, is simple, robust and inexpensive. In the case of the optimized isolation transformer design, with low leakage inductance, the adverse impact on the efficiency of the converter can be small [3].

A review of the technical literature published in recent decades reveals a large number of publications dealing with analysis of the RCD voltage clamp circuit for the flyback converter [4]-[10] or providing transformer demagnetization of the forward converter when the power semiconductor is switched off by returning the transformer magnetic energy into the input dc bus.

In this paper, the conventional passive and dissipative RCD voltage clamp circuit for the forward converter with demagnetizing winding and a diode to provide magnetizing inductance demagnetization is analyzed. The role of this voltage clamp circuit is to absorb only the energy stored in the leakage inductances. Based on a literature search, exact analysis of the RCD voltage clamp circuit for the forward converter with demagnetizing winding does not appear to have been previously reported, even for ideal components of the circuit.

II. ANALYSIS OF THE RCD VOLTAGE CLAMP CIRCUIT
A power stage diagram of the conventional forward converter with demagnetizing winding \( N_i \) is shown in Figure 1.

![Figure 1. Conventional forward converter with demagnetizing winding \( N_i \).](image)

The same converter, with the RCD clamp circuit included, is shown in Figure 2(a), while the corresponding equivalent circuit with all parameters referred to the primary side of the transformer is shown in Figure 2(b). In Figure 3 the same equivalent circuit is shown, in which the magnetizing inductance is replaced by the current source \( I_{m} \), which is assumed constant during the short period of time in which the demagnetization of the leakage inductance occurs. The leakage inductances of the transformer are defined as follows:

- \( l_i \): leakage inductance of the primary winding;
- \( l_2 \): leakage inductance of the secondary winding, referred to the transformer primary side;
- \( l_3 \): leakage inductance of the tertiary or demagnetization winding referred to transformer primary side.

In order to enable the mathematical description of the operation of the clamp circuit associated with the converter, it will be assumed that: (a) all semiconductors are considered ideal, (b)
during the switching time interval the output stage can be reflected to the transformer primary side and replaced by an ideal and constant current source \( I_o \), (c) during the switching time interval the magnetizing current can be replaced by an ideal and constant current source \( I_m \), (d) all resistances of the power stage components are neglected, (e) the primary and the demagnetizing windings have the same number of turns, and (f) the RC pair of the voltage clamp circuit is replaced by the voltage source \( V_g \).

The different topological states are shown in Figure 4. Prior to the start of the commutation, switch \( S \) conducts the currents \( I_m \) and \( I_o \). As shown in Figure 4(a), the diodes \( D_2 \), \( D_3 \) and \( D_g \) are blocked.

At the instant the switch \( S \) is turned off, current \( I_o \) starts to be transferred from \( D_g \) to \( D_1 \). The corresponding topological state is shown in Figure 4(c). During this time interval, the transfer of energy to the clamp circuit continues.

From the moment diode \( D_1 \) conducts all current \( I_m \), the diode \( D_g \) is blocked and the commutation is completed. The corresponding topological state is shown in Figure 4(d). The corresponding relevant waveforms are shown in Figure 5.

A. Determination of the Time Interval \( \Delta t_1 \)

As follows from the waveforms shown in Figure 5, the behavior of the circuit for the time interval \( \Delta t_1 \) is described by

\[
V_i + V_{g} = \left( l_1 + l_2 \right) \cdot \frac{I_o}{\Delta t_1}
\]

where \( I_o \) is load current referred to the transformer primary side.

Hence,

\[
\Delta t_1 = \frac{\left( l_1 + l_2 \right) \cdot I_o}{V_i + V_{g}}
\]

The sum of voltages \( V_i \) and \( V_{g} \) is given by

\[
V_i + V_{g} = V_{g} - V_i
\]

Substitution of (3) in (2) yields

\[
\Delta t_1 = \frac{\left( l_1 + l_2 \right) \cdot I_o}{V_{g} - V_i}
\]
B. Determination of the Time Interval $\Delta t_2$

As follows from Figure 5, the behavior of the circuit during the time interval $\Delta t_2$ is described by

$$V_i + V_o = (I_i + I_o) \Delta t_2$$

(5)

where $I_m$ is the magnetizing current at the instant of the commutation.

Thus,

$$\Delta t_2 = \frac{(I_i + I_o) \cdot I_m}{V_i + V_o}$$

(6)

The sum of voltages $V_i$ and $V_o$ is given by

$$V_i + V_o = V_g - 2V_i$$

(7)
Substituting (7) in (6) we find

\[
\Delta z = \frac{(l_i + l_z) \cdot I_m}{V_g - 2V_i} \tag{8}
\]

C. Determination of the Average Current in the Diode \(D_g\)

The values of the average currents through \(D_g\) during the time intervals \(\Delta t\) and \(\Delta t_2\) are defined by (9) and (10), respectively.

\[
I_{D_0} = \frac{I_m \cdot \Delta t_1}{T} + \frac{I_m \cdot \Delta t_1}{2 \cdot T} \tag{9}
\]

\[
I_{D_2} = \frac{I_m \cdot \Delta t_2}{2 \cdot T} \tag{10}
\]

The total average current through the diode \(D_g\) is then determined by

\[
I_{D_g} = I_{D_0} + I_{D_2} \tag{11}
\]

Substitution of (9) and (10) in (11) gives

\[
I_{D_g} = \left( I_m \cdot \frac{\Delta t_1}{T} + \frac{I_m \cdot \Delta t_1}{2 \cdot T} + \frac{I_m \cdot \Delta t_1}{2 \cdot T} \right) \cdot f_s \tag{12}
\]

Substituting (4) and (8) in (12), we obtain

\[
I_{D_g} = \frac{I_m \cdot (l_i + l_z) \cdot I_m \cdot f_s}{V_g - V_i} + \frac{I_m \cdot (l_i + l_z) \cdot I_m \cdot f_s}{2 \cdot (V_g - 2V_i)} + \frac{I_m \cdot (l_i + l_z) \cdot I_m \cdot f_s}{2 \cdot (V_g - V_i)} \tag{13}
\]

D. Determination of the Power Dissipated in the Resistor \(R_g\)

The power dissipated in the resistor \(R_g\) is defined by

\[
P_g = V_g \cdot I_{D_g} \tag{14}
\]

Substituting (13) in (14) and arranging the terms, we obtain the dissipated average power in the resistor \(R_g\), given by

\[
P_g = \frac{1}{2} \cdot \left( l_i + l_z \right) \cdot I_m \cdot f_s \cdot \left( \frac{1}{1 - \frac{V_i}{V_g}} \right)
\]

\[
+ \frac{1}{2} \cdot \left( l_i + l_z \right) \cdot I_m \cdot f_s \cdot \left( \frac{1}{1 - \frac{V_i}{V_g}} \right)
\]

\[
+ \left( l_i + l_z \right) \cdot I_m \cdot f_s \cdot \left( \frac{1}{1 - \frac{V_i}{V_g}} \right) \tag{15}
\]

E. Determination of the Resistance \(R_g\) and the Capacitance \(C_g\)

The value of the resistance \(R_g\) is given by

\[
R_g = \frac{V_g^2}{P_g} \tag{16}
\]

To determine the capacitance value of the capacitor \(C_g\), we will analyze the equivalent circuit shown in Figure 6, where \(i_{D_g}\) is the instantaneous current through diode \(D_g\).

\[
\text{Figure 6. Equivalent circuit used to determine the capacitance of } C_g. \]

The waveform of the current \(i_{D_g}\) is shown in Figure 7. Its alternating component circulates through the capacitor \(C_g\) while its continuous component circulates through the resistor \(R_g\). To simplify the analysis and because the continuous component of the current is much smaller than its peak value, we assume that all of the energy is absorbed by the capacitor.
The electrical charge transferred to the capacitor during the time intervals $\Delta t_1$ and $\Delta t_2$ is given by

$$\Delta Q = I_m \cdot \Delta t_1 + \frac{I_m \cdot \Delta t_1}{2} + \frac{I_m \cdot \Delta t_2}{2}$$

(17)

The peak-to-peak value of the alternating component of the voltage across the clamping capacitor $C_g$ is defined by

$$\Delta V = \frac{\Delta Q}{C_g}$$

(18)

Thus,

$$C_g = \frac{\Delta Q}{\Delta V}$$

(19)

The electrical charge can also be given by

$$\Delta Q = I_{DG} \cdot T_s = \frac{I_{DG}}{f_s}$$

(20)

Substitution of (20) in (19) yields

$$C_g = \frac{I_{DG}}{f_s \cdot \Delta V}$$

(21)

Substituting (13) and (15) in (21) and rearranging the terms, we find

$$C_g = \frac{P_g}{f_s \cdot V_g \cdot \Delta V}$$

(22)

The power dissipated in the resistor $R_g$ is calculated using (15). In order to simplify the calculations, let us define and calculate the values of $\alpha_1$ and $\alpha_2$ as follows.

$$\alpha_1 = \frac{1}{2} \left( \frac{V_g}{V_i} \right) = 0.2$$

and

$$\alpha_2 = \frac{1}{1 - \frac{V_g}{V_i}} = 1.67.$$  

The remaining terms of (15) are obtained numerically as follows.

$$\alpha_3 = \frac{1}{2} \left( l_1 + l_2 \right) \cdot I_m \cdot f_s = \frac{1}{2} \times 8 \times 10^{-6} \times 16 \times 10^3 = 2.56 W$$

$$\alpha_4 = \left( l_1 + l_2 \right) \cdot I_m \cdot f_s = 8 \times 10^{-6} \times 1 \times 4 \times 10^3 = 1.280 W$$

Substituting the values of $\alpha_1$, $\alpha_2$, $\alpha_3$, $\alpha_4$ and $\alpha_5$ in (15) we find

$$P_g = 0.2 \times 5 + 2.57 \times 1.67 + 1.28 \times 1.67 = 7.415 W$$

Hence, the value of the resistor $R_g$ is

$$R_g = \frac{V_g^2}{P_g} = \frac{1000^2}{7.415} = 135 k\Omega$$

The minimum capacitance of capacitor $C_g$ is

$$C_g = \frac{P_g}{f_s \cdot V_g \cdot \Delta V} = \frac{7.415}{40 \times 10^{3} \times 10} = 18.5 nF$$

The time intervals $\Delta t_1$ and $\Delta t_2$ are

$$\Delta t_1 = \frac{(l_1 + l_2) \cdot I_m \cdot V_g + V_i}{V_g + V_i} \times \frac{5 \times 10^{-6} + 2 \times 10^{-6}}{1000 - 100} = 5.33 \times 10^{-8} s$$

and

$$\Delta t_2 = \frac{(l_1 + l_2) \cdot I_m \cdot V_g + V_i}{V_g + V_i} \times \frac{5 \times 10^{-6} + 5 \times 10^{-6}}{1000 - 2 \times 400} = 5 \times 10^{-8} s$$

The total time duration of the energy transfer from the leakage inductances to the capacitor $C_g$ is

$$\Delta t = \Delta t_1 + \Delta t_2 = 10.33 \times 10^{-8} s.$$
The simulation and calculation results are shown in Table I while the waveforms obtained by computer simulation are shown in Figure 8.

### Table I
Simulation and Calculation Results for the Numerical Example

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Calculation Results</th>
<th>Simulation Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time interval (Δt₁)</td>
<td>5.33 x10⁻⁸ s</td>
<td>5.37 x10⁻⁸ s</td>
</tr>
<tr>
<td>Time interval (Δt₂)</td>
<td>5.0 x10⁻⁸ s</td>
<td>4.9 x10⁻⁸ s</td>
</tr>
<tr>
<td>Power dissipated in the resistor (P_s)</td>
<td>7.415 W</td>
<td>7.42 W</td>
</tr>
<tr>
<td>Capacitor voltage ripple (ΔV)</td>
<td>10 V</td>
<td>12.26 V</td>
</tr>
<tr>
<td>Average clamping voltage (V_g)</td>
<td>1000 V</td>
<td>1000 V</td>
</tr>
</tbody>
</table>

![Waveform plots](image)

**Figure 8.** Waveforms generated by simulation. (a) Current in the leakage inductance of the primary winding of the transformer. (b) Current in the diode D_s. (c) Voltage across the capacitor C_g.

### III. Minimization of the Power Dissipated in the RCD Voltage Clamp Circuit

According to (15), the power dissipated in the voltage clamp circuit decreases when the voltage V_g across the capacitor C_g increases. On the other hand, the power lost in the power semiconductor (assumed to be a MOSFET) due to the discharge of the parasitic capacitor C_on increases with an increase in V_g, according to

\[ P_s = \frac{1}{2} C_{on} f_s V_g^2 \]  

(23)

The decrease in the power dissipated in the clamp circuit and increase in the power loss in the MOSFET due to the discharge of the parasitic capacitor C_on with increasing voltage V_g suggests that there may be an optimum value for V_g that minimizes the sum of the two power losses, thus improving the efficiency of the converter.

Adding (15) and (23) we obtain the total power loss as a function of V_g, given by

\[ P = \frac{1}{2} (l_1 + l_s) \cdot I_m^2 \cdot f_s \left( \frac{1}{1 - \frac{V_g}{V_i}} \right) \]

\[ + \frac{1}{2} (l_1 + l_s) \cdot I_m^2 \cdot f_s \left( \frac{1}{1 - \frac{V_g}{V_i}} \right) \]

\[ + (l_1 + l_2) \cdot I_o \cdot f_s \left( \frac{1}{1 - \frac{V_g}{V_i}} \right) \]

\[ + \frac{1}{2} C_{on} f_s V_g^2 \]  

(24)

**Figure 9.** Losses as a function of voltage V_g.

It is not possible to obtain an explicit expression for the value of V_g that minimizes the value of \( P = P_s + P_c \). Therefore, for each particular case the curve of \( P \) as a function of V_g needs to be plotted in order to determine the optimal value of the clamp capacitor voltage V_g.

**Figure 9** shows the plots of P_g, P, and P as a function of V_g for a forward converter with the parameters \( V_i = 400 V \).
\[ f_c = 40 \text{kHz} , \quad I_1 = I_2 = 3 \mu \text{H} , \quad I_3 = 1 \mu \text{H} , \quad I_w = 1 \text{A} , \quad I_o = 4 \text{A} , \]
and \[ C_{oss} = 200 \mu \text{F} . \]
The curves show that the dissipated power is minimized when \( V_g \approx 950V \). The values of \( I_w \) and \( I_o \) are determined for the converter operating at rated power.

IV. TOPOLOGICAL VARIATION OF THE RCD VOLTAGE CLAMP CIRCUIT

Figure 10 shows a topological variation of the forward converter, in which the resistor \( R_g \) is connected across the positive terminal of the capacitor \( C_g \) and the positive terminal of the power supply \( V_i \). The advantage of this configuration, in relation to that shown in Figure 2(a), is the reduction of the power dissipated in the resistor \( R_g \) and the consequent improvement of the converter efficiency.

![Figure 10](image)

**Figure 10.** Forward converter with a topological variation of the RCD voltage clamp circuit.

In this case, the resistance of the resistor \( R_g \) is determined by

\[ R_g = \frac{V_g - V_i}{I_{De}} \]  

while the determination of the other parameters is made using the previously obtained equations, which are still valid.

The relation between the dissipated power \( P_{g1} \) in the resistor \( R_g \) connected to the source \( V_i \) and the dissipated power \( P_g \) with the resistor \( R_g \) connected in parallel with the capacitor \( C_g \) is given by

\[ \frac{P_{g1}}{P_g} = \frac{V_g - V_i}{V_g} \]  

Thus, \( P_{g1} \leq P_g \) as expected.

V. CONCLUSION

A theoretical design oriented analysis of the RCD voltage clamp circuit employed to limit the instantaneous peak voltage across the active power semiconductor of the forward converter with demagnetizing winding, caused by the energy stored in the leakage inductances of the isolation transformer, is detailed in this paper.

The results obtained, which were validated by computer simulation, can be used to optimize the parameters of the conventional RCD voltage clamp circuit. The conduction and remainder commutation losses are independent of the previously described losses.

REFERENCES


IVO BARBI (Life Fellow, IEEE) was born in Gaspar, Santa Catarina, Brazil. He received the B.S. and M.Sc. degrees in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianopolis, Brazil, in 1973 and 1976, respectively, and the Dr. Ing. degree in electrical engineering from the Institut National Polytechnique de Toulouse, Toulouse, France, in 1979. He founded the Brazilian Power Electronics Society in 1990, the Brazilian Power Electronics Conference in 1991, and the Brazilian Institute of Power Electronics and Renewable Energy, in 2016. He is currently a Researcher with the Solar Energy Research Center, Florianopolis, SC, Brazil, and a Professor Emeritus of electrical engineering with UFSC. Dr. Barbi was a recipient of the 2020 IEEE William E. Newell Power Electronics Award. He was an Associate Editor for the IEEE Transactions on Industrial Electronics and the IEEE Transactions on Power Electronics for several years.