Acknowledgments

We would like to thank Professor Ivo Barbi for his help and his availability during the entire project. We also want to thank all the technicians who helped us, especially Mr. Pacheco who built with much precision our full circuit. We are also very grateful to Doctorand Eloi Agostini Jr for his presence and help during all the design and the test phase of our converter. We also want to address a special thank to Ayres Ulysséa for his help and advises in making all the connections. Finally we thank Professor Marion for his patience and availability in correcting our final report.

Analysis and design of a bidirectional DC-DC converter

Students : EV2 E. Bigot et F. Le Toullec, EN2007

Type of report : Rapport de Projet de Fin d'Etude (PFE)

University : Federal University of Santa Catarina (U.F.S.C)
Power Electronic Engineering Department (I.N.E.P)

Project Chief : Ivo Barbi, Professor in Power Electronic Engineering at the UFSC

ABSTRACT

This project consists in the analysis and the design of a bidirectional DC/DC converter with given specifications. Since the power was quite high it was necessary to be very precise when calculating all the parameters of the converter.

That is why our first step was to study basic converters such as buck converter in order to better understand more complex ones such as our bidirectional converter, especially concerning switches states. Then, once the parameters needed were known, it was possible to use mathematic equations to choose the right components for the converter.

Since the converter has to be very stable, especially the voltage in the first bus, the following step was the design of a control chain which could ensure the good operating of the system.

Computer software such as PSIM or Math CAD, allowed us to obtain waveforms and numerical values which characterize the operating of the converter.

Finally, the converter was built and tested in order to validate and improve our previous theoretical study and simulation results.

RESUME

Ce projet a pour but l'étude et la réalisation d'un convertisseur bidirectionnel à courant continu régi par un cahier des charges fixant les paramètres électriques souhaités.

Une étude qualitative a permis de comprendre le comportement d'un tel convertisseur, notamment au niveau des interrupteurs. Il a ainsi été possible par la suite d'utiliser les équations mathématiques adéquates afin de dimensionner les paramètres électriques et thermiques nécessaires dans le choix des composants du convertisseur.

L'étape suivante a été l'insertion dans une boucle de contrôle dans le but de réguler les paramètres les plus critiques du convertisseur telle la voltage dans le bus primaire.

Les outils informatiques de calcul (Math CAD) et de simulation (PSIM) ont complété l'étude théorique et permis d'obtenir des valeurs numériques caractérisant le comportement statique et dynamique du convertisseur.

Enfin, le convertisseur ainsi dimensionné a été construit puis testé afin de valider et éventuellement améliorer l'étude théorique et les simulations effectuées.

Key words: Bidirectional DC/DC Converter, Inductor

Summary

Symbols Table

t	Time	s
f	Frequency	Hz
T	Period	s
V_{out}	Output voltage	V
V_i	Voltage across component i	V
I_i	Current through component i	A
I_{iAVG}	Average current through component i	A
I_{iRMS}	Efficient current through component i	A
ΔI_i	Peak to peak value of the current through component i	A
ΔV_i	Peak to peak value of the voltage across component i	V
t_c	Transistor conduction time	s
α	Duty cycle	No dimension
R_i	Resistor i	Ω
L	Inductance	H
C_i	Capacity i	F
P	Power of the system	W
A_e	Central area over the core	cm²
A_w	Window area over the core	cm²
k_w	Factor in core due to air gaps between different wires	No dimension
μ_0	Vacuum permeability	SI
B_{max}	Maximum value of the magnetic field	T
J_{RMS}	Efficient value of the current density	A/cm²
I_{peak}	Peak current through the inductor	A
A_{wire}	Area occupied by one wire	cm²
Φ	Magnetic flux	T/cm²
N	Number of turns of wire	No dimension
l_{wire}	Length of a wire	m
l_g	Gap length	mm
δ	Skin thickness	m
D_{wire} $D_{wire\ iso}$	Diameter of a wire without and with isolation	cm
n_{cond}	Number of wires in parallel	No dimension
P_{copper}	Copper losses	W
P_{mag}	Magnetic losses	W
V_{core}	Volume of the core	cm^3
B_{ac}	Half of the amplitude of magnetic field	T
ΔT	Amplitude of the temperature	K
R_{th}	Thermo resistance	°C/W
V_f	Saturation voltage of the diode	V
P_{condi}	Conduction losses	W
P_{comi}	Commutation losses	W
E_{on} E_{off}	Energy dissipated during commutation	J
T_i	Temperature in point i	K
$\widehat{\imath_L}$	Disturbance of the average inductor current over a period	A
$\widehat{v1}$	Disturbance of the average voltage in the first bus over a period	V
$\hat{\alpha}$	Disturbance of the duty cycle	No dimension
p	Laplace parameter	No dimension

f_c	Cut frequency	Hz
K	Proportional gain	No dimension
τ	Time constant	s
ω	Pulsation	rad/s
Z	Impedance	No dimension
G	Static gain	No dimension
FTOL(f)	Transfer function in open loop	No dimension
$Gain_x(f)$	Gain of the transfer function in open loop	dB

Introduction

Power electronics engineering has increased a lot over the last decades especially because it has lots of applications in everyday life objects, but also thanks to the improvement of useful components such as switches. Indeed, these components are essential to the design of DC/DC converters which are one of the major applications of power electronics.

Moreover, the increasing interest in renewable energies such as hydroelectricity and the worldwide concern about reducing the carbonic gas emission contribute to the development of more powerful and efficient systems that include DC/DC converters, especially the reversible kind.

In the case of a car powered with electricity, the batteries provide the energy necessary to make the vehicle move. Then the aim of using reversible DC/DC converters is to be able to recharge these batteries through the same circuit thanks to the energy provided by a breaking period.

Nevertheless, it is very difficult to obtain a perfect DC component in the output of such converters. That is why their design needs to be very precise.

Our project proposes to fully design a reversible DC/DC converter which has a power of 2kW and operates with two different sources of 200V on one side and 300V on the other side.

To conduct this study, a qualitative analysis will be made first in order to understand the operating of such converters. Then, a theoretical part will explain the design of the main components such as input and output loads, inductor and switches. Finally, the converter will be inserted in a control loop, built and tested to check if the operating is suitable.

I Generalities about DC/DC converters

DC/DC converters are power electronic systems used to transfer electric energy from one continuous source to one another. We can find many different sorts of converters. For example, the most common are buck or boost converters. In this part, we will study these converters which are needed in the design of a more complex reversible converter. All the main waveforms and equations are extracted from the book *Conversores CC-CC básicos não isolados* by Professor Ivo Barbi [1]

I.1. Buck converters

Before studying bidirectional converters, it is necessary to understand how the unidirectional converters work.
The aim of this kind of converter is to allow the energy transfer from a voltage source to a current source. The condition to be respected is that: $0 \leq \overline{V_{out}} \leq V1$ with $\overline{V_{out}}$ the average value of the voltage at the input of the current source.
Here, the current source is represented by a capacitor and a resistor in parallel both plugged to an inductor.

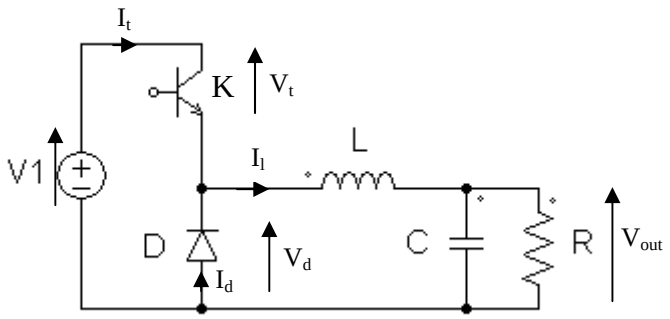


Figure 1: Structure of a buck converter

I.1.a. Commutation cells

The commutation cells are identified as a switch (K) and a diode (D). To realize the mechanism of commutation, it is necessary to command the switch. To build this command, a continuous signal is used and compared to a triangular wave signal. To control the time of conducting and the time of blocking of the switch we just have to change the duty cycle α of the square wave signal. And thanks to this control, it is possible to influence the value of $\overline{V_{out}}$.

Regarding the mechanism of control, two states of commutation can be isolated.
If K is conducting and D is blocking: $V_d = V1$

$$I_l = I_k$$

If K is blocking and D is conducting: $V_d = 0$

$$I_l = I_d$$

Finally, the operating of the buck converter can be summed up by the following curves:

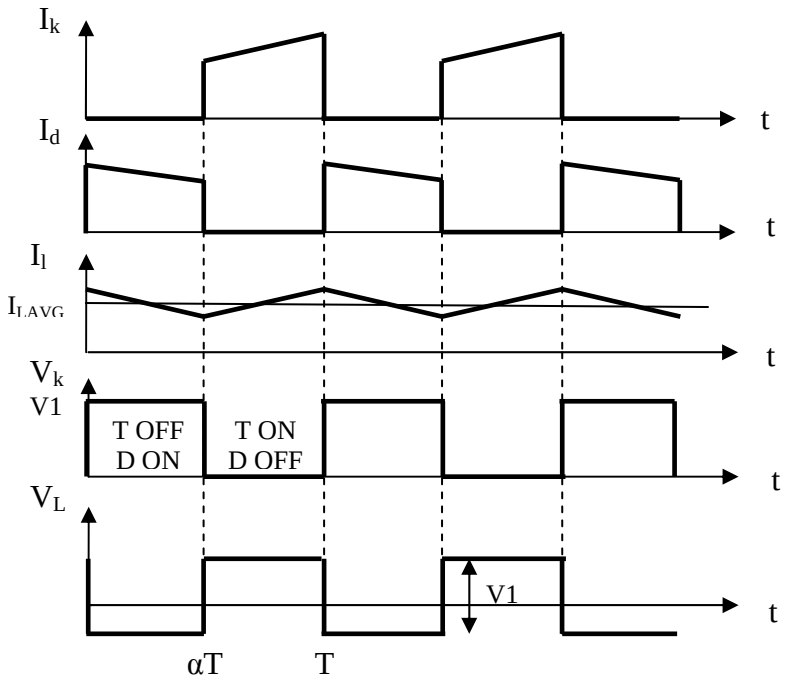


Figure 2: Waveforms of a buck converter

I.1.b. Fundamental relations

According to the states of the switches, output voltage (V_{out}) can have the same value as input voltage (V1) or can reach zero. The problem is that the output voltage has to be a direct one. The solution is given by the output load. Indeed, resistor and capacitor create a low-pass filter. If the cut frequency of this filter is lower than the commutation frequency, then we can take the average value for the output voltage.
Finally, a relation links average output voltage, duty cycle and input voltage:

$$\overline{V_{out}} = \frac{1}{T}\int_0^T V_{out}(t)dt = \frac{1}{T}\int_0^{\alpha T} V1\ dt = \frac{1}{T}(\alpha T * V1 - 0 * V1)$$

$$\text{Thus } \overline{V_{out}} = \alpha * V1 \quad (1)$$

α is the duty cycle. It is defined by the ratio between the time of conduction of the switch (t_c) over the commutation period (T)

$$\alpha = \frac{t_c}{T}\ with\ 0 \leq \alpha \leq 1$$

Therefore, action on conduction time allows us to control the value of direct output voltage, and equation (1) illustrates the fact that the output voltage is effectively lowered.

I.2. Boost converters

The operating of a boost converter is almost similar to that of a buck converter. Now the aim is just to increase the input voltage. In order to do this, we just have to reorganize the commutation cells as is shown in figure 3:

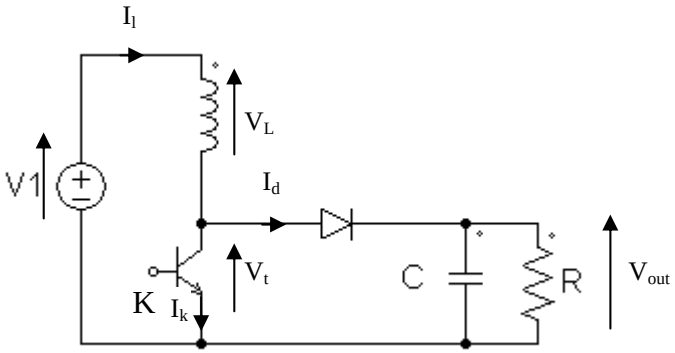


Figure 3: Structure of a boost converter

I.2.a. Commutation cells

The commutation cell is still a switch (K) and a diode (D). The mechanism of control used is the same as in part I.1.a. In this case, there are also two states of switch:
If K is conducting and D is blocking: $V_L = V1$

$$I_l = I_k$$

If D is conducting and K is blocking: $V_L = V1 - V_{out}$

$$I_l = I_d$$

Thus, we obtain the waveforms of figure 4:

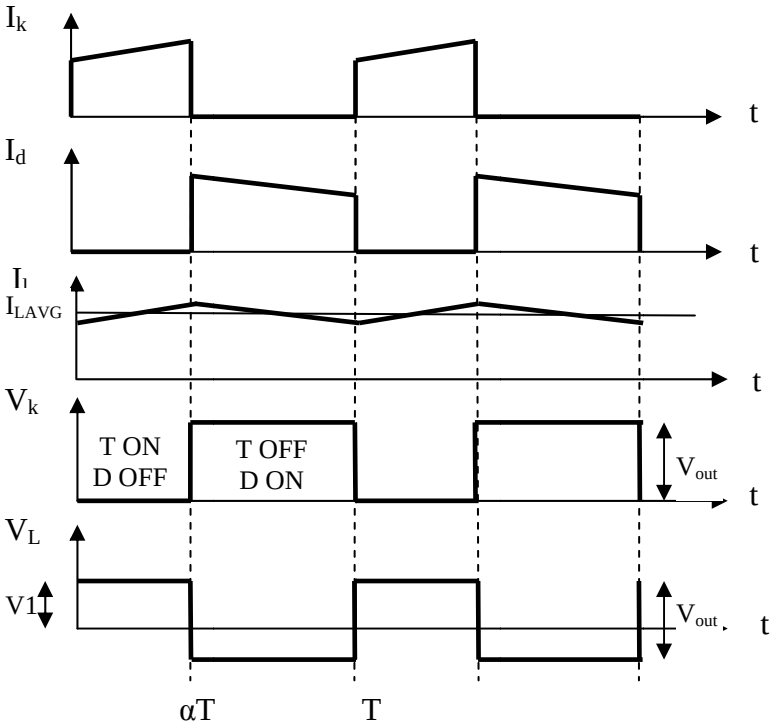


Figure 4: Waveforms of a boost converter

I.2.b. Fundamental relations

The output voltage still has to be a direct one. So, the average voltage value of this converter must be studied.
The average voltage in the inductor can be expressed with the next relation:

$$\overline{V_l} = \frac{1}{T}\int_0^T V_l(t)dt = \frac{1}{T}\left(\int_0^{\alpha T} V1dt + \int_{\alpha T}^{T}(V1 - V_{out})dt\right) = \alpha * V1 + (1-\alpha)(V1 - V_{out}) \quad (2)$$

Now, when the converter operates in steady state, the average value of the inductor must be equal to zero.
Thus (2) is equivalent to: $0 = V1 - (1-\alpha) * V_{out}$

$$\text{Finally: } V_{out} = \frac{1}{1-\alpha} * V1 \quad (3)$$

As $0 \leq \alpha < 1$, equation (3) illustrates the fact that the output voltage is increased as a function of the input voltage.

I.3. Reversible converters

A reversible converter can be modeled in lots of different ways. For our study, the association of a buck and a boost converter has been chosen.
Thanks to this structure, the transfer of power will be done in both ways. Figure 5 illustrates the structure of the converter. On the left part, the buck converter is recognizable, the only difference with the "classic" representation of part I.1. is that the diode and the switch have been replaced by two module (IGBT and diode plugged in parallel). On the right part, this is the boost converter where the diode and the switch have also been replaced by the same two module. Also the function of the inductor is to allow the transfer of power from one voltage source to another. Indeed, it is physically impossible to connect directly two sources of the same nature.
During all this part, we will only consider the conversion in the way V1→V2. Moreover, the study is here considering two voltage sources in the input and in the output in order to ease the understanding of the system. Later, to be nearer to reality, these two sources will be replaced by a capacitor and a resistor both associated in parallel.

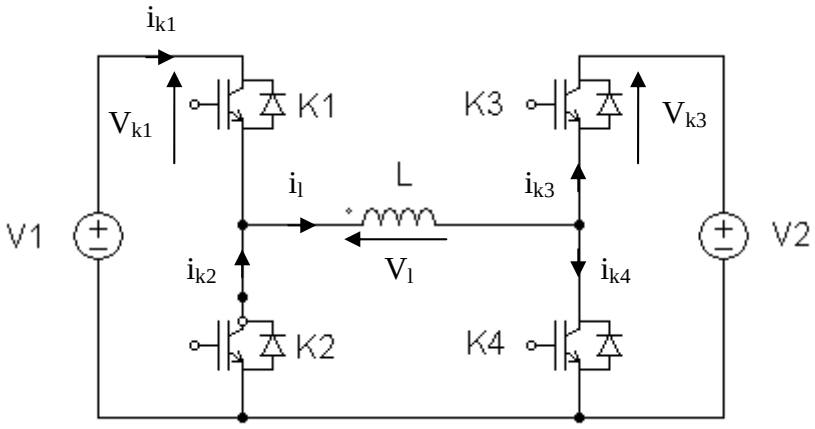


Figure 5 : Structure of a bidirectional DC-DC converter

I.3.a. Commutation cells

Here all the commutation cells are the modules that have been defined. All the commutation will operate two by two. But before trying to identify the waveforms, it is necessary to list all the impossible cases. First, if K1/K2 or K3/K4 are conducting at the same time, it is a case of short-circuit. Then, if K1/K3 or K2/K4 are conducting at the same time, the circuit is of no interest. So there is one case left: K1/K4 or K2/K3 conducting.
If K1/K4 are conducting and K2/K3 are blocking: $V_L = V1$

$$I_L = I_{k1}$$

In this case, the voltage source (V1) imposes the way of the current through the circuit. The current flows through the IGBT and the power flows from V1 to the inductor.

If K2/K3 are conducting and K1/K4 are blocking: $V_L = -V2$

$$I_L = I_{k2}$$

In this second case, it is the inductor which imposes the way of the current through the circuit. The current flows through the diodes of the modules and the power flows from the inductor to V2
The waveforms are now given in figure 6:

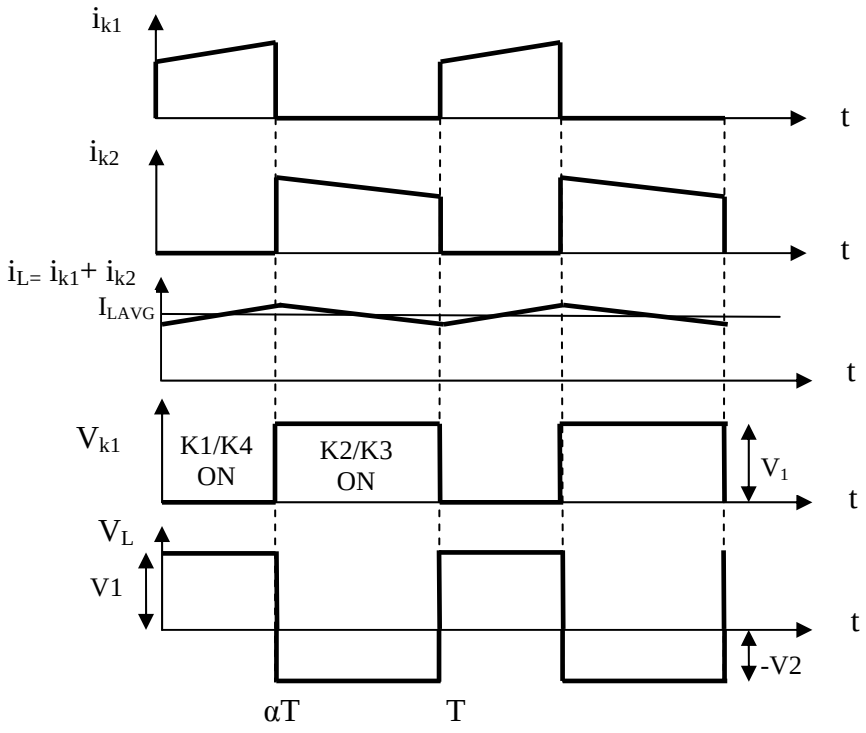


Figure 6: Waveforms of a bidirectional DC-DC Converter

The main observation about these curves is that the output signal is not a perfect equivalent to a DC component. In fact, the inductor provides an oscillating component. That is why in reality V1 and V2 are considered as a capacitor and a resistor in parallel. Indeed the aim of the capacitor is to reduce the oscillating component and provide a DC component to the resistor.
Practice shows that it is impossible to make all the oscillations disappear. Also, we usually prefer to consider an error quoted as ΔV2 and to assimilate the average value of the signal as V2.

I.3.b Fundamental relations

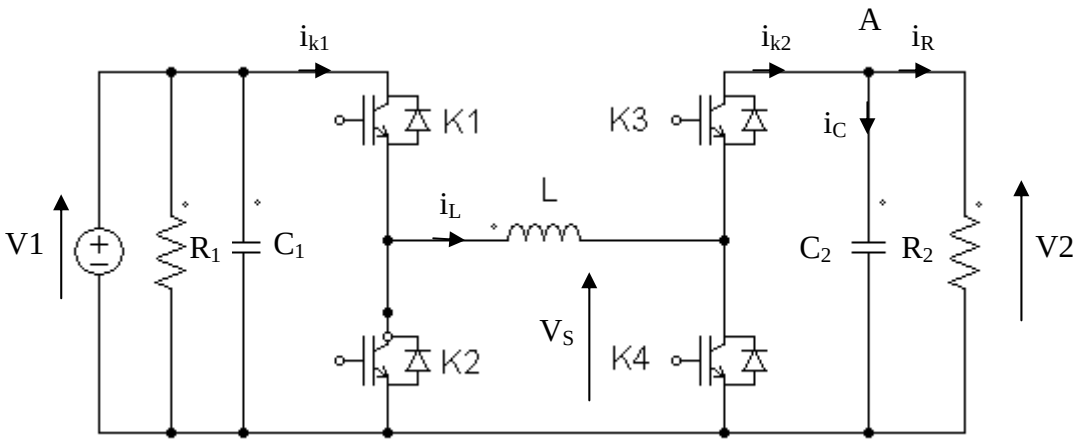


Figure 7:Bidirectional DC/DC converter with real voltage sources

For the quantitative study, it was necessary to consider the converter we had to build. Its' structure is given in figure 7. As explained before, the voltage sources have been modeled by a capacitor and a resistor in parallel.
As a matter of fact, the equations which govern the system must be defined. The first step is to define the duty cycle of the system.

Here, the left part of the converter is still a buck converter. As a consequence, according to equation (1):

$$\frac{V_S}{V1} = \alpha \quad (4)$$

Also, the right part is a boost converter. Now, according to equation (3):

$$\frac{V2}{V_S} = \frac{1}{1-\alpha} \quad (5)$$

By mixing equations (4) and (5), we obtain:

$$G = \frac{V2}{V1} = \frac{\alpha}{1-\alpha} \text{ which leads to } \alpha = \frac{V2}{V1+V2} = 0.6 \quad (6)$$

The next step is to define all the parameters of the inductor. The most important ones are:
L: inductance of the inductor
ΔI_L: peak to peak value of the inductor current
I_{LRMS}: RMS value of the inductor current
I_{LAVG}: average value of the inductor current
V_L: Voltage across the inductor

The voltage across the inductor is defined by the elementary relation:

$$V_L = L * \frac{di_L}{dt} \quad (7)$$

According to the waveforms of figure 6 and for $0 \leq t \leq \alpha T$ equation (7) gives:

$$V_L = L * \frac{\Delta I_L}{\alpha T} = V1 \text{ as a consequence } \Delta I_L = \frac{V1 * \alpha}{L * f} \text{ (8) with } f = \frac{1}{T}$$

If we consider I_1 as the average value of the current i_{k1}, the power can be defined as:

$$P = V1 * I_1$$

But according to the waveforms of figure 6, for $0 \leq t \leq \alpha T$ the peak to peak value of i_{k1} is very low, as a consequence, we can consider that $i_{k1} = I_{LAVG}$. Thus:

$$I_1 = \alpha * I_{LAVG}$$

$$\text{Finally } P = V1 * \alpha * I_{LAVG} \text{ and } I_{LAVG} = \frac{P}{V1 * \alpha} \text{ (9)}$$

In order to have the best design of the inductor, it is also necessary to calculate the Root Mean Square (RMS) current through the inductor and as we need to be very accurate, $i_L(t)$ will not be approximated to I_{LAVG}.

$$I_{LRMS} = \sqrt{\frac{1}{T} * \int_0^T (i_L(t))^2 \, dt} = \sqrt{{I_{LAVG}}^2 + {\Delta I_L}^2 \left(\frac{(\alpha + 1)^2}{3} - \frac{\alpha}{4} \right)} \text{ (10)}$$

The last step is to define the parameters of the capacitor. The current through a capacitor is characterized by:

$$i_C = C * \frac{dV2}{dt} \text{ (11)}$$

As is said in part I.3.a. the output voltage has an oscillating component. As a consequence, for $\alpha T \leq t \leq T$, equation (11) is equivalent to:

$$i_C = C_2 * \frac{\Delta V2}{(1 - \alpha)T} \text{ (12) } with\ \Delta V2 = V2_{max} - V2_{min}$$

Then for $\alpha T \leq t \leq T$, if we consider, for the same reason as with i_{k1}, that the value of i_{k2} is approximated to I_{LAVG}, the Kirchhoff law applied on point A gives:

$$i_C = I_{LAVG} - \frac{V2}{R_2} \text{ (13)}$$

Moreover, considering that the power transmitted is kept:

$$P = \frac{V2^2}{R_2} \ thus \ R_2 = \frac{V2^2}{P} \text{ (14)}$$

Finally, associating equations (12), (13) and (14)

$$C_2 = \frac{(1-\alpha) * \left(I_{LAVG} - \frac{P}{V2}\right)}{f * \Delta V2} \quad (15)$$

To complete the design of the capacitor, we also need to calculate the value of the RMS current through it.

$$I_{CRMS} = \sqrt{\frac{1}{T} * \int_0^T (i_c(t))^2 dt} = \sqrt{(1-\alpha) * \left({I_{LAVG}}^2 - 2 * \frac{P * I_{LAVG}}{V2}\right) + \left(\frac{P}{V2}\right)^2} \quad (16)$$

Now that we have all the equations which govern the converter, we can calculate the values of the components of our bidirectional converter. This converter will be designed to work in particular conditions which are summarized in Table 1:

Conditions	D	I_{LAVG}(A)	I_{LRMS}(A)	L(mH)	R_2(Ω)	I_{CRMS}(A)	C_2(µF)
V1=200V V2=300V ΔV2=3V $\Delta I_L=0.2I_{LAVG}$ f=20kHz P=2kW	0.6	16.667	16.694	1.8	45	8.165	66.7

Table 1: Physic parameters of the designed converter

All these values have been tested and confirmed with a simulation software called PSIM. Indeed, the simulation reveals that all the specified parameters as power, average value and error of the output voltage are respected.

II Design and construction of the converter

The converter will be designed to operate in the condition we defined in Table 1. In order to conduct the analytical study we used MathCAD software to get all numerical values about the inductor and the semiconductors. Indeed, we have to choose the components that best fit the parameters we calculated. Moreover, instead of choosing an inductor, this study proposes to build our own inductor. Then , all the main equations used in this design have been checked with the book *Projetos de fontes chaveadas* by Professor Ivo Barbi [2].

II.1. Design of the inductor

First of all, we may define the structure of an inductor. In fact, this is a ferrite core which is surrounded with lots of turns of wires. What we have to do here is to calculate all the necessary parameters in order to choose the right core and wires. Moreover, the current flux through the inductor implies an increase of temperature, and each core is manufactured to operate in a precise window of temperature. That is why we also have to take account of heat transfer in the inductor.
Now, to conduct this study, we need to introduce new values:

A_e : Central area over the core.
A_w : Window area over the core.
k_w : Factor in core due to air gaps between different wires. $k_w = 0.7$
B_{max} : Maximum value of the magnetic field density. $B_{max} = 0.35$ T
J_{rms} : RMS value of the current density. $J_{rms} = 270$ A/cm^2
I_{peak} : Peak value of the current through the inductor. $I_{peak} = I_{Lavg} + \Delta I_L/2$
A_{wire} : Area occupied by one wire. $A_{wire} = I_{rms}/ J_{rms}$

II.1.a. Design of the core

The inductor will be designed for its limit application. As a consequence, it will be designed for the highest value of the current and the highest value of the magnetic field density. Moreover, we already choose a shape for this core which is shown in figure 8.

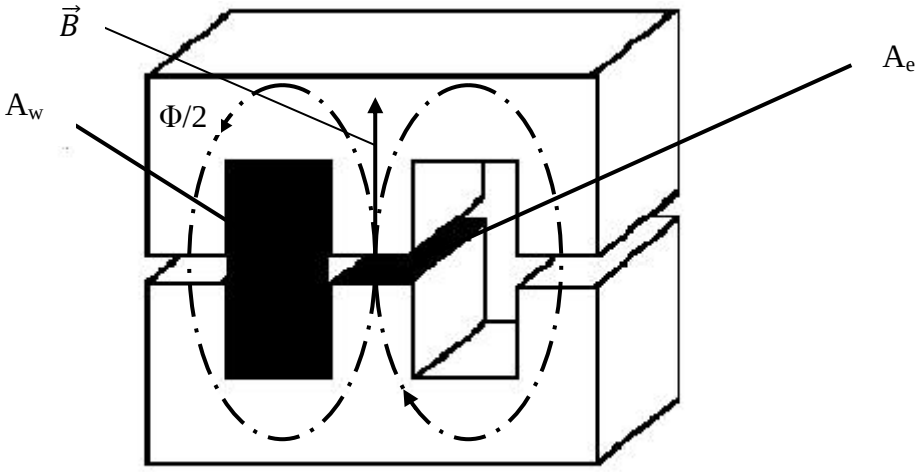


Figure 8: Core geometry of the inductor

First, we made the hypothesis that the magnetic flux is homogenous in the core, it means that the flux is symmetrically distributed.
The magnetic flux is defined by:

$$\Phi = \iint_S \vec{B}.d\vec{S} = B * A_e \ (17) \ with \ S \ the \ section \ parallel \ to \ A_e$$

Besides the flux across an inductor composed of N turns:

$$N * \Phi = L * i_L(t) \leftrightarrow N * B * A_e = L * i_L \ (18)$$

Considering the maximal values:

$$A_e = \frac{L * \mathrm{I_{peak}}}{B_{max} * N} \ (19)$$

Now, the window area which is necessary to be available can be defined as:

$$A_W = \frac{N}{k_w} A_{wire} = \frac{N * I_{rms}}{k_w * J_{rms}} \ (20)$$

Finally, if (19) and (20) are linked we obtain the design ratio which will allow us to choose the right core:

$$A_e A_W = \frac{L * I_{rms} * \mathrm{I_{peak}}}{k_w * J_{rms} * B_{max}} \ (21) \ thus \ A_e A_W = 75.711 \ cm^4$$

We refer the value in the core table. No value corresponds accurately to this one. As a consequence, we need to oversize the core, it means that we need to take a core with a higher value of $A_e A_W$. The advantage is that a bigger core will lower the temperature rise.
We decided to choose a value of A_eA_w equal to 187,3 cm^4 which matches with **NEE-76/50/76** core. This core is made by **Thornton Eletrônica Ltda**. Moreover, the company gives us the characteristics of the core: $A_e = 19.35 \ cm^2$; $A_w = 9.67 cm^2$; $V_{core} = 421.35 cm^3$
But, to simplify the building of the inductor, we decided to roll up the wires around a plastic part that fits into the core, and then to plug the two parts of the core. Consequently, the theoretical value of A_w is lowered to another value with a factor we evaluated to 0.67 .
Thus, $A_w = 9.67 * 0.67 = 6.45 \ cm^2$

II.1.b. Number of turns and gap length

Once the core is chosen, it is necessary to determine the number of turns around the central part of the core, and the distance we have to put between the two parts of the core in order to get the value of inductance we calculated in part I.3.b.
According to equation (19):

$$N = \frac{L * \mathrm{I_{peak}}}{B_{max} * A_e} = 48.73$$

As it is impossible to make 48.73 turns, we decided to increase this value to the next integer one. Thus, N = 49.
Besides equation (19) shows that N and B_{max} are linked. We need to recalculate B_{max} to verify the consistence of our hypothesis. Now taking N = 49 and using equation (19): B_{max} =0.348 T.
If we calculate the relative error $\varepsilon = \frac{0.35 - 0.348}{0.35} = 0.57\%$
The hypothesis is valid, the number of turns will effectively be N = 49.

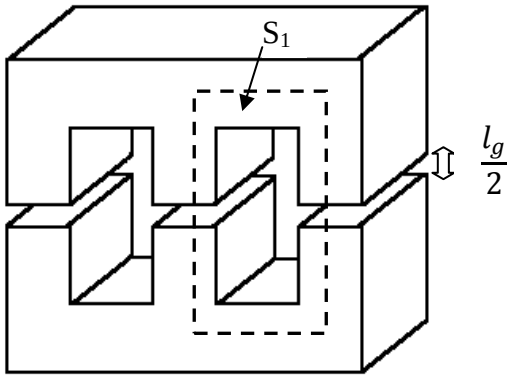


Figure 9: Diagram of the core expressing gap length

Then, we have to evaluate what we call the gap length. This is the distance between the two parts of the core.
The Maxwell-Ampere relation in permanent mode gives:

$$\overrightarrow{rot}(\vec{H}) = \vec{J}$$

By integration on the area S_1 and applying Stokes theorem:

$$\oint_{L(S_1)} \vec{H}.d\vec{l} = \iint_{S_1} \vec{J}.d\vec{S}$$

$$H_{core} * l_{core} + H_{gap} * l_g = N * i_L$$

Moreover, $B_i = \mu_i * H_i$ and $\mu_0 \ll \mu_{core}$ with μ_0 the vacuum permeability and μ_{core} the core permeability (ferrite)
Finally considering that B has almost the same value in the core as in the gap:

$$l_g = \frac{\mu_0 * N * i_L}{B} \quad (22)$$

Otherwise, equation (18) allows us to express the last equation with known variable:

$$l_g = \frac{\mu_0 * N^2 * A_e}{L} \quad thus \; \mathrm{l_g} = 3.24 \text{ mm}$$

II.1.c. Determination of the wires parameters

The study of the wires is an important step in the conception of the inductor. On the one hand, the wires are at the origin of the intern resistance. This resistance will fix the value of the copper losses. On the other hand, the wires have to be designed so that the 49 turns of wires fit into the core.
Moreover, in a conductor, the current circulates in a well defined thickness. This phenomenon is called skin effect and it is linked to the frequency and to the nature of the wires. In our case, an empirical equation has been determined by the manufacturer of the wires: $\delta = 7{,}5/\sqrt{f}$
This value is very important for the design of the wires, it will determine their maximum diameter (D_{wire}).

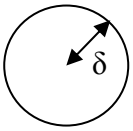


Figure 10: Skin thickness in a conductor

The condition selected:

$$D_{wire} < 2\delta = 0.106\ cm$$

Lots of wires correspond to this condition. However, making availability at the laboratory our first criterion, we selected the American Wire Gauge 24: **AWG24**.
This wire has the following parameters:

$$D_{wire} = 0.051cm \quad D_{wire\_iso} = 0.057cm \quad \rho = 0.001125\,\Omega/cm$$

Nevertheless, it is impossible to get the right inductor with only one wire. As a consequence, we have to put several wires in parallel. But before calculating, we need to introduce new parameters:
A_{wire_tot}: Area necessary to have the right current density in the wires according to the value of I_{rms} $A_{wire\_tot} = I_{rms}/J_{rms} = 0.062\ cm^2$
S_{wire} : Section of one wire. $S_{wire} = \pi {D_{wire}}^2/4 = 2.04 * 10^{-3} cm^2$
n_{cond} : Number of wires in parallel
Finally,

$$n_{cond} = \frac{A_{wire\ tot}}{S_{wire}} = 30.23$$

As there is no way to split one wire, we decided to use the next integer value: $n_{cond} = 31$.
The last parameter is the length of wire (l_{wire}) which will be necessary. The average length of a turn around the central part of the core has been measured as l_{turn} = 25.4 cm.
Consequently: $l_{wire} = N\ l_{turn}$ = 12.44 m

II.1.d. Power losses and heat calculation

There are two kinds of power losses in an inductor: copper and magnetic losses. The copper losses are linked to the value of the internal resistance of the inductor. This resistance comes from the wires that are used. As we have 31 conductors in parallel, the internal resistance is given by the formula:

$$R_{copper} = \frac{\rho * l_{wire}}{n_{cond}} = 45\ m\Omega$$

Then, the power dissipated in a resistance:

$$P_{copper} = R_{copper} * {I_{rms}}^2 = 12.58\,W$$

Regarding the magnetic losses, we used an empirical formula which is generally used by factories for this kind of core:

$$P_{mag} = 1{,}052 * {B_{ac}}^{2{,}44} * f^{1{,}5} * V_{core} \quad (23)$$

The magnetic field density B has the same variation as i_L. The peak to peak value of B is defined thanks to equation (13) as:

$$\Delta B = \frac{L * \Delta I_L}{N * A_e} = 0.064\ T$$

And:

$$B_{ac} = \frac{\Delta B}{2} = 0.032\ T$$

Thus:

$$P_{mag} = 2.75\ W$$

Since we calculated the power losses, we can now evaluate the temperature rise (ΔT). Indeed, the inductor has to work under a well defined temperature to be efficient. If the losses are too important, the temperature will be too high and the component will be damaged. If ΔT is not suitable we will have to restart the designing of the inductor.
The Thermo equation of our system is:

$$\Delta T = R_{th}\left(P_{copper} + P_{mag}\right)\ (24) \text{ with } R_{th} \text{ the thermo resistance}$$

The thermo resistance of the core we used:

$$R_{th} = \frac{23}{(A_e A_w * 10^8)^{0,37}} = 3.86\ °C/W$$

Finally,

$$\Delta T = 59.1\ °C$$

The core is manufactured to work with a temperature lower than 210 °C. If we consider that the ambient temperature is around 25 °C, the operating temperature of our inductor will be 84.1 °C. The thermo conditions are respected.

II.1.e. Possibility of execution

Once the physical parameters are valid, it is necessary to check if the core can be technically realized, it means that we have to check if the wires can fit into the core.
We first define the area occupied by all the turns of wires considering their isolation part:

$$S_{wire\ iso} = \frac{\pi * N * n_{cond} * {D_{wire\ iso}}^2}{4 * k_w} = 5.54\ cm^2$$

Then we define the possibility of execution ratio K_{exec} which is the ratio of $S_{wire\ iso}$ over A_w

$$K_{exec} = \frac{S_{wire\ iso}}{A_w} = \frac{5.54}{6.45} = 0.858$$

This ratio reveals the occupation of the window by all the turns of wires. Thus, 85.8% of the window will be occupied by the wires.
Considering all the parameters of this study, we can say that our inductor is well designed.

II.1.f. Construction and measures

We built our inductor at the laboratory of INEP. To perform this, we first put the 31 wires together. Then, we rolled up the bundle of wires around the plastic part. After that, we plugged the two parts of the core together with the plastic part.
Finally, in order to get the inductance value that we wanted (L=1.8mH), we adjusted the gap length by measuring the inductance with different values of the gap.

The most suitable practical value we obtained is: L=1.83mH and $l_g \approx 2.7$mm

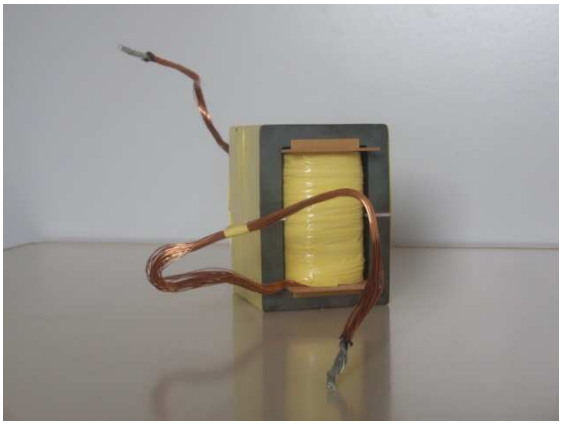


Figure 11: Picture of our inductor

II.2. Design of the power semiconductors

Once the inductor is designed and the parameters of the circuit are fixed, it is necessary to study the power semiconductors. Indeed, these components dissipate some energy which has to be taken into account. In this part, we will not try to choose the semiconductors which correspond the best to our system. In fact, we had to use the components which were available at the laboratory. Thus the IGBT used was **SKM 100GB063D** manufactured by **Semikron Ltda**. Its' maximal condition of operating are U = 600V and I = 100A which are much higher than the values of our system.

II.2.a. Equivalent electric diagram

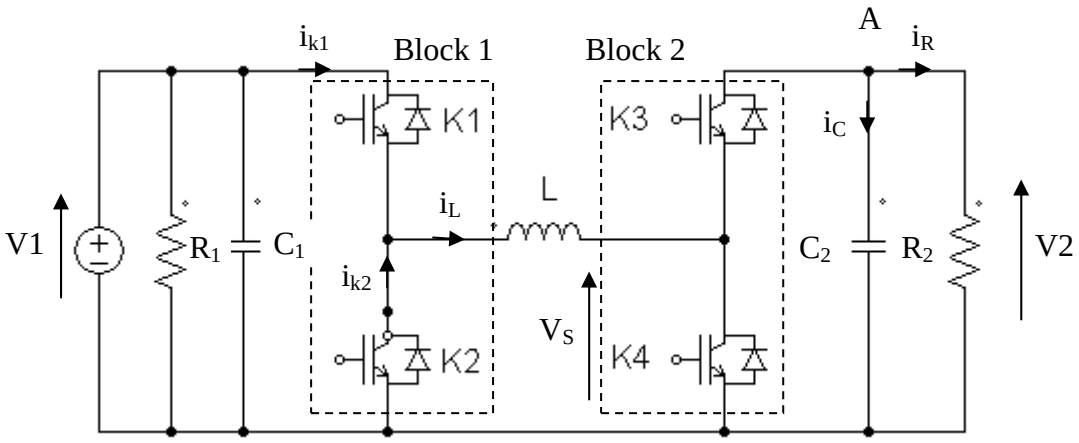


Figure 12 : Identification of the two blocks

We can now consider two blocks in the circuit. The first one composed of K1 and K2, and the second one composed of K3 and K4. Indeed, if we consider that the power flows from V1 to V2 , K1 and K4 are in the same state at the same moment so as K2 and K3. Finally we can say that block 1 and block 2 have the same operating, and we can reduce the study to block 1.

The next step is to identify the electric parameters of the two switches. The most important one is the current.
If we still consider that on a period, $i_L = I_{LAVG}$, then according to figure 6, a calculus of area gives:

$$I_{K1\,AVG} = \alpha I_{LAVG} \; and \; I_{K2\,AVG} = (1-\alpha) I_{LAVG} \quad (25)$$

Moreover:

$$I_{K1\,RMS} = \sqrt{\frac{1}{T}\int_0^T (i_{K1}(t))^2 dt} = \sqrt{\frac{1}{T}\int_0^{\alpha T} {I_{LAVG}}^2 dt}$$

$$I_{K2\,RMS} = \sqrt{\frac{1}{T}\int_0^T (i_{K2}(t))^2 dt} = \sqrt{\frac{1}{T}\int_{\alpha T}^{T} {I_{LAVG}}^2 dt}$$

Thus:

$$I_{K1\,RMS} = I_{LAVG}\sqrt{\alpha} \; and \; I_{K2\,RMS} = I_{LAVG}\sqrt{1-\alpha} \quad (26)$$

Once we know the current through each module, we have to identify which component of the module is conducting. This step has already been done in part I.3.a. We remember that when the power flows from V1 to V2 and K1/K4 are conducting, the current flows through the transistor. In the same case, when K2/K3 are conducting, the current flows through the diode.

Then, it is necessary to determine a model for each component in order to be able to calculate the power losses. In our case we decided to choose the classical representation for each component:

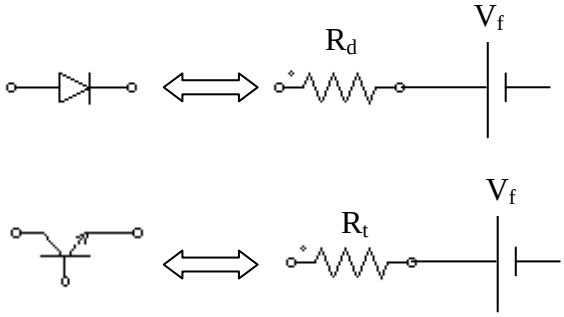


Figure 13 : Equivalent representation of a diode and a transistor

With the parameters extracted from the datasheet of the IGBT and taken for a 125°C temperature:

R_d : Internal resistance of the diode $R_d = 14 * 10^{-3}\Omega$
R_t : Internal resistance of the transistor $R_t = 10 * 10^{-3}\Omega$
V_f : Saturation voltage in the diode and in the transistor $V_f = 1.05V$

II.2.b. Conduction losses

The study of conduction losses is very important because if the switches do not suit the system, the losses could be very high and the converter would have bad efficiency. The losses are the results of the Joule effect.
According to equations (25) and (26) the numeric values of the currents are:

$$I_{K1\,AVG} = 10\,A \;\; ; \;\; I_{K1\,RMS} = 12.91\,A \;\; ; \;\; I_{K2\,AVG} = 6.67\,A \;\; ; \;\; I_{K2\,RMS} = 10.54\,A$$

The conduction losses can be modeled by the formula $P_{cond\,Ki} = P_{R\,Ki} + P_{V\,Ki}$ where P_R and P_V are respectively the losses in the resistor and across the voltage source V_f.
Thus since K1 can be modeled as a transistor and K2 as a diode:

$$P_{cond\,K1} = R_t * {I_{K1\,RMS}}^2 + V_f * I_{K1\,AVG}$$

$$P_{cond\,K2} = R_d * {I_{K2\,RMS}}^2 + V_f * I_{K2\,AVG}$$

Finally, the conduction losses for block 1:

$$P_{cond\,B1} = P_{cond\,K1} + P_{cond\,K2} \;\; thus \;\; P_{cond\,B1} = 20.94\,W$$

And the conduction losses for the whole converter:

$$P_{cond} = 2 * P_{cond\,B1} = 41.88\,W$$

II.2.c. Commutation losses

The conduction losses are not the only power losses of our converter. Indeed, since the IGBT are not perfect conductors, there is a time during which the current and the voltage are both not equal to zero, this is the time of commutation. Thus, there is a loss of energy which needs to be considered.

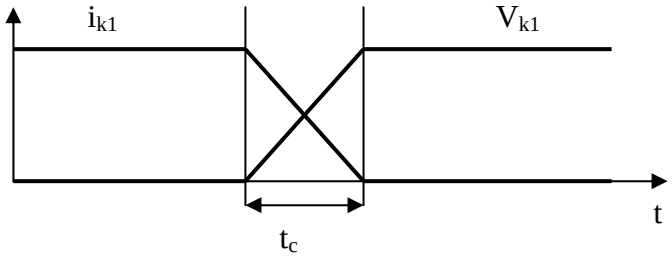


Figure 14 : Illustration of the commutation time

Then, we can distinguish two sorts of commutation losses. The losses when the switch is opening and the losses when the switch is closing, respectively E_{on} and E_{off}. These two energies are proportional to the current through the switch. Since the current is not really continuous in each switch when it is conducting, we decided to consider its highest value I_{peak} = 18,33 A
Moreover, the datasheet of the switch gives us for a current of 100 A and a block of 2 IGBT:

$$E_{on} = 4\,mJ \;\; and \; E_{off} = 3\,mJ$$

Then considering a worse case than our real peak current, we took a current of 20 A and finally we obtain:

$$E_{on} = 0{,}8\ mJ \ \ and\ E_{off} = 0.6\ mJ$$

Thus, since there is one turning on and one turning off in each period, the commutation losses can be modeled by:

$$P_{com\,B1} = f\left(E_{on} + E_{off}\right) = 28\ W$$

Thus, as block 2 has the same behaviour as block 1:

$$P_{com\,B2} = f\left(E_{on} + E_{off}\right) = 28\ W$$

Finally, the whole commutation losses are: $P_{com} = P_{com\,B1} + P_{com\,B2} = 56\ W$

And the overall power losses: $P_{tot} = P_{cond} + P_{com} = 97.88\ W$

II.2.d Heat calculation

Since there are electrical power losses related to the Joule effect in the switches, we must pay attention to the temperature in the system. As each component is manufactured to operate bellow a certain temperature, it is necessary to study the thermo comportment of the switches in order to design a heat sink which will limit the increase in temperature.
To conduct this study, we will consider that junction temperature (T_j) and case temperature (T_c) are respectively the same in each component whichever block is considered. Moreover, as the two blocks are dropped on the heat sink they also have the same temperature (T_{HS}). In order to be able to dissipate the highest quantity of heat, the heat sink will be designed for the highest junction temperature T_j = 125°C.
Also, as the whole system (switches and heat sink) is in a stuffy environment we considered the environment temperature T_{env} = 50°C.
Then, we have to make an equivalent diagram to ease the calculus of R_{HS} (the main parameter in designing the heat sink)

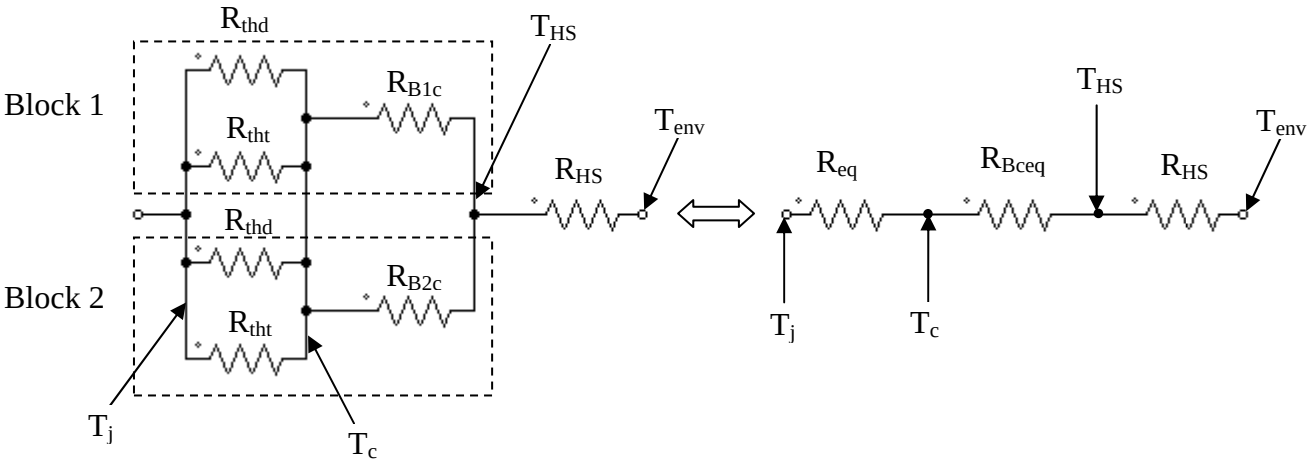


Figure 15: Equivalent thermo diagram

Let us introduce:
R_{thi} : thermo resistance of component i between junction and case.
R_{Bic} : thermo resistance of block i between case and heat sink.
R_{HS} : thermo resistance of the heat sink.

The datasheet given by the manufacturer reveals:

$$R_{thd} = 0.6\,°C/W \;;\; R_{tht} = 0.27\,°C/W \;;\; R_{Bic} = 0.05\,°C/W$$

Then:

$$\frac{1}{R_{eq}} = \frac{2}{R_{thd}} + \frac{2}{R_{tht}} = \frac{2(R_{tht} + R_{thd})}{R_{thd} * R_{tht}} \;\; and \;\; \frac{1}{R_{Bceq}} = \frac{2}{R_{Bic}}$$

Thus:

$$R_{eq} = 0.093\,°C/W \;\; and \;\; R_{Bceq} = 0.025\,°C/W$$

Finally, the thermo application of Ohm law according to figure 15:

$$T_j - T_{env} = \left(R_{HS} + R_{eq} + R_{Bceq}\right) * P_{tot} \quad (27)$$

As a consequence:

$$R_{HS} = \frac{T_j - T_{env}}{P_{tot}} - \left(R_{eq} + R_{Bceq}\right) = 0.648\,°C/W$$

The result of this calculus gives us the ideal thermo resistance of the heat sink. We tried to find in the manufacturer datasheets the heat sink that best corresponds to our system but without success. As a consequence, we had to choose a heat sink with a lower value of thermo resistance. Finally, we chose **HS19334** with a length of 30 centimeters and a thermo resistance R_{HS} = 0.62 °C/W, manufactured by **HS Beneficiamento de Alumínio Ltda.**

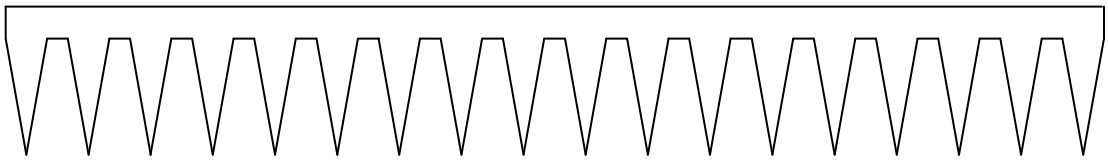


Figure 16: Shape of the heat sink HS19334

III Control of the converter

Once the converter is designed, it is necessary to design the control circuit. This circuit is the one which allows the converter to operate in a good way. The aim of this part is to study and control the current through the inductor and the voltage in the first bus.

III.1. Current control

The current control is an important issue for the good operating of the converter. Indeed, we considered in all our previous calculus that the inductor current could be approximated to its average value and that this value was a constant. As a consequence, this value has to be regulated in order not to be divergent. That is why we have to add a current control loop to our system.

III.1.a. Transfer function

The first step is to calculate the transfer function H(p) linked to the current. But here, as the system is non-linear, we have to argue in a quasi-instantaneous regime. Thus it is necessary to introduce some new parameters taking into account the perturbations of the system. For the control in current, we considered that V1 and V2 were two ideal voltage sources.

$$I_{LAVG\,T} = I_{LAVG} + \widehat{\imath_L} \;\; and \; V_{LAVG\,T} = (\alpha + \hat{\alpha}) * V1 - (\alpha' - \hat{\alpha}) * V2 \quad (28)$$

With:
$I_{LAVG\,T}$: Average value of the current over a period
$\widehat{\imath_L}$: Disturbance of the average current over a period
α : Constant value of the duty cycle
$\hat{\alpha}$: Disturbance of the duty cycle over a period
α' : Complementary of constant value of the duty cycle $\alpha' = 1 - \alpha$

Then, the classic relation between current and voltage in an inductor applied to the average value:

$$L * \frac{dI_{LAVG\,T}}{dt} = V_{LAVG\,T}$$

$$L\frac{d\widehat{\imath_L}}{dt} = \underbrace{\alpha * V1 - \alpha' * V2}_{= 0\ (cf\ duty\ cycle\ definition)} + \hat{\alpha} * (V1 + V2)$$

$$L\frac{d\widehat{\imath_L}}{dt} = \hat{\alpha} * (V1 + V2)$$

With Laplace transform:

$$Lp * \widehat{\imath_L} = \hat{\alpha} * (V1 + V2)$$

Finally the transfer function:

$$H(p) = \frac{\widehat{\imath_L}}{\hat{\alpha}} = \frac{(V1 + V2)}{Lp} \quad (29)$$

This transfer function reveals that the comportment of the current is the same as a first order system. We know that by nature, this kind of system is stable. But in order to have a better approach, we decided to plot the Bode diagram.

Thus:

$$Gain_1(f) = 20\log|H(f)| \ with \ f = \frac{p}{2j\pi}$$

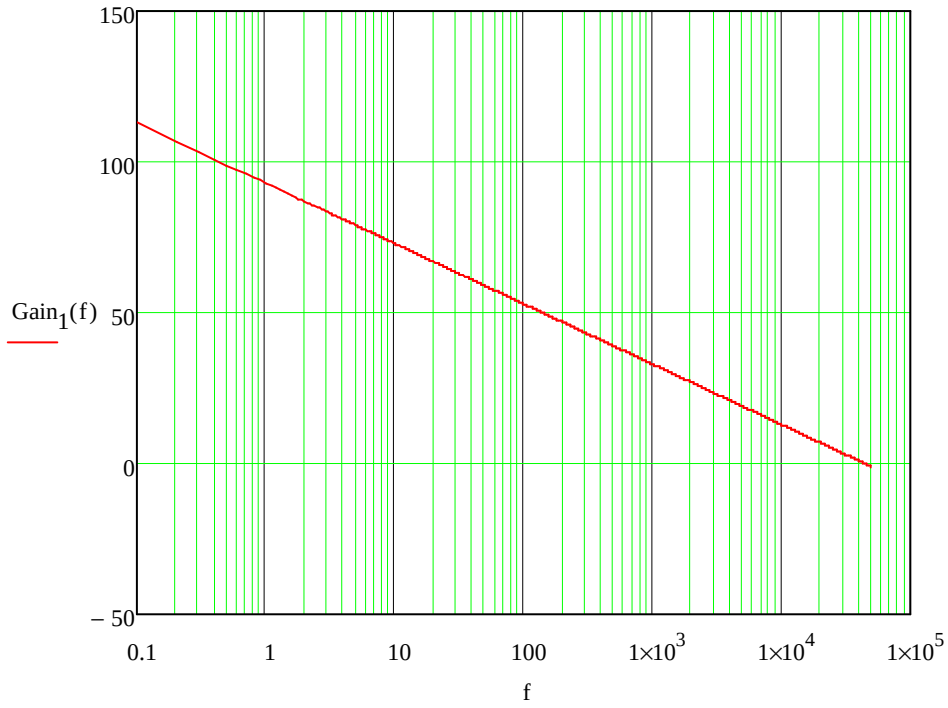


Figure 17:Bode diagram in gain of the current transfer function without error amplifier

This figure reveals that the system is stable and equivalent to a first order with a slope of $-20dB/dec$. But the problem is that the cut frequency (f_c) is higher than the frequency of our converter; $f_c = 44kHz > f = 20kHZ$.
That is why we have to design a error amplifier which will reduce the cut frequency. For better results and in accordance with Shannon law, we decided to impose $f_c = f/4 = 5kHz$.

III.1.b. Control loop

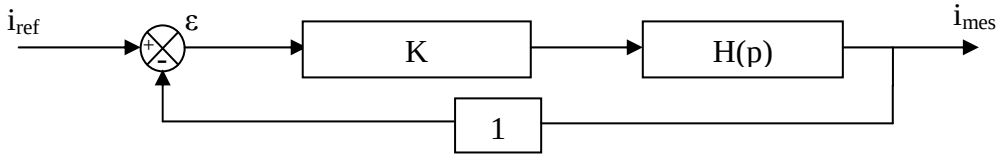


Figure 18: Block scheme of current control loop

Since the comportment of the current is such as a first order system, we just need it to design a proportional error amplifier in order to make the control loop.
The transfer function in open loop:

$$FTOL(f) = K * H(f) \ (30)$$

We aim to have $Gain_{tot1}(5kHz) = 0dB$

Thus:

$$|K * H(5kHz)| = 1$$

Finally:

$$K = \frac{1}{|H(5kHZ)|} = 0.113$$

Now the transfer function of the corrected system is given by:

$$H_{tot}(p) = \frac{0.113 * (V1 + V2)}{Lp} \quad (31)$$

In order to check if the correction is efficient, we plotted a new Bode diagram:

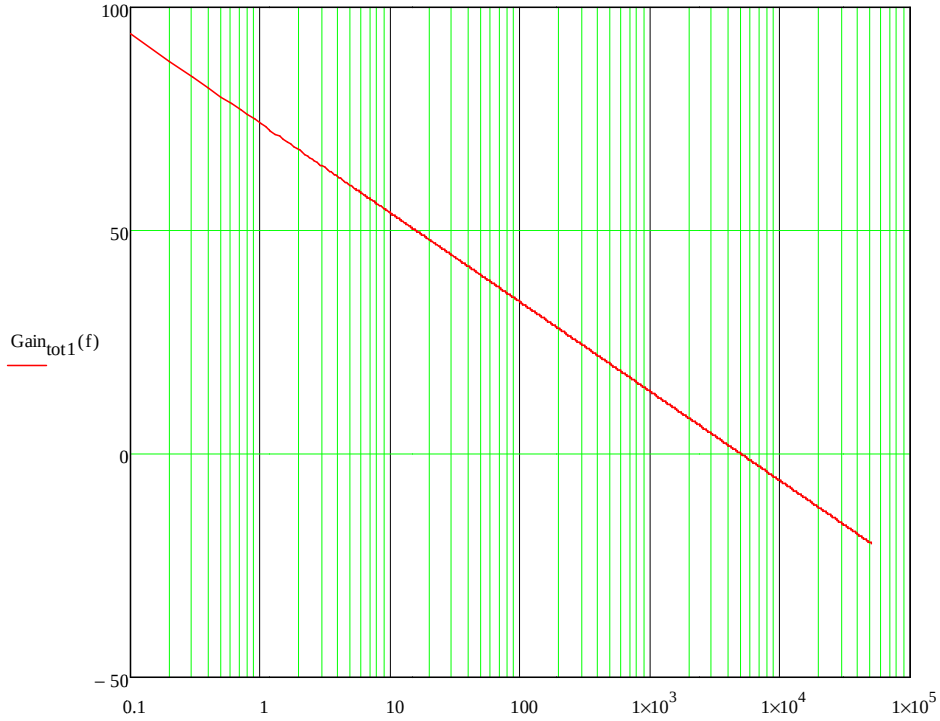


Figure 19 : Bode diagram in gain of the current transfer function with error amplifier

The system is still stable and the cut frequency is the one that we planned. As a consequence, we can say that the current control is efficient.

III.1.c. Practical realization

The classical design of a proportional error amplifier is given by:

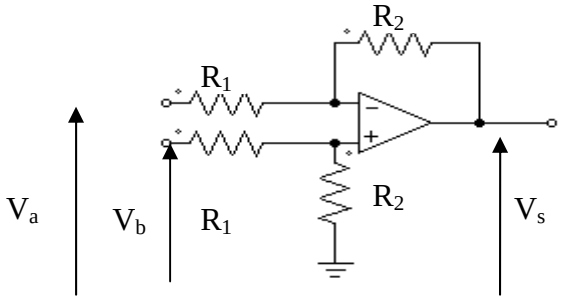


Figure 20: Proportional error amplifier scheme

We want to obtain:

$$K = \frac{V_S}{V_b - V_a} = 0.113$$

Using Millman theorem:

$$V_+ = \frac{\frac{V_b}{R_1}}{\frac{1}{R_1} + \frac{1}{R_2}} \quad and \quad V_- = \frac{\frac{V_a}{R_1} + \frac{V_s}{R_2}}{\frac{1}{R_1} + \frac{1}{R_2}}$$

Then if we consider the operational amplifier as ideal: $\varepsilon = V_+ - V_- = 0$
Thus:

$$\frac{V_b}{R_1} = \frac{V_a}{R_1} + \frac{V_s}{R_2} \quad thus \quad \frac{V_b - V_a}{R_1} = \frac{V_s}{R_2}$$

Finally:

$$\frac{V_s}{V_b - V_a} = \frac{R_2}{R_1} = 0.113 \quad (32)$$

To complete the design, we just have to choose a value of resistance high enough not to have a too high current. Moreover this resistance cannot be too high also because in this case there would be interferences.
Thus:

$$R_1 = 100k\Omega \ and \ R_2 = 11.3k\Omega$$

III.2. Voltage control

Once the current is controlled, we have to pay attention to the voltage in the first bus. Indeed, when the voltage source V1 is connected to bus 1 we have to be sure that the voltage in this bus does not oscillate too much. Moreover, if the voltage source V1 is unplugged from bus 1, it is necessary that the voltage in this bus does not collapse and remains equal to 200V. That is why we have to design a voltage error amplifier.

III.2.a. Transfer function

As has been done with the current, we have to calculate the transfer function G(p) of the system. The quasi-instantaneous regime approximation is still needed because the system is still non-linear. Now we cannot consider V1 as an ideal voltage source as a consequence, we have to consider a disturbance term. It is also necessary to model an equivalent circuit:

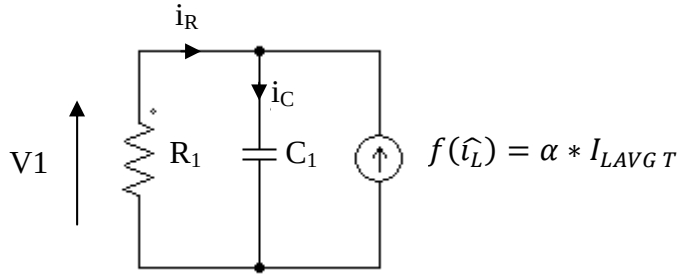


Figure 21: Equivalent electrical scheme

According to the switches states, the inductor which is symbolized as a current source provides current between 0 and αT. Moreover, in this part, the duty cycle is considered as constant.
Thus:

$$I_{CAVG\,T} = \alpha * I_{LAVG\,T} - \alpha\frac{V1 + \widehat{v1}}{R_1} - (1-\alpha)\frac{V1 + \widehat{v1}}{R_1} \quad (33)$$

The fundamental relation between current and voltage in a capacitor is given by :

$$C_1 * \frac{d(V1 + \widehat{v1})}{dt} = I_{CAVG\,T}$$

$$C_1 * \frac{d\widehat{v1}}{dt} = \alpha(I_{LAVG} + \widehat{i_L}) - \frac{V1 + \widehat{v1}}{R_1}$$

$$C_1 * \frac{d\widehat{v1}}{dt} = \underbrace{\alpha I_{LAVG} - \frac{V1}{R_1}}_{=0(DC\ component)} + \alpha\widehat{i_L} - \frac{\widehat{v1}}{R_1}$$

By Laplace :

$$C_1 p * \widehat{v1} = \alpha\widehat{i_L} - \frac{\widehat{v1}}{R_1}$$

Finally :

$$G(p) = \frac{\widehat{v1}}{\widehat{i_L}} = \frac{\alpha R_1}{1 + R_1 C_1 p} \quad (34)$$

In order to have a better idea of the comportment of the system, we plotted this function in a Bode diagram.

$$Gain_2(f) = 20\log(|G(f)|)\ with\ f = \frac{p}{2j\pi}$$

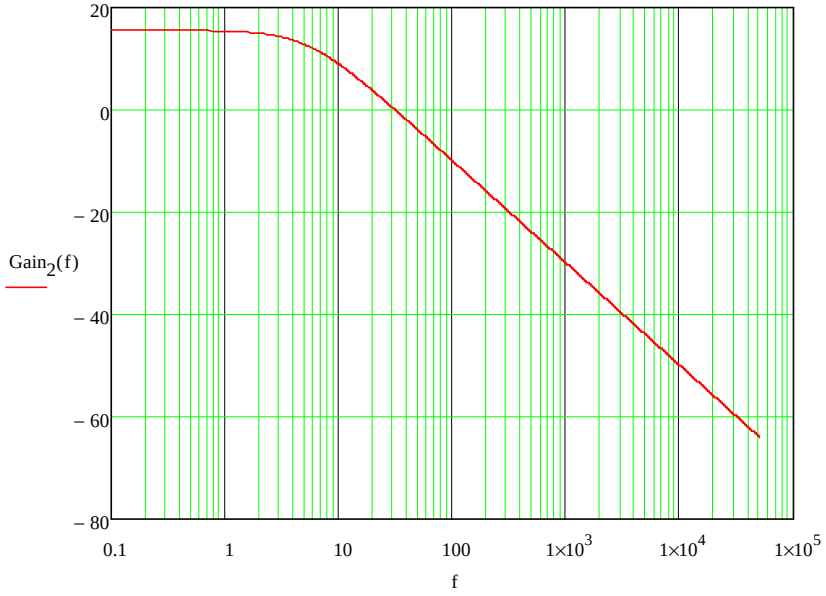


Figure 22: Bode diagram in gain of the voltage transfer function without error amplifier

The behavior of the voltage is the same as a low-pass filter. This type of system is stable, but if we want to have a good control on the voltage, this is not sufficient. That is why it is necessary to design an error amplifier which will make the behaviour of the system such as a pure integrator.
In order to realize this condition, we have to design the complementary high-pass filter; the filter which has the same eigen frequency.

III.2.b. Control loop

The high-pass filter can be designed as a proportional integrator (PI) error amplifier. Moreover, since the voltage measured in the first bus is equal to 200V, we had to reduce this value in the control loop. That is why we decided to apply a sensor gain to the system: $K_{sensor} = 1/100$, so that the voltage in the control loop is reduced to 2V which is a more acceptable value. Finally, the control loop is given in figure 23:

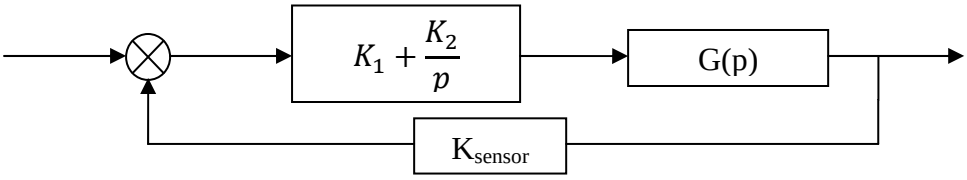


Figure 23: Block scheme of voltage control loop

Before calculating the transfer function in open loop, it is necessary to modify the expression of the transfer function of the PI.
Thus:

$$K_1 + \frac{K_2}{p} = \frac{K_1 p + K_2}{p} = K_2 \frac{1 + \frac{K_1}{K_2} p}{p} = K_1 * \frac{1 + \tau p}{\tau p} \quad (35)\ with\ \tau = \frac{K_1}{K_2}$$

As a consequence, the transfer function in open loop gives:

$$FTOL_2(p) = K_{sensor} * K_1 * \frac{1 + \tau p}{\tau p} * G(p) = K_{sensor} K_1 \frac{(1 + \tau p)\alpha R_1}{\tau p (1 + R_1 C_1 p)} \quad (36)$$

Thus, if we want to make a pure integrator, the condition is $\tau = R_1 C_1$=60ms. Once this condition is fixed, we also fix the cut frequency value $f_c = 5kHz$, so that we can calculate the value of K_1.

$$|FTOL_2(f_c)| = K_{sensor} K_1 \frac{\alpha R_1}{2\pi\tau f_c} = 1$$

$$K_1 = \frac{2\pi\tau f_c}{\alpha R_1 K_{sensor}} = 15708$$

These results revealed a high gain and a high time constant which seem not consistent to us. That is why we decided to plot another Bode diagram in order to be able to understand the operating of the overall system.

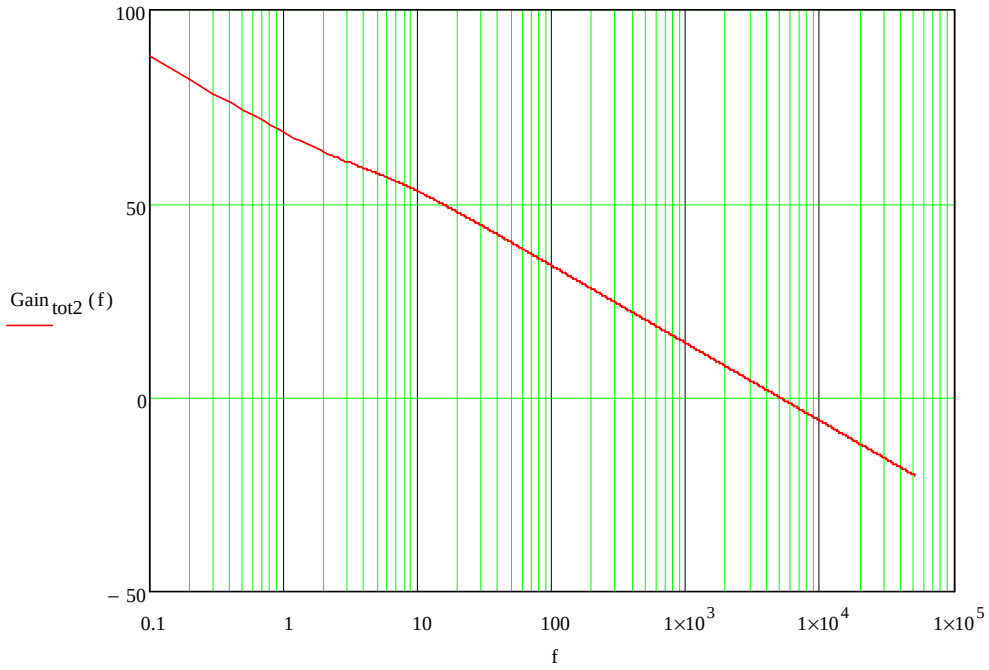
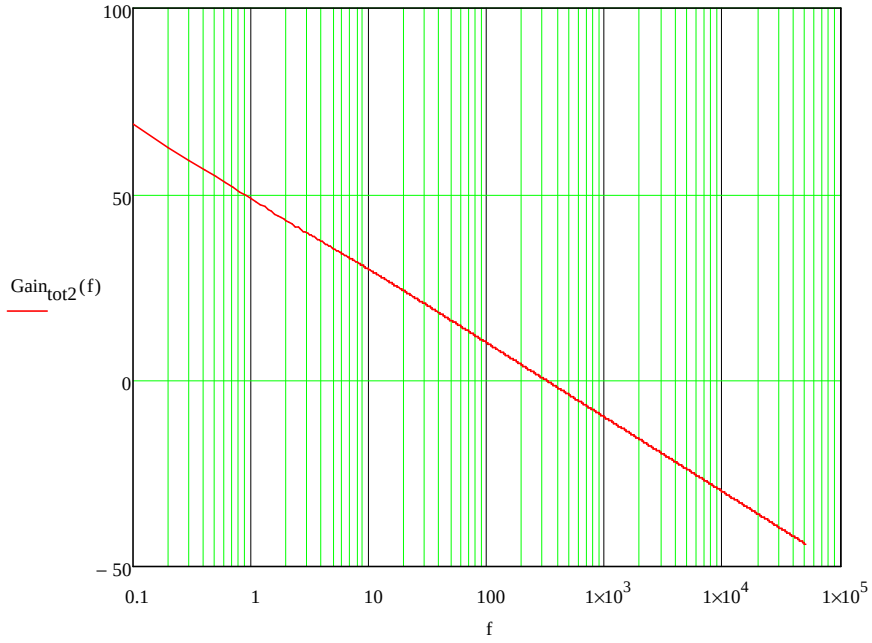
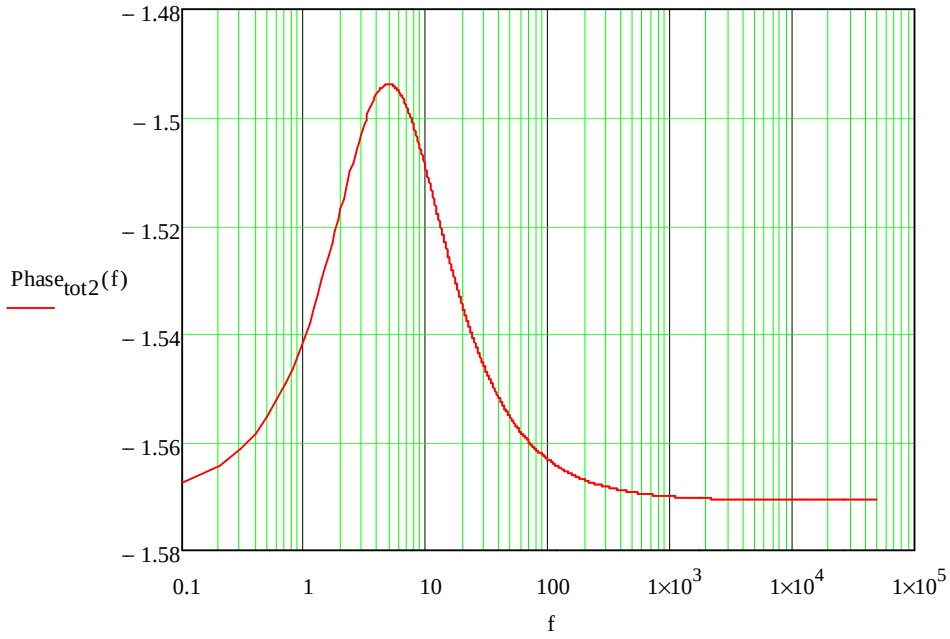


Figure 24: Bode diagram in gain of the voltage transfer function with error amplifier

This first approach of an error amplifier gives us bad results. Indeed the correction in low frequencies is not very efficient. Moreover, the simulation on PSIM confirms this observation. As a consequence, in order to design the best error amplifier, we decided to find the values of K_1 and τ which give the best results thanks to the simulation.
The best results are obtained with $K_1 = 500 \ and \ \tau = 5ms$. Now the Bode diagrams in gain and in phase are more consistent.



(a)



(b)

Figure 25: Bode diagram (a)in gain and (b) in phase of the voltage transfer function with error amplifier

The diagram in phase reveals that there is still an error for low frequencies, but this error is insignificant. Moreover, in the gain diagram, we can notice that the cut frequency has been decreased. But that does not matter since this value is still lower than the working frequency. It is now possible to begin the design of the real error amplifier.

III.2.c Practical realization

In this part, such as in part III.1.c. we used the classical representation for a proportional integrator error amplifier.

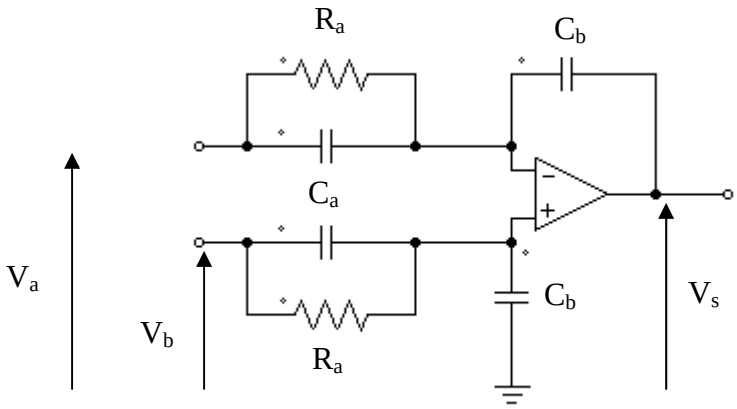


Figure 26: Proportional integrator error amplifier scheme

In order to be able to apply Millman's theorem, we have to simplify the diagram by finding the equivalent impedance for the resistors and capacitors associated in parallel.

The equivalent impedance Z is given by:

$$\frac{1}{Z} = \frac{1}{R_a} + jC_a\omega \;\; thus\; Z = \frac{R_a}{1 + jRC_a\omega} \quad (37)$$

As a consequence Millman's theorem gives:

$$V_- = \frac{\frac{V_a}{Z} + jV_sC_b\omega}{\frac{1}{Z} + jC_b\omega} \;\; and \;\; V_+ = \frac{\frac{V_b}{Z}}{\frac{1}{Z} + jC_b\omega}$$

Considering that the operational amplifier is ideal: $\varepsilon = V_+ - V_- = 0$
Then:

$$\frac{V_a}{Z} + jV_sC_b\omega = \frac{V_b}{Z}$$

And with equation (37):

$$\frac{V_s}{V_b - V_a} = \frac{1}{jZC_b\omega} = \frac{1 + jR_aC_a\omega}{jR_aC_b\omega} \quad (38)$$

Nevertheless, according to the definition of the proportional integrator error amplifier:

$$\frac{V_s}{V_b - V_a} = K_1 * \frac{1 + \tau p}{\tau p} \quad (39)$$

By identification :

$$\tau = R_aC_a \;\; and \;\; \frac{\tau}{K_1} = R_aC_b$$

Finally:

$$\tau = R_aC_a \; and \; K_1 = \frac{C_a}{C_b}$$

Since the laboratory of INEP owns capacitors with a capacity of 220pF, we decided to choose this value as a reference for C_b. And regarding the expected values of K_1 and τ, the final values are:

$$C_b = 220pF$$
$$C_a = 110nF$$
$$R_a = 45.45k\Omega$$

III.3. Control of the whole circuit and simulation results

Once all the different control loops are designed, it is necessary to plug them together to the converter. Figure 27 gives the final representation of the converter including the control loops, the low power system and all the loads that are needed.

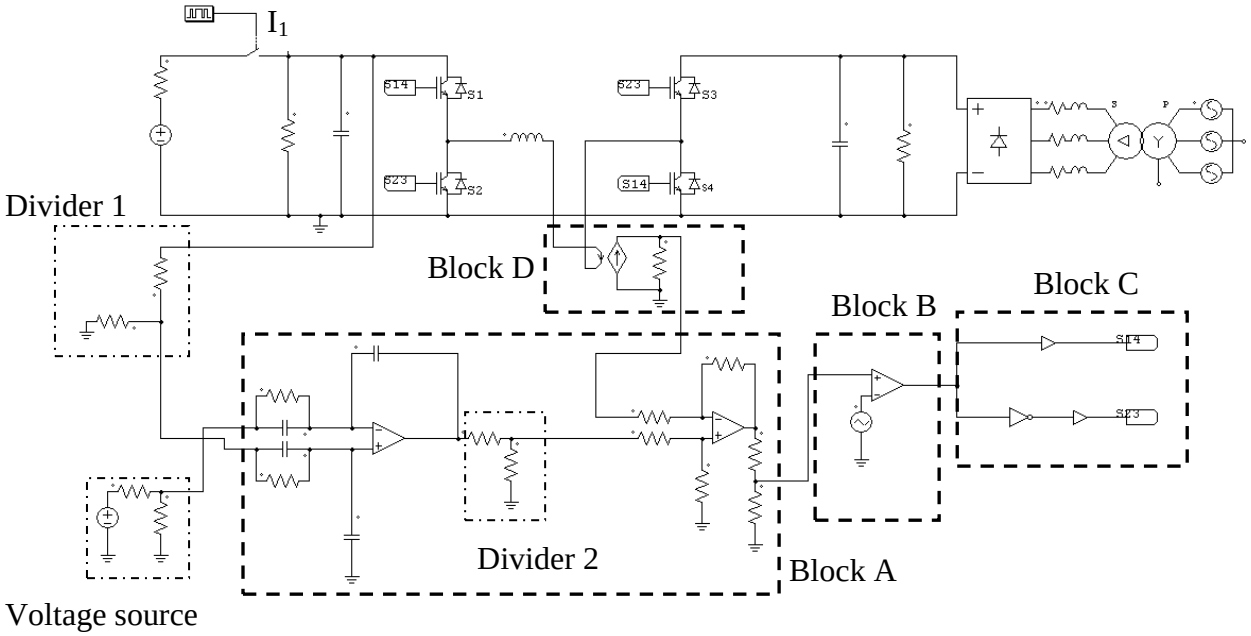


Figure 27:Scheme of the whole circuit including the error amplifiers

III.3.a. Description of the circuit

The power stage is well known since the beginning of this study. In this scheme we just added one switch (I_1) in order to highlight the two different power transfers. When I_1 is closed, the power flows from the left to the right and inversely when I_1 is open.
Then the low power system can be divided into 4 different main blocks which represent all the functions needed to realize the current and voltage control.

Block A: Current and voltage control with the two error amplifiers designed in the previous part.
Block B: Signal comparator which will generate the duty cycle required thanks to a triangular reference.
Block C: Drivers of the converter. Their aim is to generate an impulsion with the right duty cycle which will influence the opening and the closing of the 4 IGBT.
Block D: Current sensor. This component measures the current and transform this current into a voltage that can be used by the operational amplifier.
Moreover, since the voltage in the first bus is equal to 200V, it is impossible to have such a high value in the input of the first operational amplifier. That is why we had to design a voltage divider with a ratio of 1/100. On the other hand, the output voltage of the first operational amplifier is equal to 15V which is once again too high for the second amplifier. But, since the gain of the current sensor of block D is equal to 0.2 and the current is almost equal to 20A in the power stage, we will have to design a divider with a ratio higher than 4/15 in order to make the control loop efficient. Thus we choose a ratio of 5/15 which is easy to design. Figure 28 gives the common scheme of a voltage divider.

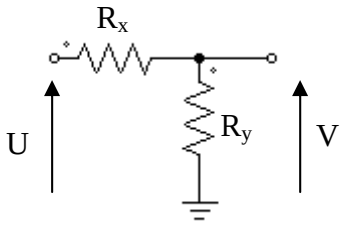


Figure 28: Scheme of a voltage divider

Thus, according to the classic formula:

$$\frac{V}{U} = \frac{R_y}{R_x + R_y} \quad (40)$$

Then, if we consider divider 1 which has a ratio of 1/100, since the voltage is equal to 200V we have to use a high value for R_x if we want to keep the losses under an acceptable value. That is why we chose:

$$R_x = 19.8k\Omega \ \ and \ R_y = 200\Omega$$

With these values, the power losses are rated as:

$$P_R = \frac{200^2}{19800} = 2.02W$$

This value is acceptable, we will keep the two resistors which have been calculated.
And for divider 2, which has a ratio of 5/15: $R_x = 1k\Omega \ \ and \ R_y = 500\Omega$
The last component is the voltage source which is used as a reference for the first operational amplifier. This voltage source provides a voltage of 2V.

III.3.b. Final simulation

The results of the first simulation were not very good. Indeed, the current control was not efficient at all and the converter was not operating. The reason of this problem is that in the calculus of the gain in current control, we have to consider the operational amplifier, the comparator, the current sensor and the output limiter. As a consequence, we had to recalculate the values of $R_1$and R_2.
If we call G the gain of the operational amplifier, G' the one of the comparator, G'' the one of the current sensor and G''' the gain of the output limiter. Then in the current control loop, we have the relation between these 4 gains and the real gain expected K as it was calculated:

$$G * G' * G'' * G''' = K = 0.113 \quad (41)$$

For the current sensor the gain is given by the data sheet and G'=0.2.
For the limiter, since the value of the upper resistor equals 2,75kΩ and the lower one equals 1kΩ, we have:

$$G''' = \frac{1}{3.75}$$

Finally, the gain for the comparator is approximated by the formula:

$$G'' = \frac{1}{\overline{V_r}}$$

With $\overline{V_r}$ the mean value of the reference triangular signal in the comparator, $\overline{V_r} = 2.3V$
Consequently, the new value of the gain for the operational amplifier is given by:

$$G = \frac{R_2}{R_1} = \frac{0{,}113}{G' * G'' * G'''} = 4.87$$

Thus,

$$R_1 = 10k\Omega \; and \;\; R_2 = 48.7k\Omega$$

Now, the simulation results which are shown in figure 29 give us satisfaction.

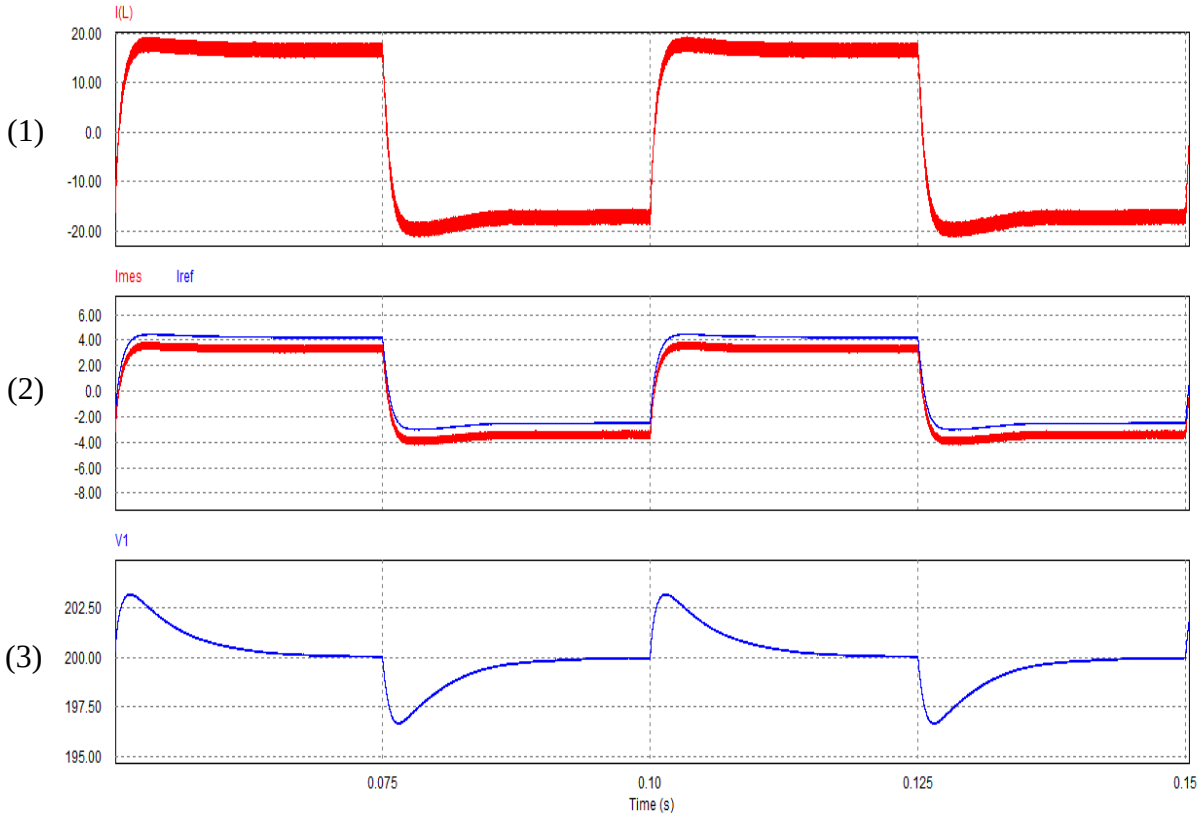


Figure 29: Simulation results for DC/DC converter.(1) current in the inductor,(2) reference current and measured current at input of the second operational amplifier,(3) voltage in the first bus.

These graphs reveal the good operating of the converter. Indeed, in the first half period, when I_1 is closed, the current reaches its expected average value of 16.7A quickly and the peak to peak value (ΔI_L) is maintained below the fixed value of $0.2I_{LAVG}$. Also, we can notice thanks to the second graph that the error amplifier is efficient. Moreover, the voltage in the first bus has the expected shape, the overshoot is contained and it reaches the 200V value required for good operating quickly enough so that we can consider the signal as a DC component.
Then, when we open I_1 which corresponds to the second half period, the power flow is reversed. But we can observe that the converter has a good response because the first bus voltage is still maintained at 200V.
Now we can say that our converter is operating. We can start the designing of the low power circuit with real components.

IV Design of the low power circuit

Once the converter is considered as operating by simulation, it is necessary to select the right components for the low power circuit. Indeed, we have to select components which are manufactured by factories and then we have to adapt them to our specific system. In this part, we will study each block which has been defined in part III.3.a. Each one is related to a specific component that needs to be studied.

IV.1. Block A

This block is the one which contains the two error amplifiers. In order to practically realize those error amplifiers, we had to choose a component that provides operational amplifiers and then to plug the right pins with the resistors and capacitors we calculated. Thus we choose a component which was available at the lab. This was **LF347,** manufactured by **Fairchild Semiconductor Corporation**. This component provides four operational amplifiers so that we can use two of them and disconnect the two others without having any problem in the operating of the circuit.
Figure 30 illustrates the shape of this component:

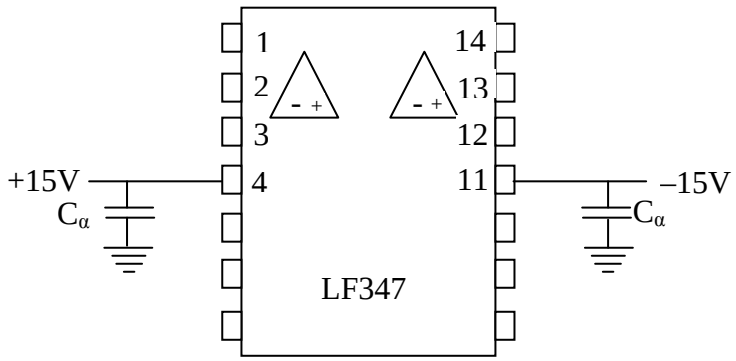


Figure 30: Operational amplifier component

In this component, pin 1, 2 and 3 are respectively the output, the negative and the positive input of the first operational amplifier; so as pin 14, 13 and 12 for the second one.
Then, pin 4 and 11 are respectively used for positive and negative power supply. According to the data sheets [8], we chose a value of 15V and –15V.
Finally, we can observe that we added a capacitor in each supply. The aim is to absorb a possible peak of current which could destroy the operational amplifier.

IV.2. Block B

This block is made of an integrated circuit which will compare the output signal of the second operational amplifier to a carrier signal in order to get in output of this component a signal generated with the frequency we calculated at the beginning (f=20kHz).
In this part, we decided to use the integrated circuit **UC 3525** manufactured by **Fairchild Semiconductor Ltda**.
Its shape and the connections we made are given in figure 31:

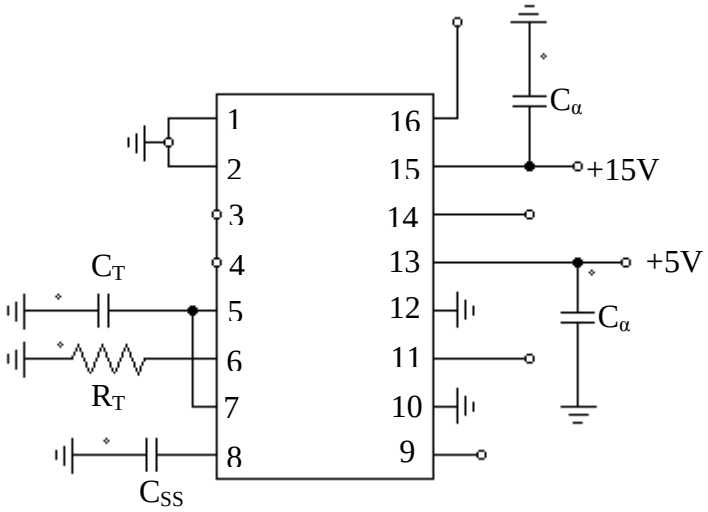


Figure 31: Integrated circuit UC3525

Pin 1 and 2 are both the input of an internal logic component we do not want to use that is why it is connected to the ground. For the same reason pin 10 which corresponds to the shut down is also plugged to the ground. Then pin 12 is the overall ground of the component.
Then pin 3 and 4 are left open because they have no influence on the operating of the system in this state. Practically, they correspond respectively to the synchronization and the output of the carrier. Concerning pin 5 and 6, we have to plug the accurate resistor and capacitor in order to obtain the right carrier frequency. The data sheet of the component [6] gives us a formula which allows to calculate these values:

$$f = \frac{1}{0{,}7 * R_T * C_T}$$

Then we fixed the value of C_T so that we can calculate R_T. Thus,

$$C_T = 6.8nF \;\; and \; R_T = 10.5k\Omega$$

Pin 7 corresponds to the discharge of the oscillator and pin 8 is relative to an eventual soft start.
Pin 9 is the input of the integrated circuit, it is connected to the output of the second operational amplifier which provides a signal with the right duty cycle but with an inappropriate frequency. Pin 11 and 14 are the outputs of the system, here the corrected signal with the right frequency is obtained.
Pin 13 and 15 are two power supplies of respectively 5V and 15V. The first supply is used to limit the output signals to an amplitude of 5V whereas the second one is used for the operating of the component.
Finally, pin 16 provides a reference voltage of 5V which is used as reference in the voltage control loop.

IV.3. Block C

Block C is composed of two different components. First the inverter which will invert the signal provided by pin 11 and 14 of the integrated circuit so that we have two complementary signals. Then the driver which receives the two signals and generates two other signals that can be read by the IGBTs.

IV.3.a. Inverter

To perform the inversion, we chose the component **SN 5404** manufactured by **Texas Instrument Corporation** [7]. It is composed of 6 blocks of two pins. Each block makes one inversion.

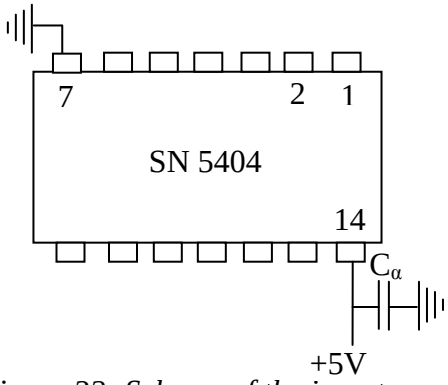


Figure 32: Scheme of the inverter

This component operates with a supply of 5V. Pin 1 is the input of the inverter, this pin receives the signal from pin 11 and 14 of the integrated circuit. Pin 2 is the output of the inverter, this pin provides the inverted signal to the driver we will study in the next part.

IV.3.b. Driver

Once the compared signal is created, this one has to be driven to the IGBT in order to perform the voltage and current control, but also in order to make the converter operate. Thus we need to use a driver which will generate a signal that can be read by the IGBTs. Indeed, the IGBT operate with a square signal. When it receives the impulsion, the IGBT gets close. When the signal reaches zero, the IGBT gets open. To design this signal, we decided to choose driver **SKHI 23/12** manufactured by **Semikron Ltda** whose shape is given in figure 32.

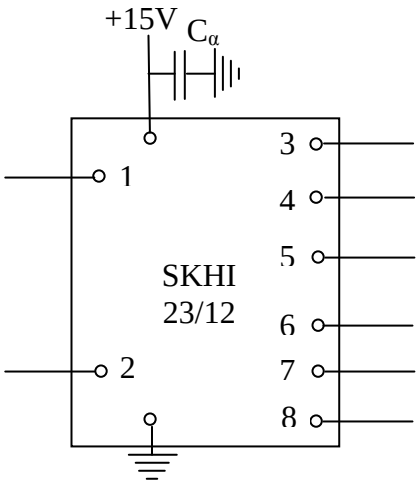


Figure 32: Scheme of the driver

This driver has two inputs (1 and 2), 6 outputs (3, 4, 5, 6, 7, 8) and needs a 15V power supply such as in the operational amplifier.

According to the datasheets [10], this driver can be separated in two parts: the upper part and the bottom part with one input and three outputs each. The upper part will generate a signal that will be used to drive IGBT 1 and the bottom part will generate the complementary signal that will be used to drive IGBT 2. We use a second driver for IGBT 3 and 4.
Practically, the upper input receives the compared signal from the integrated circuit and we will get in output: for $0 \leq t \leq \alpha T$ a Heaviside impulsion and for $\alpha T \leq t \leq T$ a null impulsion. Conversely, the bottom part receives the inverted compared signal and since it has the same logic as the upper part, we will get in output a null impulsion for $0 \leq t \leq \alpha T$ and a Heaviside impulsion for $\alpha T \leq t \leq T$.
But these Heaviside impulsions are not perfect, there is a time called dead time during which the signal is increasing. The drivers are built in order to have a dead time equal to 10µs. But this value was too high for our system. Hopefully, we can influence this value by adding two accurate resistors. Finally, after consulting the datasheets and since the period of our signal is equal to 50µs, we decided to fix the dead time to 2.5µs which corresponds to the add of two resistance of 33kΩ.

IV.4. Block D

This block is essential in the current control. Indeed, since we cannot directly control the current with the error amplifier which has been designed, we need to transform the measured current into a readable voltage. To perform this, we used the component **LA 25–NP** which is a current sensor manufactured by **LEM**. Figure 33 illustrates the shape of this component.

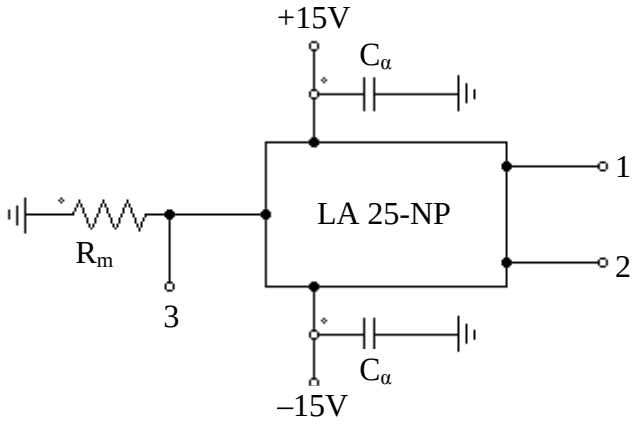


Figure 33: Scheme of the current sensor

This component has a double function. First it measures the current flowing in a wire between points 1 and 2. And then, this current is transformed into a voltage signal whose output is point 3. Moreover, the other advantage of this component is that we can adjust the gain to a suitable value. Indeed, if the current in the power stage is considered as equal to 20A, according to the datasheets [9], the gain of the component is equal to 0.001; and in order to adjust the gain, we just have to change the value of the resistor R_m. In our case we choose R_m=200Ω so that the overall gain is increased to 0.2 such as it has been considered for the final simulation in part III.3.b.

IV.5. Power supply

All the components we studied before need a power supply of 15V or 5V. We have two options to design these supplies. The first one is to take two different supplies, one of 15V and another of 5V. But this solution is too expensive and takes too much space. The second option is to use only one power supply of 15V and to make a specific assembly to get 5V when it is needed. To design this assembly, we need a new component which is **LM7805** manufactured by **Fairchild Semiconductor Ltda**. This component operates as voltage divider made with resistors, but its advantage is that it provides 5V in output even if the input voltage varies.
According to the datasheets [12] the input voltage can vary from 7V to 21V. This solution is cheaper and quite flexible. As a consequence, we decided to select it in order to obtain our 5V supply. Figure 34 illustrates the connection which is necessary for this assembly.

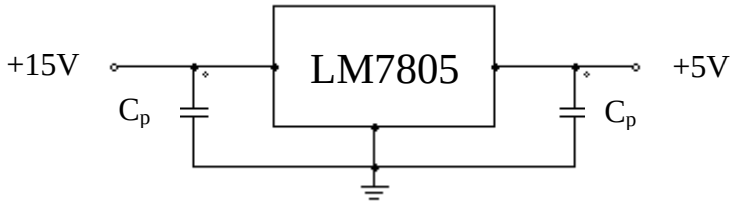


Figure 34: Scheme of the 5V power supply

To operate, the two components just have to be plugged to the 15V supply. But in order to get the best signal and to protect these components, we decided to add two electrolytic capacitors (C_p) with a capacity of 1mF so that we avoid any possible peak of current.

IV.6. Overall connection

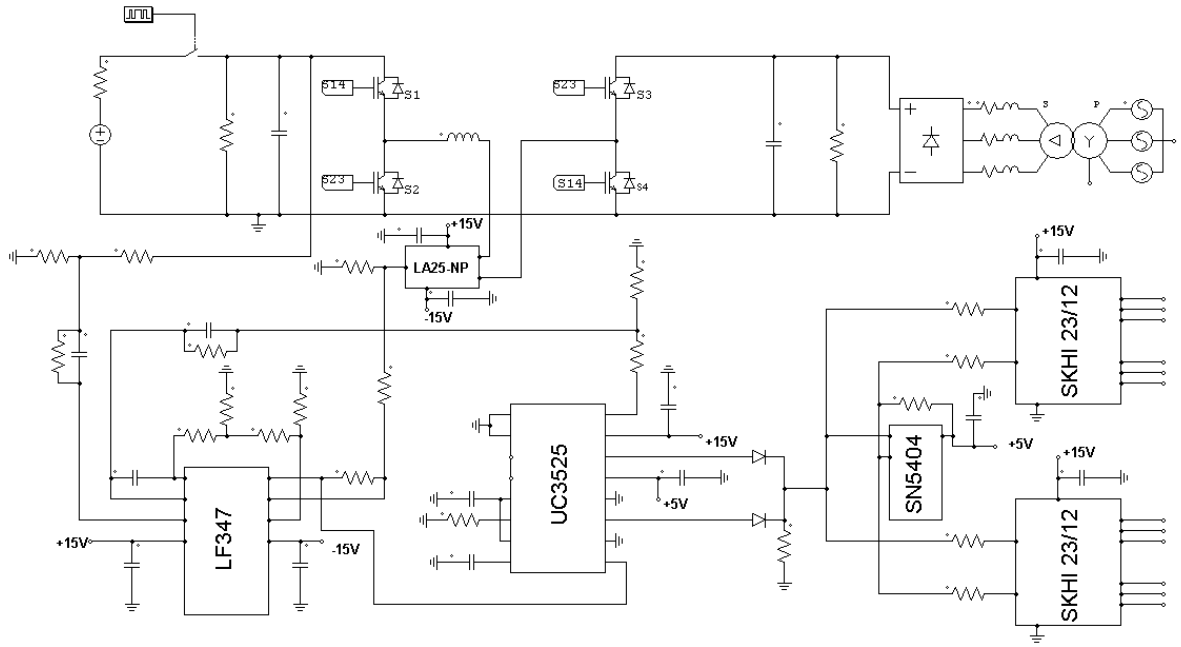


Figure 35: Scheme given to the technician for the building of the converter

Figure 35 illustrates the final scheme of our converter. We can notice some modifications. First, in order to protect the drivers, we decided to put resistors of 1kΩ before each input. Then, we also had to sum the two output signals of the integrated circuit. Indeed, we noticed that the logic of the each output was made to provide a duty cycle between 0 and 0.5. Since we want a duty cycle of 0.6, it was necessary to add the two outputs. Thus each output provides a duty cycle of 0.3 and the right duty cycle is obtained after summation.
Finally, we can notice that we add two resistors, one in the output of the two diodes we just studied and one between pin 2 and 14 of the inverter. The aim of these resistors is to prevent the input signal of the drivers from reaching a null value. Indeed, the logic of these components would not “understand” such a command and so the output gate signals will not be correct and the converter will not operate at all. These resistors impose a kind of offset.
Now the converter can be built and the test phase can be started. The scheme and table given to the technicians are represented in appendix A and B.

V Construction of the converter and final tests

Once the converter is fully designed and constructed, it is necessary to test its operating step by step in order not to break down our system. That is why we first decided to test the low power circuit in order to know if the gate control was effective. The following step was testing the converter in open loop with two distinguished states of power; one when power flows from V2 to V1 and the other one when power flows in the opposite way. Then the close loop test will reveal the efficiency of the control. And the final test will highlight the behavior of the converter when the power flow is inverted. In this part, all the measures are provided by an oscilloscope available at INEP workshop. Unfortunately, it was impossible to get the axis and grid with the waveforms, that is why we had to draw fictive axis.

V.1. Print board tests

The aim of these tests is to check if the gate signal provided to the IGBTs is correct. It means that it is provided with the right duty cycle and frequency.
First we had to adjust the output frequency of the integrated circuit. Indeed, with the calculated parameters the frequency was equal to 23kHz. Thus we had to adjust the resistor R_T and capacitor C_T. By experimentation, the values that provide 20kHz are:

$$R_T = 11k\Omega \ and \ C_T = 3.3nF$$

Then we tested the saturation of the operational amplifier. Indeed, it is necessary to know if they saturate at the right voltage to avoid an over voltage in the next component. To conduct this test, we disconnected one of the input and the other one was feed with a potentiometer which forced the saturation. This test revealed that the saturation had the expected value of 12V.
The next step was to add a diode between pin 9 of the integrated circuit and the ground not to have negative values for the input voltage.
Finally the print board was tested and the output signals of the drivers were those expected, so that the IGBTs receive the right gate signal.

V.2. Open loop tests

Once the print board is tested and validated, the tests on the power stage can be started. Here, we first took some precautions and began the tests with low voltage and power. The aim was to check the operating of the overall system without risks of breaking it.
Since the component **LF347** (figure 35) was disconnected from the print board, there was no input signal in pin 9. But we needed to use the print board to drive the IGBTs. As a consequence, we decided to replace the output signal of **LF347** which is connected to pin 9 of **UC3525** by a perfect source provided by a potentiometer. Before turning on the power stage, we made some adjustments with the potentiometer in order to have the gate signal expected. Then the operating was tested with low power and voltage to be sure that the whole circuit was operating.
The electrical and thermo results were conclusive, as a consequence it was decided to initiate the experimentation with the nominal power (2kW) and voltages (200V in first bus and 300V in second bus).

V.2.a. Power flows from V2 to V1

In this test the voltage provided in bus 2 is equal to 300V. The important parameters are the current through the inductor, the voltage across the IGBTs and the voltage in the first bus. We measured each of these and obtained the waveforms of figure 36.

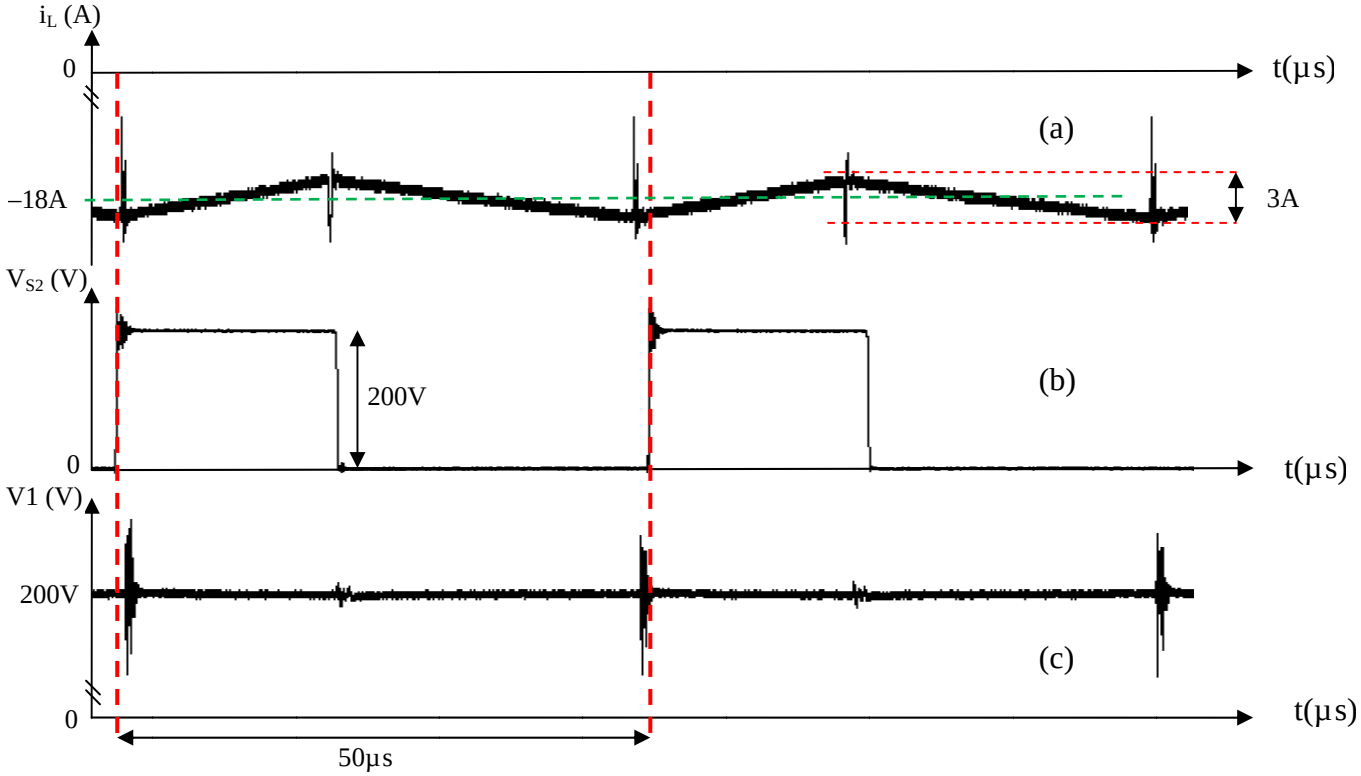


Figure 36: Waveforms of current in the inductor (a), voltage in switch S2 (b) and voltage in bus 1 (c)

These waveforms reveal that the operating of the converter is good. Indeed, the signals are the ones expected even if the overshoots are quite large when switch S2 turns off. Here the amplitude of the overshoots cannot be trusted because we used a low resolution mode from the oscilloscope so that it can be considered as noise.
If we pay more attention to the numerical values, we observe that the current ripple is low. The converter has been designed to operate with an error of 20% on the current. The experimentation reveals a peak to peak value of 3A and a RMS value of 18A. As a consequence the error is equal to 16.6% which is completely convenient.
Nevertheless, the 18A measured through the inductor is a higher value than the one expected, but since the components are not perfect, this value can be considered as valid. Also, the value is negative because of the power flow.
Finally, the average voltage in the first bus is rated to 200V with a low ripple. The only negative point is that the overshoot is a little large when S2 turns off. Except for this overshoot, the results were satisfactory and we can ensure that the converter is operating in this way of power transfer.

V.2.b. Power flows from V1 to V2

In this test, bus 1 is fed with 200V. The parameters are the same as in the previous part, they are given in figure 37.

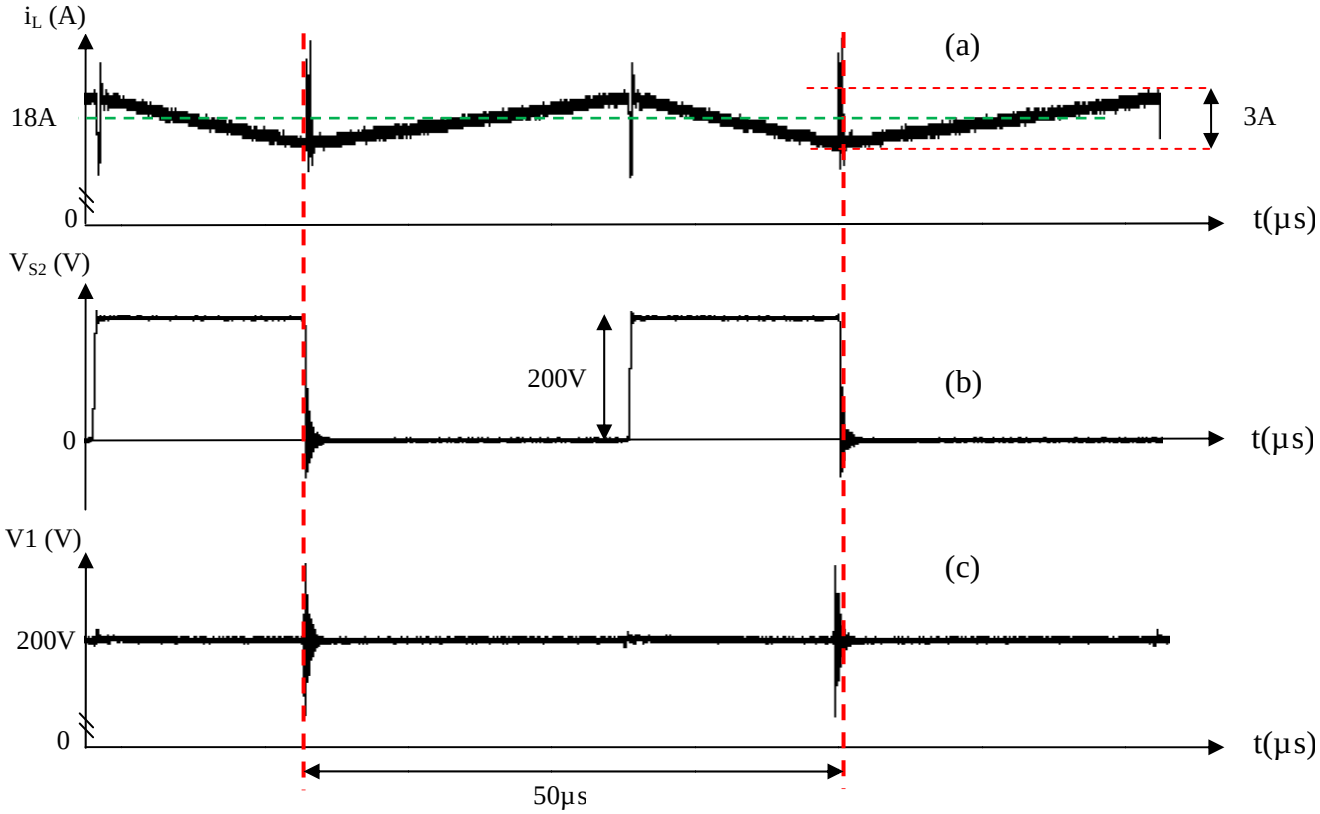


Figure 37: Waveforms of current in the inductor (a), voltage in switch S2 (b) and voltage in bus 1 (c)

In this case, we can make the same observations as in the previous part. Indeed, the waveforms are those expected and the numerical values are conserved even if the power flow is reversed. We can just notice that now the current through the inductor is positive which is consistent with the inversion of power flow. Moreover the main overshoot can now be observed when switch S2 is closing.
If we do not pay attention to the noise due to the oscilloscope, these two experiments allow us to conclude that the converter is operating in both way of power transmission. The next step is the experiment including the control loop to verify its efficiency.

V.3. Close loop tests

Once the operating of the converter has been checked with the open loop test, it is necessary to conduct the tests in closed loop. We had to be very careful with this test. Indeed, we know that the current control is turned on only if the output signal from the current sensor reaches a value of 2.6V; it means that the current through the inductor has to reach at least 13A since the gain of the current sensor is equal to 2.6V. That is why, we had to design a starting protocol in order to avoid over current in the system.

V.3.a. Experimental protocol

To conduct the close loop test, we had to pay attention to the current through the whole circuit because an over current could have broken the system. The other issue is that the voltage source we used in bus 2 could not provide a current higher than 15A. Moreover, we noticed that when the converter starts operating the voltage in bus 1 immediately reaches 100V. As a consequence, if we impose 2kW the current in bus 1 has to reach:

$$I = \frac{P}{U} = \frac{2000}{100} = 20A$$

We understand that the voltage source cannot provide such a current. That is why we had to decrease the bus 1 load to 1.5kW. This adjustment has no influence on the final waveforms of the voltage in bus 1.
Then we proceeded to the start up of the converter. After turning on the load and the low power circuit we imposed a low voltage thanks to the source. Since the source we used is equipped with a current limiter, it was necessary to increase this limit to the maximum value of 15A. Then we increased slowly the voltage and noticed that the current was increasing very fast.
Finally once the current reached 13A, the converter started operating and this matter of "soft start" was over.

V.3.b. Power flows from V2 to V1

The control loop test can only be done in one way. Indeed, the aim of the voltage control loop is to regulate the voltage in the first bus to 200V. As a consequence, if we make the test when power flows from V1 to V2 with a perfect voltage source providing 200V in the first bus, there is no need to have a control operating. That is why we only did the test of power flowing from V2 to V1. After using the starting protocol we described before, we obtained in permanent regime the waveforms of figure 38:

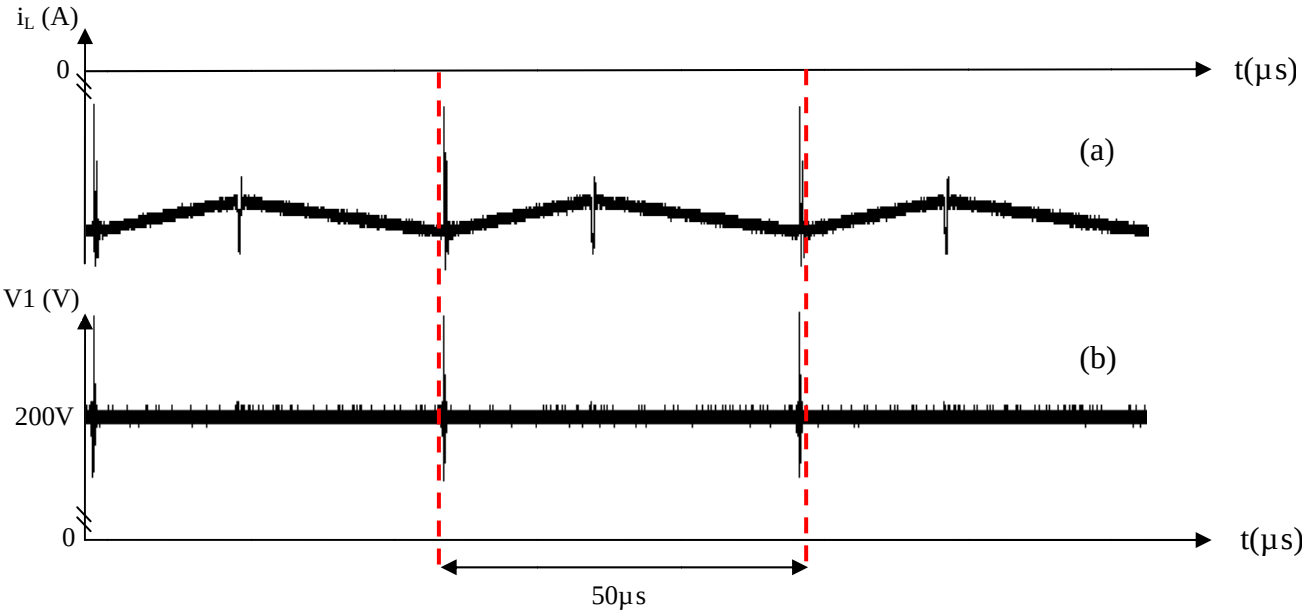


Figure 38: Waveforms of current in the inductor (a) and voltage in the first bus (b) in close loop test

The results gave us complete satisfaction. Indeed the converter is operating with a high level of power and the waveforms of current and voltage have the shape expected. If we do not pay attention to the noise in each signal due to the low resolution of the oscilloscope, we can say that the control in current and voltage are both really efficient. The overshoots are not too large anymore and during the experiment, we observe that as soon as the converter starts operating (as soon as the IGBTs started commutating), the voltage in bus 1 is immediately regulated to a DC component. With regard to the numerical values, bus 1 voltage reaches 204V and the current ripple reaches 3A. So the converter is operating and meets the conditions set at the beginning.

V.4. Thermo test

If we want to be very precise in the design of a power electronics system, it is necessary to measure the temperature of the prototype. Indeed, this converter has to be designed for a long time of operating and we have to be sure that the temperature will not pass a critical value that could break fragile components. In our case the most valuable components are the IGBTs. We have to be sure that the temperature of the system will not be higher than 125°C which is the highest operating temperature for the IGBTs. Figure 39 shows our measurements:

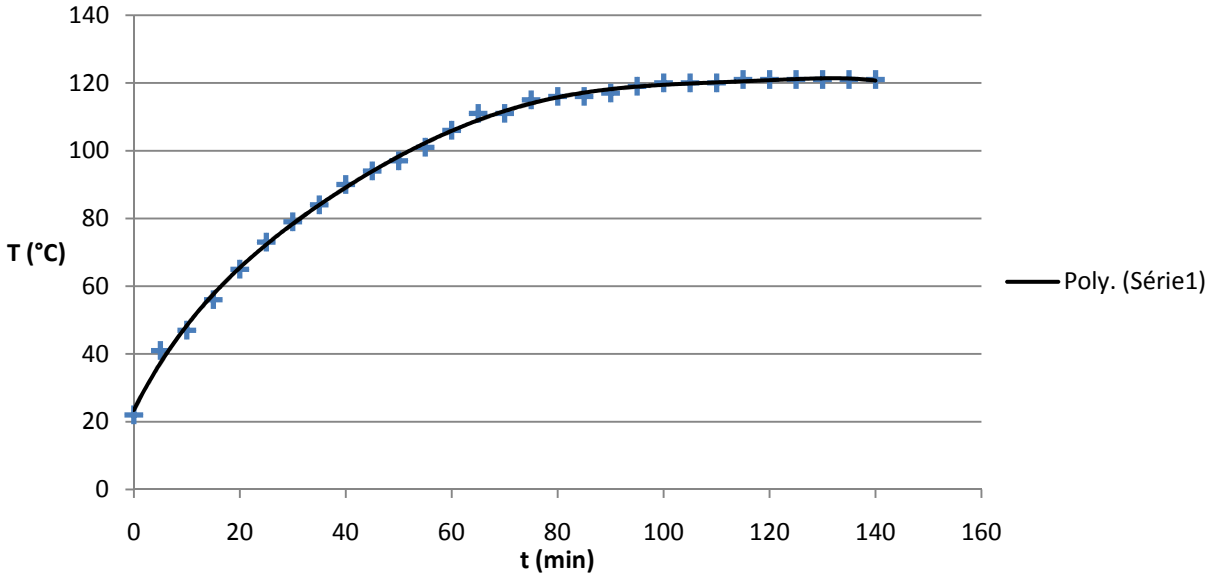


Figure 39:Evolution of the temperature of the heat sink

The first observation is that the temperature does not reach the critical value and that a steady-state regime is obtained after 120 minutes of operating. Even if the highest value seems to be very close to the critical value, we observed that the converter was still operating well and we can assume that the contact thermometer we used provided us an error of measurements.
Then we can say that the behavior of the system can be compared as a first order system which reaches a permanent state.
Finally all the results we got in the last three parts allow us to say that our converter is operating well. We can now try the final test which consists in inverting the power flow.

V.5. Final test: reversion of power flow

In this test, we used the same start protocol as has been described before except that the voltage source of the previous part was plugged to V1. For the start process, the switch we can see in figure 35 in output of the voltage source is first closed. The load was still fixed to 1.5kW. Once the voltage in bus 1 was equal to 200V we started the feeding of bus 2 and fixed its value to 300V. Then once the converter is in permanent regime, we can proceed to the reversion of power flow by successively turning on and turning off the switch. The results are given by figure 40:

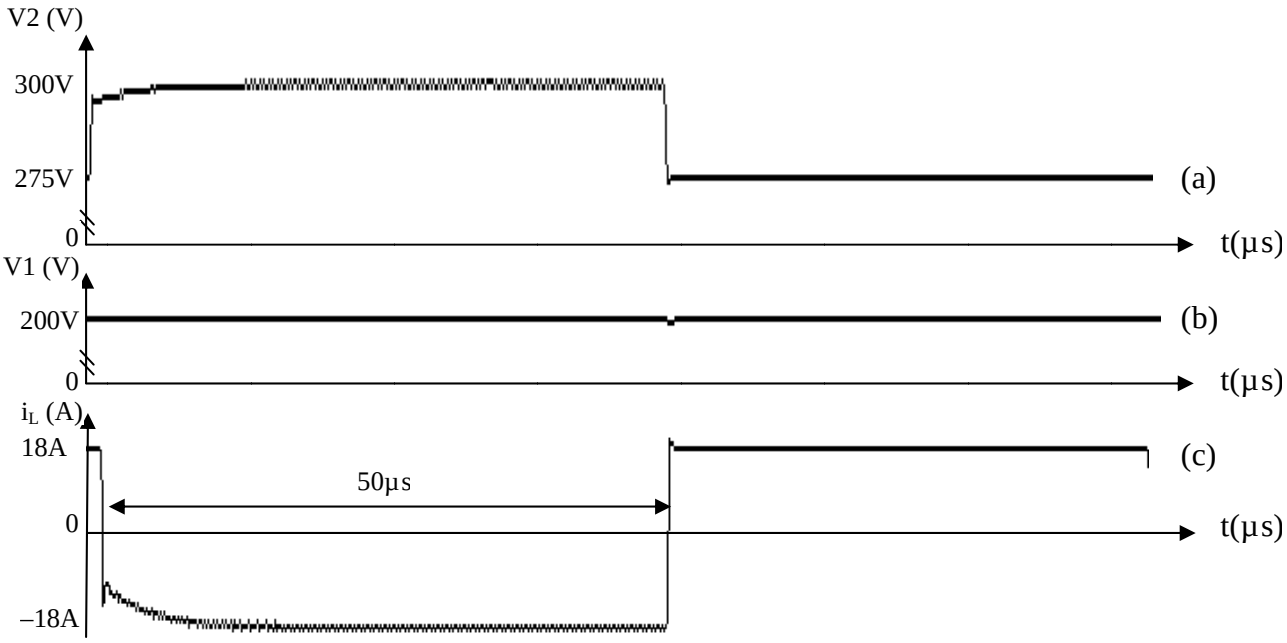


Figure 40: Waveforms of the voltage in second bus (a), first bus (b) and current through the inductor (c)

This test allows us to understand the dynamic response of the system to a fast change of state. The first part of the waveforms provides the dynamic response of the system when the source V1 is connected whereas the second part corresponds to the disconnection of the source V1. Moreover, this time we used the high resolution mode of the oscilloscope.
These waveforms reveal that in both cases (source V1 connected and disconnected), the system provides a fast response to the change of state. Moreover, we can notice that both current control and voltage control of bus 1 are very efficient and that the overshoots are maintained under an acceptable value. Besides, these waveforms have the same shape as the simulations waveforms. We have a great concordance between practical and theoretical results. The only difference is about the numerical values but since the components we used are not as perfect as they are considered to be in the simulation we can ensure that the results are acceptable.
Then, we can observe that the voltage in bus 2 is decreasing when the switch is opened. This can be explained by the fact that bus 2 has to feed its own load but also the load of bus 1 in order to maintain the 200V voltage in bus 1. It can also be due to a bad efficiency of the transformers used to feed bus 2.
Finally, we decided to reduce the time step of the oscilloscope in order to have a better view on a possible ripple on each signal.

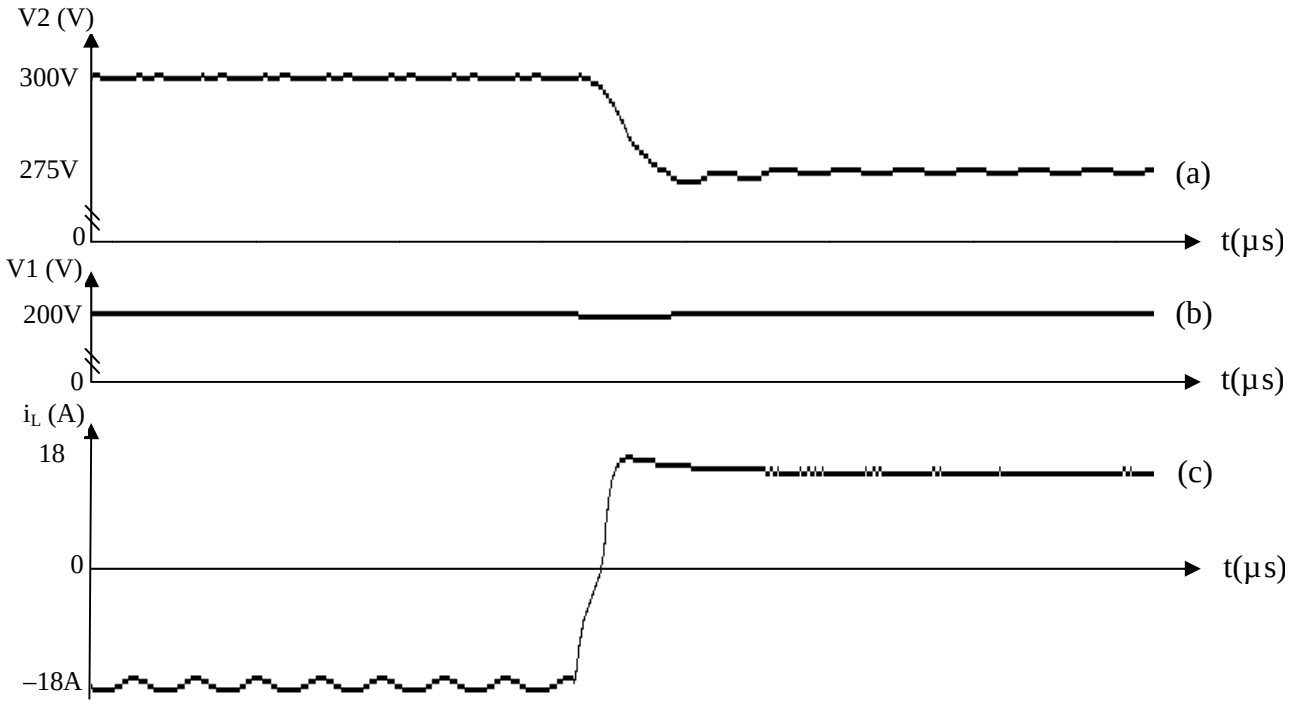


Figure 41: Zoom on one commutation for the voltage in second bus (a), first bus (b) and current through the inductor (c)

These last figures reveal that except for the overshoot there is no ripple for the bus 1 voltage, even if the perfect voltage source is unplugged. Moreover, we have a better view on the time response of the system which can be rated as low and consistent with the simulation results. To conclude, we can say that our prototype has a fast response and the voltage in bus 1 is well controlled.
This is the end of the full analysis and design of a bidirectional DC/DC converter.

Figure 42: Picture of our prototype

Conclusion

The design of a reversible DC/DC converter demands great precision and has to be conducted step by step in order to avoid any mistake that could ruin the whole project. The first step was to understand how the converter operates. From an electric scheme it was possible thanks to a qualitative analysis to get the different waveforms that characterize this kind of converter. Then, according to the required specifications of the converter, we were able to calculate all its electrical and physical parameters.

Once this had been done, it was necessary to build the inductor and to choose the other components of the power stage that corresponded the best to the specifications of the circuit. In this part we had to face the problems of availability at the workshop and the problem of commercial values which are very frequent while engineers design a new prototype. Moreover, to prevent unexpected breaks we had to oversize some components. Indeed, designing is the result of a compromise between making the smallest prototype and making a prototype that has more chances to operate.

The following step was the design of the current and voltage control loops. To complete this step, it was necessary to study the dynamic of the converter and to deduce the main transfer function of each control loop. A final simulation with PSIM software allowed us to validate all the theoretical study and to start the construction of the prototype.

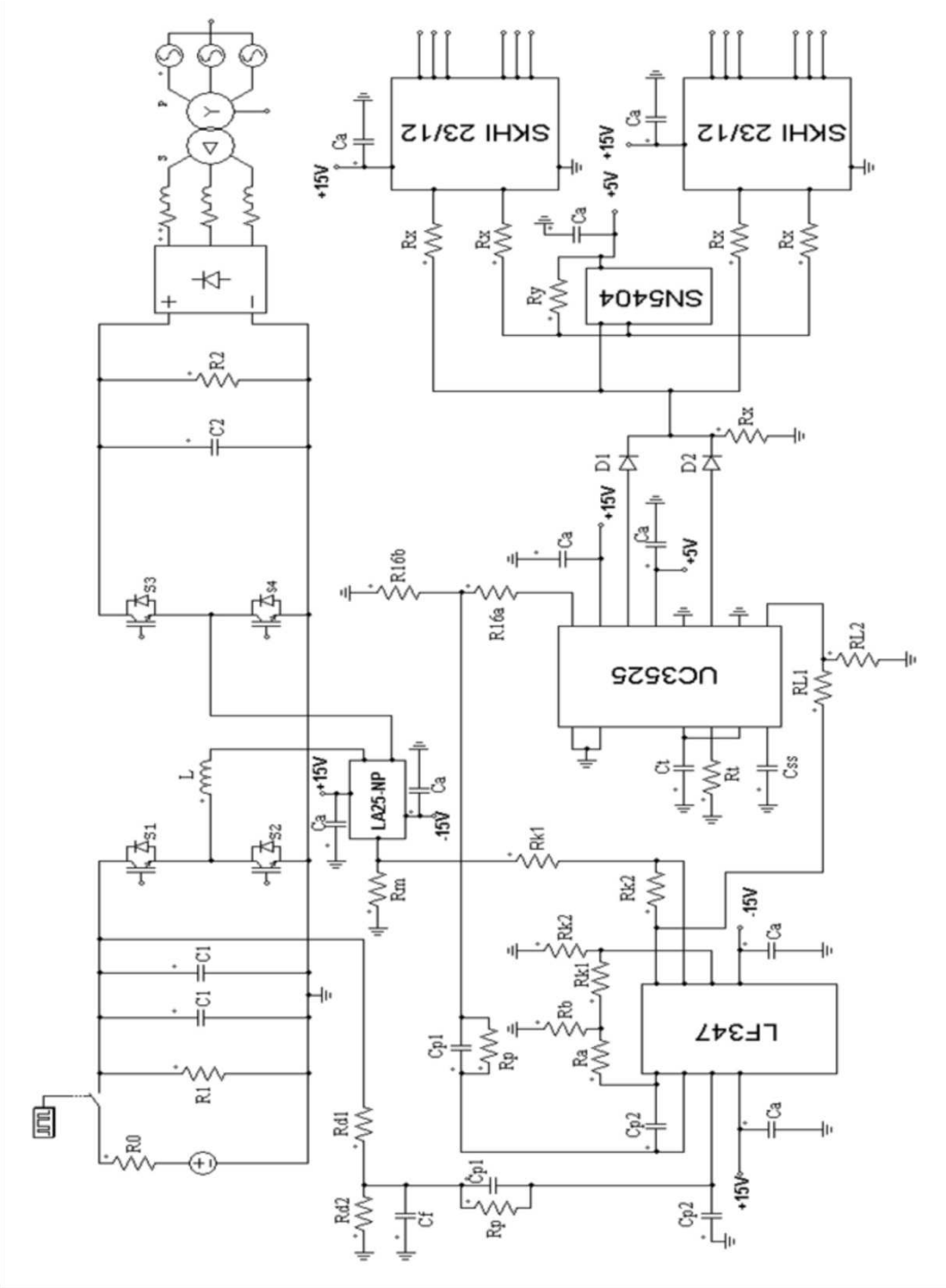
Then, we had to face the problem of all the differences between simulation and reality. All the sequence of tests, especially on the low power circuit, revealed that we had to make some adjustments to obtain the right signal. For example, the theoretical calculation on frequency was not very accurate and we had to add a low filter in voltage control loop because there was too much noise.

Finally all the tests on power stage in each state of control (open and close loop) revealed that practical results are really close to theoretical results, so that it confirmed that simulation is a very powerful tool while designing power electronics circuits. The only problem we faced at this stage was the “soft start” of the converter in close loop, it was necessary to pay attention to a possible over current in the circuit. Once this problem was solved, the final test was conducted and gave us full satisfaction.

To conclude, this project was a good way to understand all the difficulties that engineers face when they design a complex product. Besides, we learned how to work with new simulation and calculation software. Moreover, beyond all the theoretical aspects of a design, we also learned more practical aspects such as solving problems in test phase. One of the best proof of this success is that our prototype operates well. To complete this study, since this kind of converter has a great technological interest, we could have tried to technically and economically study a whole renewable energy system and insert our own designed converter in it.

Appendix

Appendix A: General scheme of the converter given to the technicians



Appendix B: Table of values given to the technicians

Name	Value	Quantity	Association for commercial values
R0	4Ω	1	/
R1	20 Ω	1	/
R2	45 Ω	1	/
Ra	1k Ω	1	/
Rb	500 Ω	1	/
Rp	55,55k Ω	2	33k Ω + 22k Ω + 470 Ω (series)
Rd1	19,8k Ω	1	18k Ω + 1,8k Ω (series)
Rd2	200 Ω	1	100 Ω + 100 Ω (series)
Rk1	10k Ω	2	/
Rk2	130k Ω	2	120k Ω + 10k Ω (series)
R16a	300 Ω	1	100 Ω + 100 Ω + 100 Ω (series)
R16b	200 Ω	1	100 Ω + 100 Ω (series)
Rx	1k Ω	5	/
Ry	1,2k Ω	1	/
Rt	11k Ω	1	/
RL1	2,75k Ω	1	2,7k Ω + 47 Ω (series)
RL2	1k Ω	1	/
Rm	200 Ω	1	100 Ω + 100 Ω (series)
C1	1,5mF	2	/
C2	1mF	1	/
Cp1	110nF	2	100nF + 10nF (parallel)
Cp2	220pF	2	/
Ca	1µF	9	/
Css	10nF	1	/
Ct	3,3nF	1	/

Bibliography

Classical references

[1] BARBI, Ivo & MARTINS, Denizar Cruz. Eletrônica de Potência: Conversores CC-CC básicos não isolados. 3rd ed rev. Florianopolis : Edição dos Autores, 2008. 377p.

[2] BARBI, Ivo. Eletrônica de Potência: Projetos de fontes chaveadas. 2nd ed. Florianopolis : Edição do Autor, 2007. 334p.

[3] MASSELOT Ch. & GIRARD M. Electronique non-linéaire tome 1. Edition Masson et Cie, 1975. 160p. ISBN 2-225-41-162-X

Web sites

[4] Thornton Eletronica Ltda [on line]. Ferrite core datasheets. Required software: Adobe Acrobat Reader.
Available on web: http://www.thornton.com.br/produtos/nee_ing.htm

[5] HS Beneficiamento de Alumínio Ltda [on line]. Calculation of heat sink thermo resistance
Available on web: http://www.hsdissipadores.com.br/calculo.asp

[6] Regulating pulse with modulator datasheets. Required software: Adobe Acrobat Reader.
Available on web: http://www.alldatasheet.com/datasheet-pdf/pdf/29335/TI/UC3525.html

[7] Texas Instrument [on line]. Signal inverter datasheets. Required software: Adobe Acrobat Reader.
Available on web: http://focus.ti.com/lit/ds/symlink/sn5404.pdf

[8] Fairchild Semiconductor [on line]. Operational amplifiers datasheets. Required software: Adobe Acrobat Reader.
Available on web: http://www.datasheetcatalog.org/datasheet/fairchild/LF347.pdf

[9] LEM Ltda [on line]. Current sensor datasheets. Required software: Adobe Acrobat Reader.
Available on web: http://www.datasheetcatalog.org/datasheet/lem/LA25-NP.pdf

[10] Semikron Ltda [on line]. Drivers datasheets. Required software: Adobe Acrobat Reader.
Available on web: http://www.semikron.com/internet/webcms/online/pdf/SKHI_23_12.pdf

[11] Semikron Ltda [on line]. IGBTs datasheets. Required software: Adobe Acrobat Reader.
Available on web: http://www.semikron.com/internet/ds.jsp?file=17.html