MARINE
NATIONALE

Ecole Navale
Et
Groupe des Ecoles du Poulmic

PROJET DE FIN D'ETUDES
GENIE ENERGETIQUE.

ANALYSIS AND DESIGN OF A FORWARD CONVERTER.

ECOLE NAVALE

Promotion 2006

EV2 Arboy
EV2 Cousin

UFSC

Universidade Federal de Santa Catarina. Instituto de Eletrônica de Potência

INEP

Acknowledgment

We would like to thank Professor Ivo Barbi for his help and his patience during the entire Project. We would like also to thank the technicians who built our full circuit especially Mr. Pacheco. We are also very grateful to Professor Marcelo for his help during the test phase of our project. Finally we thank Professor Marion who help us in the correction of this report.

Analysis and design of a Forward Converter.

Students : EV2. C. Arboy et B. Cousin, EN 2006

Type of report : Rapport de Projet de Fin d'Etude (PFE)

University : Federal University of Santa Catarina (UFSC)
Power Electronic Engineering Department (INEP)

Project chief : Ivo Barbi, Professor in Power Electronics Institute at the UFSC

ABSTRACT

Our project consists in the study, the design and the realization of a *Forward* converter. The design of a forward converter demands great precision when calculating the different parameters and restrictions that will have to be applied when conceiving the model.

The first step was the understanding of the forward converter in order to know the main parameters needed and the different mathematical equations for the choice of the different components of the forward. The use of the software PSIM completes this work for the comprehension,the collection of different values and for the checking of the circuit calculations.

Once this had been done it was possible to proceed to the construction and to the test the forward converter in the laboratory. These different tests allowed us to validate the performed design and simulations.

Then we have controlled the output voltage of the forward converter with a feedback control circuit in order to assure the optimal function of the forward and automatic control of the different parameters.

RESUME

Ce projet a pour but l'étude et la réalisation complète d'un convertisseur *Forward* s'inscrivant dans un cahier des charges bien précis afin d'être tester.

Un travail préliminaire portant sur l'étude qualitatives du convertisseur permet de dégager les nombreux paramètres qu'il sera nécessaire de surveiller ainsi que d'obtenir les différentes équations mathématiques utiles pour dimensionner les éléments constitutif du convertisseur.

La simulation par outil informatique vient compléter cette démarche amont et nous aide ainsi à accéder à des résultats qu'il convient de confronter une fois le prototype réaliser.

Ensuite le convertisseur une fois dimensionner, en ayant respecté au maximum le cahier des charges est construit puis testé. Ces différents tests nous permettent de valider notre convertisseur et les simulations effectuées.

Enfin l'intégration dans une chaine de contrôle permet d'asservir le convertisseur tout en assurant un fonctionnement optimal de ce dernier et le contrôle des différents paramètres.

Keywords : Buck converter, Forward converter, Transformer, Inductor, Capacitor.

Summary

SYMBOLS TABLE 1
INTRODUCTION 3
I Power electronic DC/DC converter 4
I-1 Buck converter. 4
I-1-a Commutation cell 4
I-1-b The output load 6
I-1-c Fundamentals relations 7
I-2 Advantages of an isolated Buck 8
I-3 Forward converter 9
I-3-a From the Buck to the Forward converter 9
I-3-b Explanation of the different waves forms 10
II Design of a Forward converter 13
II-1 specific problem 13
II-2 Forward Transformer design. 14
II-2-a design of the core 15
II-2-b Number of wires turn 16
II-2-c Wires diameter 17
II-2-d Measure of the transformer's losses 18
II-2-e Heat calculation 19
II-3 Output Inductor Design 21
II-3-a Determination of the inductance's value 21
II-3-b Determination of the inductor core 22
II-3-c Determination of the inductor's wire and air gap 22
II-4 Choice of the INEP components. 23
II-4-a Output Capacitor Design 24
II-4-b Determination of the switch 26
II-4-c Determination of the heat sink for the switch 26
II-4-d Clamping Circuit Design 28
II-4-e Choice of the diodes 30
II-4-f Diode thermal calculation 31
III Auxiliary Power Supply (Gate signal circuit) 33
III-1 Driver and integrated circuit 33
III-2 Driver design. 34
III-2-a Design of driver transformer core 35
III-2-b Number of wires turn 35
III-2-c Wires diameter 35
III-2-d Measure of the driver transformer's losses 35
III-2-e Heat calculation 36
III-3 Determination of the driver switch 36
III-4 Driver circuit protection Design 36
III-4-a switch gate power stage protection 36
III-4-b driver switch protection 37
III-4-c driver switch gate protection 37
III-4-d driver demagnetized diode 37
III-5 Integrated circuit. 38
IV Test of the laboratory prototype 41
IV-1 Integrated circuit test 41

IV-2 Driver circuit test 41
IV-3 Power stage test 42
V Control design and final test 43
V-1 Pulse with modulator (PWM) 44
V-2 Power stage transfer function 44
V-3 Corrector transfer function 46
CONCLUSION 48
APPENDIX 49
Appendix 1: Table of values from experiment of our forward 49
Bibliography 50
Classical Referencies 50
Web Sites 50

SYMBOLS TABLE

V_{in}	Input voltage	V
V_{out}	Output voltage	V
I_{in}	Input current	A
I_{out}	Output current	A
T	Switching period	s
t	Time	s
f	Switching frequency	s^{-1}
D	Duty Cycle	No dimension
I_X	Current through component x	A
$\overline{I_X}$	Average current in component x	A
I_{rmsX}	Efficient current in component x	A
U_X , V_X	Voltage across component x	V
T_1	Transistor conduction time	s
m	Transformation ratio of the transformer	No dimension
m_d	Transformation ratio between the primary winding and the demagnetize winding	No dimension
P_{out}	Output power	W
P_{in}	Input power	W
P_X	Power in component x	W
k_w	Winding factor between Primary windings surface and Secondary windings surface	No dimension
k_p	Winding factor in transformer due to isolation between different windings	No dimension
k	Inductor winding factor between primary winding surface and window surface	No dimension
$J_{\max}$	Maximum current density	$A.cm^{-2}$
ΔB	Flux density	T
$B_{\max}$	Maximum magnetic	T
A_w	Window surface or total windings surface over the core	cm^2
A_P	windings surface over the core	cm^2
A_S	Secondary windings surface over the core	cm^2
A_e	Useful windings surface over the core or central surface of the core	cm^2
N_X	Number of turn of the component x	No dimension
g , lg	Air gap	mm
V_e	Volume of the core	cm^3
P_C	Magnetic power losses	W
P_{C1}	Magnetic power losses volume	$W.cm^{-3}$
$L_{Leakage}$	Leakage inductance	H
M	Magnetizing inductance	H
R_X	Thermal resistance for component x	Ω.cm

T_a	Ambient temperature	°C
T_j	Junction temperature	°C
μ_0	Vacuum permeability	SI
T_X	Temperature in component x	°C
ΔI_X	Current peak to peak in component x	A
ΔV_X	Voltage peak to peak of component x	V
R	Resistance	Ω
C	Capacitance	F
L	Inductance	H
s	Laplace function	No dimension
G_{dB}	Decibel gain	dB

INTRODUCTION

Power electronics has increased a lot over the last few decades and there was much transformation in this discipline. This evolution was possible thanks to the development of better and reliable switches in terms of voltage blocking capacities, current capacities, losses and switching speed. One of the major applications of power electronics is the dc-dc conversion. We can distinguish two different types of applications: the first one is the use of a dc-dc convertor in order to supply a direct source knowing that we already have an input direct source. For example the supply of a system from accumulators. Second one is the use of a dc-dc converter in order to supply a direct source knowing that the primary alimentation is an alternating current supply.

Our project aims to design a dc-dc converter, in order to be able to feed a domestic tool such as a personal computer, from the electrical distribution network. The converter has to provide a power of 100 W for an output rated voltage of 20 V using an input dc voltage of 300 V generated by an ac-dc converter.

First the general structure of two different DC/DC converters will be studied: the Buck and the Forward. Then we will go through all the steps to design a Forward converter as a manufacturer process. Then we will test it to verify the results with the design/simulation. Finally we will design and insert a control loop that regulates the output voltage of the forward converter in order to assure the optimal function of the different parameters.

I Power electronics dc-dc converter

I-1 Buck converter.

The Buck converter is a unidirectional converter. It means that current and voltage can't flow the converter with a negative value. Thus the energy flux can be provided in only one way in the converter.

The aim of such converter is to allow the energy transfer between a direct voltage source and a direct current source. Thus average voltage $\overline{U_{out}}$ needed to be fixed at the entrance of I_{out} source that respected criterion: $0 \le \overline{U_{out}} \le U_{in}$ and $\overline{U_{out}}$ can be settled between these two values.

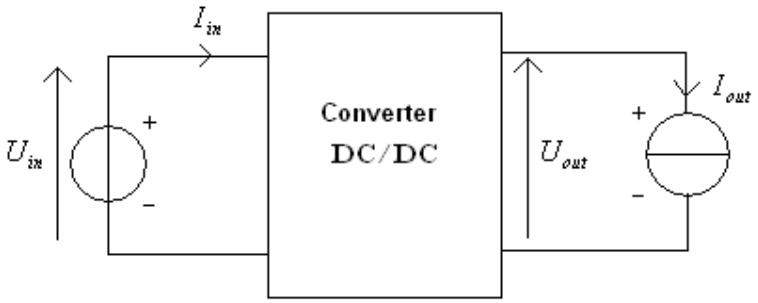

Figure 1: Buck converter.

I-1-a Commutation cell

The structure of the buck converter includes only one commutation cell as shown in the figure below.

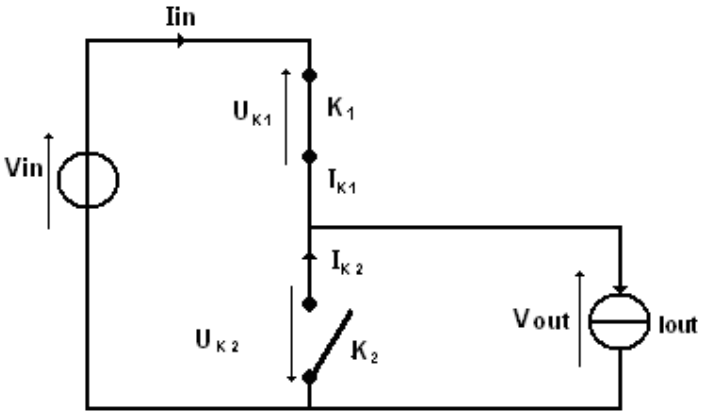

Figure 2: structure of the buck converter

Through the mechanisms of conduction and blocking of the two switches, two states are possible.

If K_1 is conducting and K_2 blocking: $V_{out} = V_{in}$ with $U_{K2} = -V_{in}$

$I_{out} = I_{in}$ with $I_{K1} = I_{out}$

If K_1 is blocking and K_2 conducting: $V_{out} = 0$ with $U_{K1} = V_{in}$

$I_{in} = 0$ with $I_{K2} = I_{out}$

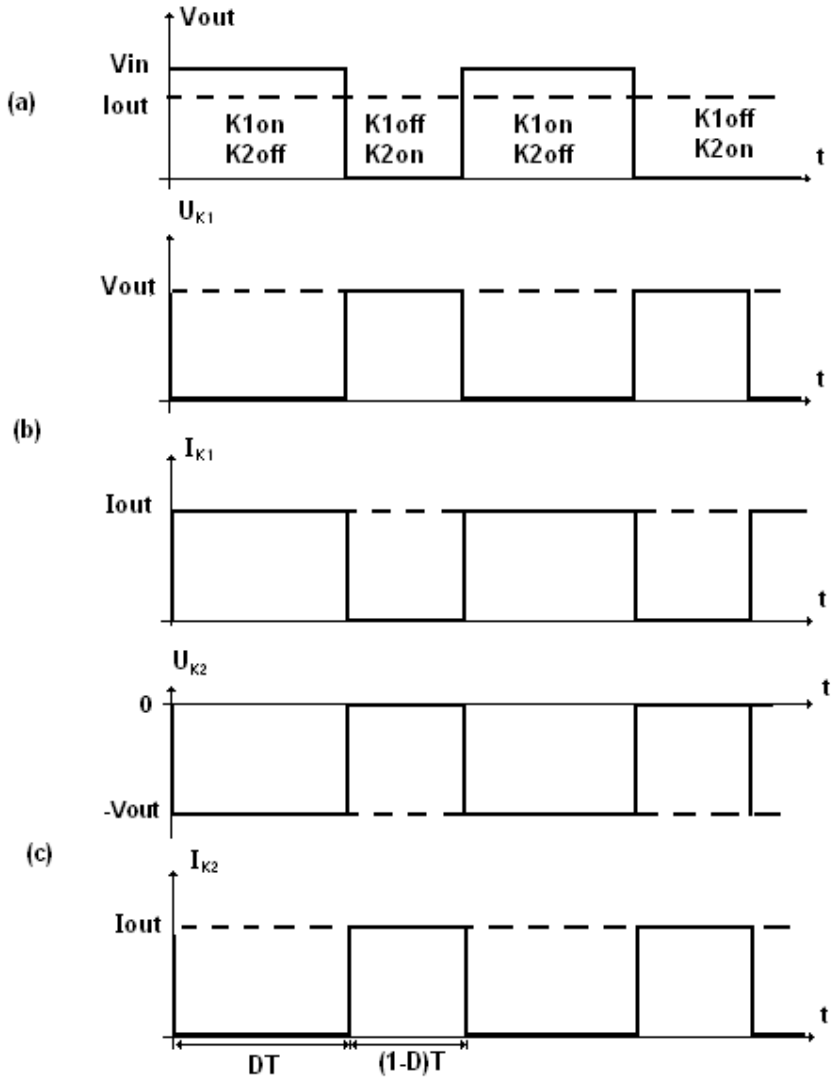

Figure 3: Typical electric values: (a) output value; (b) switch K1; (c) Switch K2.

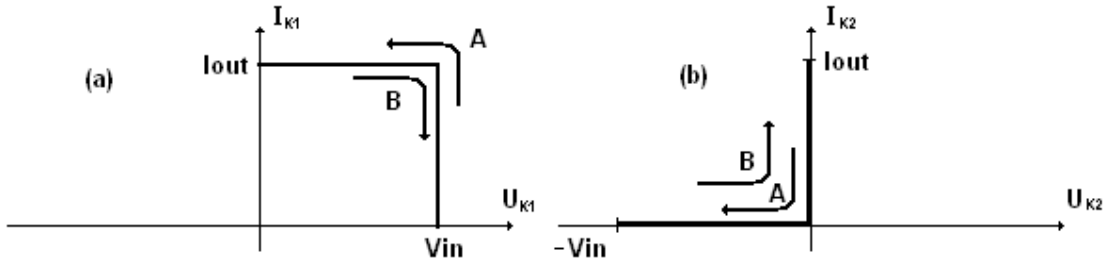

Figure 4: Static characteristic: (a) Switch K1; (b) Switch K2.

Current and voltage sources can't be reversed in this circuit. Thus, it shows that switches work in two segment for their own static characteristics (figure 4).

The first switch K1: has applied to it a positive voltage and has to conduct positive current. Besides a command commutation is needed. So the first switch is a transistor type.

The second switch K2: has to withstand a reverse voltage and has to conduct a positive current. The commutation happens spontaneously thanks to the global state of the circuit. So the second switch is a diode type.

Now we will represent the transistor by an IGBT (T) in the next figure.

I-1-b The output load

In order to be able to define and to give the fundamental relations for a Buck converter, the current source needs to be specified.

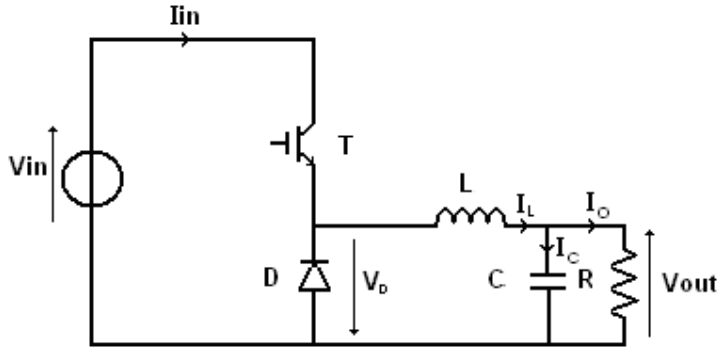

Figure 5: Buck converter and his charge.

This diagram which represents a Buck converter has a circuit with paralleled capacitor and resistor, both connected in series with an inductor. Thus, it provides to the output a source with current nature. This type of output load is standard in a Buck converter.

I-1-c Fundamental relations

According to switches states, output voltage (V_{out}) can have the same value as input voltage (V_{in}) or can reach zero. Output voltage is composed of voltage pulses. Thus output voltage is not a perfect direct voltage. The output inductor and capacitor createa low-pass filter. The cutoff frequency of this filter must be smaller than the switching frequency. Then the average value for the output voltage can be observed at the load resistor. Thus output voltage is lower than the input voltage. The following relation links the average output voltage to the duty cycle and input voltage.

$$V_{out} = \frac{1}{T}\int_0^T V(t)dt = \frac{1}{T}\int_0^{DT} V_{in}dt = \frac{1}{T}(DTV_{in} - 0 \times V_{in})$$

Thus, $\boxed{V_{out} = V_{in} \times D}$ (1)

D is the duty cycle which is defined by the ratio between the conduction time of the transistor (t_1) over the switching period (T).

$$D = \frac{t_1}{T} \text{ with } 0 \le D \le 1$$

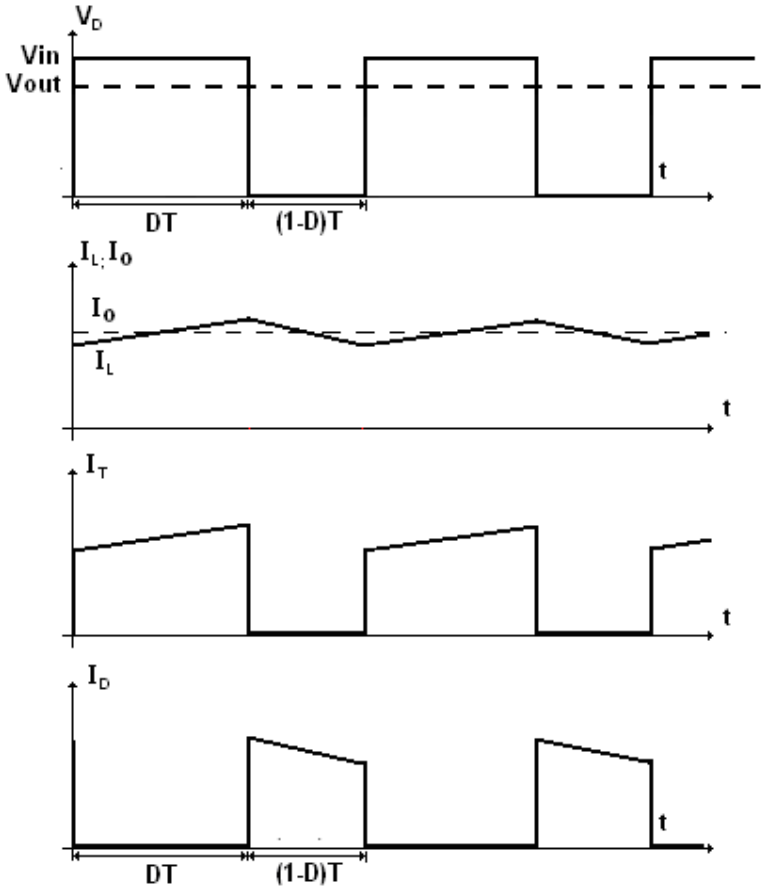

Figure 6: Waves forms type of a Buck converter

Action on conduction time of the transistor allows us to control the dc output voltage. This control happens over a wide span of values. Nevertheless $V_{out} = V_{in} \times D$ is correct, only if the current that flows through the inductor is never null. The inductor provides a current with AC and DC components. The aim of the capacitor is to absorb the AC component of the current, so that the DC component may flow directly through the resistor. Thus we will have an ac-free average output direct voltage. Still, the capacitor is not able to completelyabsorb the AC component that is why there are small parts of AC current that also flow through the resistor.

I-2 Advantages of an isolated Buck

One of the major applications of power electronics is the dc-dc conversion. This type of converter is used in electric appliances such as battery chargers. In order to improve the Buck converter we can insert a transformer. There are 3 main advantages with this transformer.

- In order to prevent a possible electric shock, an option is to isolate the output from the input by using a transformer (see figure 7).

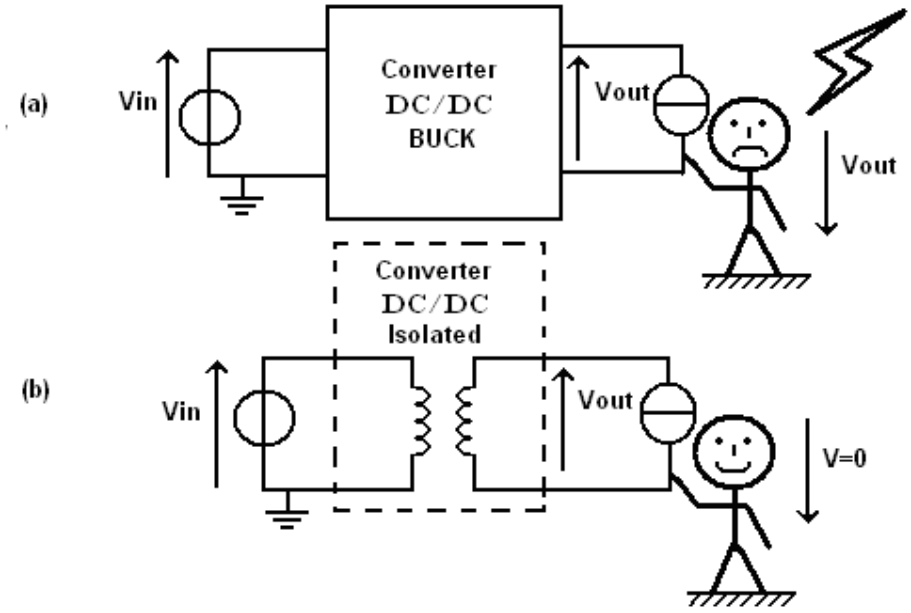

Figure 7: (a) The Buck converter is not isolated from the input;
(b) The converter is isolated, Vout is a floating value: there is no risk of electrocution.

- In a Buck if we have an important difference between the input and the output for example $V_{in} = 300V$ and $V_{out} = 20V$ the duty cycle is $\frac{V_{out}}{V_{in}} = 0.067$. It is very difficult to generate such a small duty cycle. Thanks to the transformer as we will see in the second part it is possible to increase this duty cycle in order to work with such a large voltage difference.

- The power applied to the switch in an isolated buck will be lower than in the Buck as is shown in figure 8.

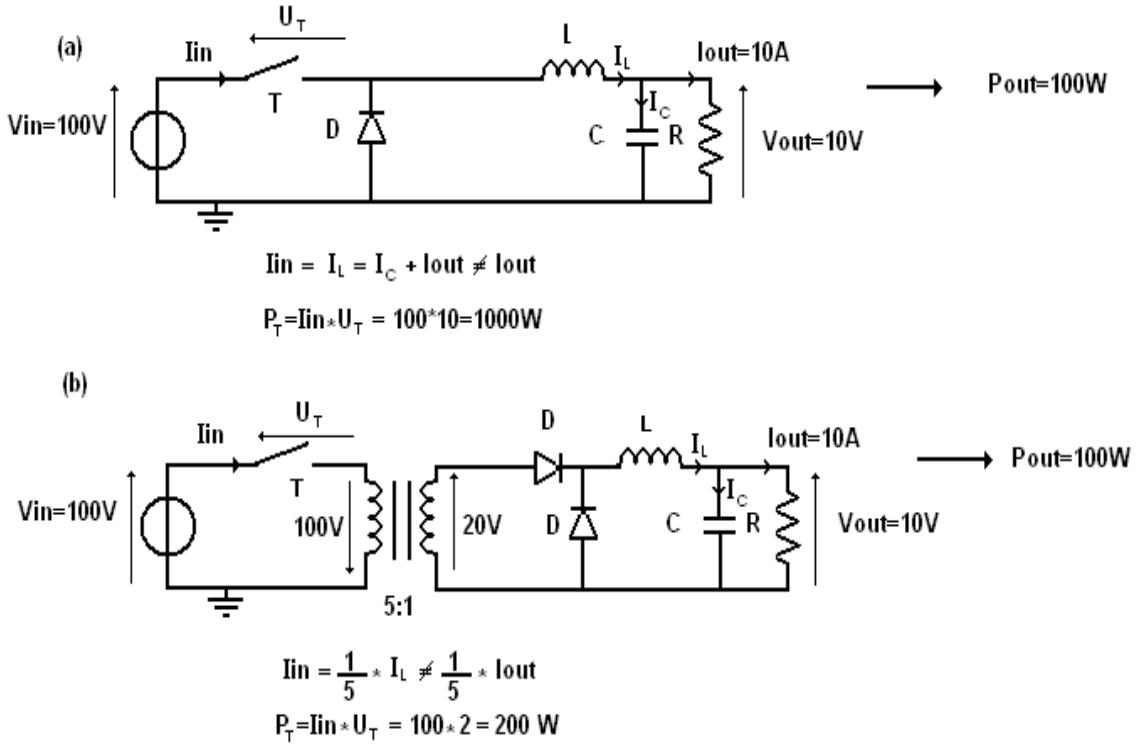

Figure 8: Difference of power applied to the switch (T) between a Buck (a) and an isolated Buck (b) for the same enter and exit value.

I-3 Forward converter

I-3-a From the Buck to the Forward converter

In the Forward converter (figure 9) the primary of the transformer is inserted in series with the transistor T. The secondary is connected to the output LC filter, where the diode D_2 plays the same role as the free-wheeling diode D in the buck converter. A second diode D_1 is inserted in order to prevent a negative current in the secondary of the transformer.

The particularity of the transformer in the Forward converter is that it has a third winding. It is supplied or not depending on if the diode D_m is opened or not. This third winding is needed because of the nature of the source applied at the primary of the transformer. Actually, without this third winding, the voltage $U_1 = V_{in}$ when the transistor T is conducting, then the voltage $U_1 = U_2 = 0$ when D_2 is conducting during the free-wheeling period.

(a)

(b)

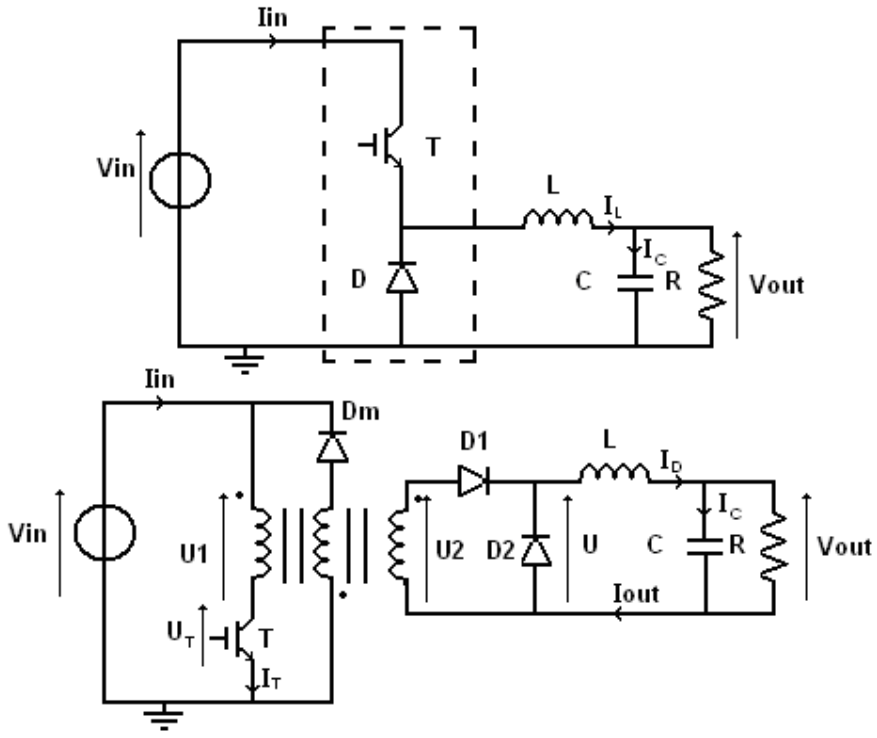

Figure 9: From the buck converter (a) to the forward converter (b).

So, the average voltage applied to the transformer is different from zero. The magnetic current then excessively increases its value until the saturation of the magnetic core. The purpose of the third winding is to assure the function of the complete demagnetisation of the transformer at the end of each commutation period of the convertor.

I-3-b Explanation of the different waveforms

The voltage value U_1 (figure 10) in the primary of the transformer is V_{in} when the transistor T is conducting. Then, the voltage U_2 in the secondary of the transformer is the same but affected by the turns ratio *m* of the transformer: $U_2 = mU_1 = mV_{in}$. As for the buck, the voltage U_2 of the forward converter must always be higher than the voltage V_{out}. We notice that the current I_2 in the secondary of the transformer is positive and increasing also in the inductance L. The current I_1 in the primary of the transformer is the sum of the current mI_2 (the current I_2 refers to primary) and a component of the magnetizing current of the transformer.

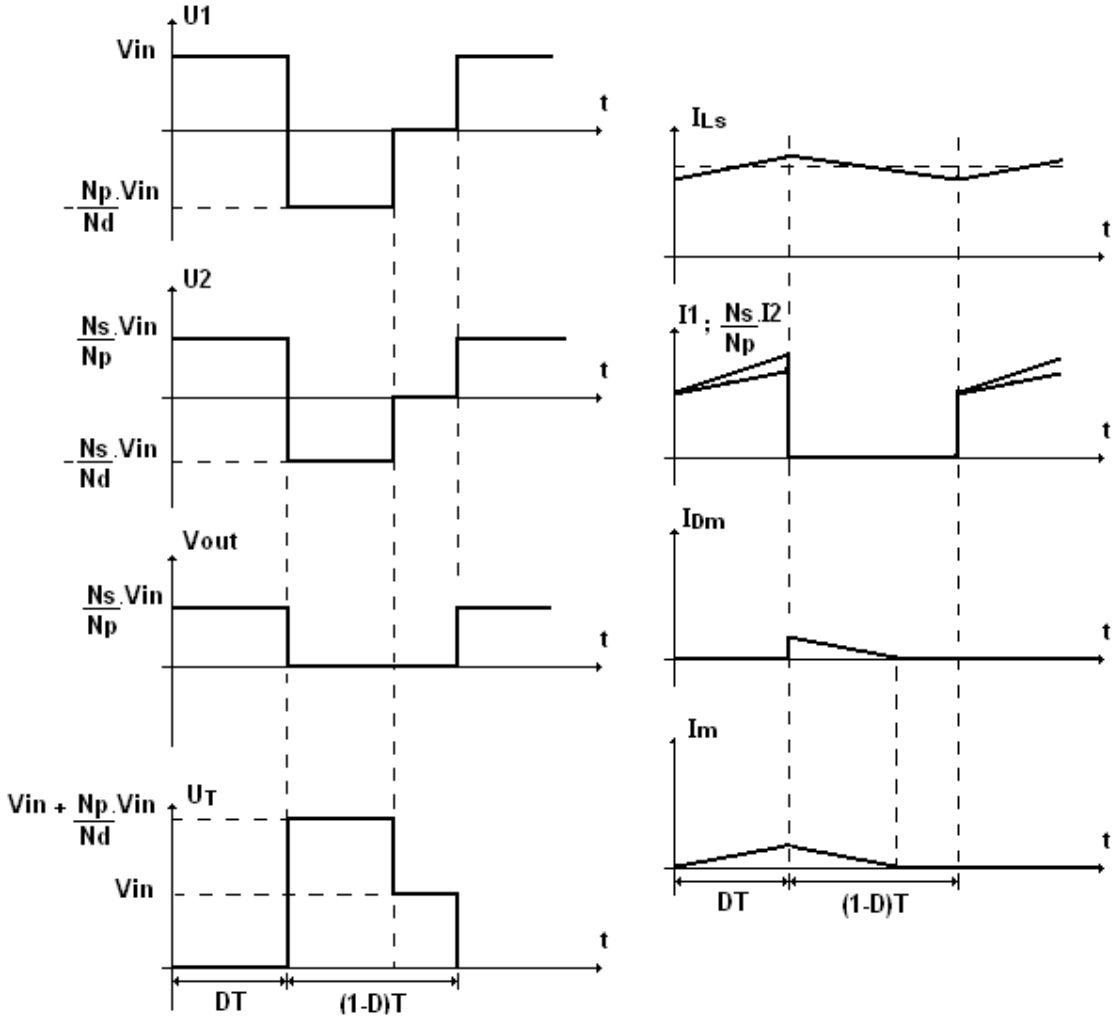

Figure 10: Waves forms type of a Forward converter

When the transistor T is blocked, the current cannot circulate in the primary of the transformer. In order to allow the continuity of the magnetic flux in the core of the transformer, the diode D_m is forward biased and conducts. The voltage of the third winding is then $-V_{in}$ which makes the magnetic current to decrease. During this phase, the voltages U_1 and U_2 become negative because of the transformer effect. The diode D_1 forbids the inversion of the current in the secondary of the transformer and must withstand the voltage $\boxed{V_{in} + mdV_{in}}$ (2) with $md = \frac{N_p}{N_d}$ the transformation ratio between the primary winding and the demagnetize winding. When the magnetize current is null then the diode D_m is blocked and the voltage U_1 and U_2 become null. We will notice that this phase must be finished before the end of the next commutation of the transistor; or else, as explained before, the magnetic current excessive increases until the saturation of the magnetic core.

During this latest phase (T blocked), which corresponds to the free-wheeling phase in the buck converter, the diode D_2 is conducting, the voltage V_{out} is null and the current in the inductance L_S is decreasing.

The voltage V_{out} creates in the forward converter is then $\boxed{V_{out} = mDV_{in}}$ (3) with D the duty cycle and *m* the transformer ratio between the primary and the secondary. m is fixed and D variable between 0 and 1. But in fact its value must be limited under 1 because of the demagnetisation stage.

In order to assure the complete demagnetisation of the transformer the surface under the curve during the time $[0, DT]$ of U_1 must be as large as the surface under the curve during the time $[DT, (1-D)T]$ (figure 11).

So :

$$D_{\max} TV_{in} = (1 - D_{\max})TV_{in} \frac{N_p}{N_d}$$

$$D_{\max} = (1 - D_{\max}) \frac{N_p}{N_d}$$

$$D_{\max} (\frac{N_p}{N_d} + 1) = \frac{N_p}{N_d}$$

$$D_{\max} = \frac{m_d}{1 + m_d}$$

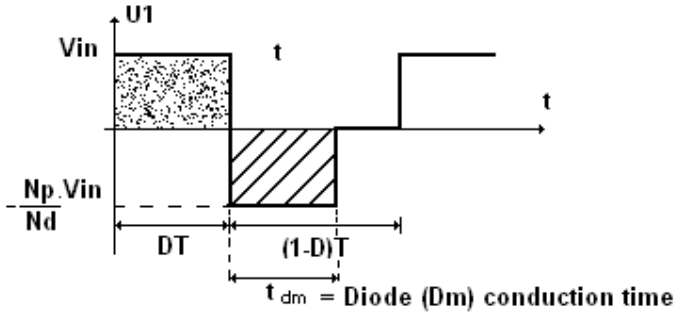

Figure 11: Surfaces to be equalized in order to assure the complete demagnetisation of the magnetic core.

II Design of a Forward converter

In order to conduct this study all the main equations used in the forward's design part are taken from the book *Projetos de fontes chaveadas* by Professor Ivo Barbi (Reference [1]). We also used PSIM simulation software for power electronics in order to simulate the forward converter and to get the main electrical parameters.

II-1 specific problem

The aim of this project is to design a forward converter in a special application. The design will help us to understand the difference between results given by simulation and results obtained through real measurement. Especially for the efficiency that will be the most important parameter to measure. Thus, we will study a forward converter that could have been used in laptop computer isolated dc supply. We will adopt a design process close from manufacturers factories. Values used through this project are close values used in computer engineering. We consider that the input supply will be provided by a French standard three-phase distribution grid: $380V / 220V / 50Hz$. The general diagram of this project is represented as it follows.

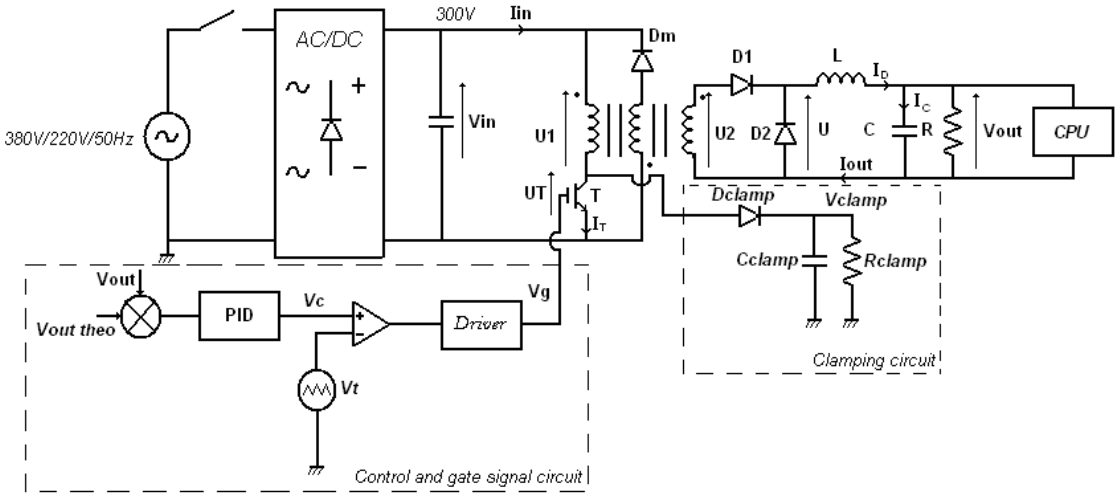

Figure 12: General circuit of the project.

Nevertheless we do not study and design directly the full circuit. It is needed to split it up into different parts. The ac-dc fronte-end is not considered here. Thus, in this part the study will be conducted in the order that follows:

- ✓ Forward Transformer design and test.
- ✓ Output inductor design and test.
- ✓ Output capacitor design.
- ✓ Switch choice.
- ✓ Clamping circuit design.
- ✓ Diodes choice.

Besides, before starting the study we need to provide the specifications that will be used to design the circuit:

$V_{out} = 20V$	$P_{in} = 125W$	$I_{in} = 0.417A$	$D_{\max} = 0.45$	$k = 0.7$
$I_{out} = 5A$	$V_{in} = 300V$	$\eta = 0.8$	$k_w = 0.4$	$J_{\max} = 450A/cm^2$ $B_{\max} = 0.3T$
$P_{out} = 100W$	$V_{in\min} = 240V$	$f = 50kHz$	$k_p = 0.5$	$\Delta B = 0.3T$

$P_{in} = \frac{P_{out}}{\eta}$, $I_{in} = \frac{P_{in}}{V_{in}}$ and $V_{in\min} = 300V - 20\%$

II-2 Forward Transformer design.

In a Forward converter the Transformer is the heart of the circuit. Indeed as it was said in the first part, not only isolation is provided by Transformer but also power reduction is applied to the switch. The frequency and the power used in the study are small; that is why we do not consider losses in the transformer during the first phase. Besides in order to see if the transformer is well designed we will make a thermal calculation of the transformer. We will calculate the maximum temperature rise in the transformer and compare it with allowable component temperature.

First of all we need to define the core that will be used to build the transformer.

So we need to define the following parameters:

A_w : Window area or total area occupied by the windings inside the core. (figure13)

A_P : Primary windings area inside the core.

A_S : Secondary windings area inside the core.

A_e : Effective windings area inside the core or central area of the core. (figure 13)

k_P : Winding factor between Primary windings area and Secondary windings area. $k_P = \frac{A_S}{A_P}$

k_w : Winding factor in transformer due to isolation between different windings. $k_w = \frac{A_P}{A_w k_P}$

Primary windings surface over the core is half the total surface of the core.

Thus $A_P = A_S$

$$N_P I_P = A_P J = k_w k_p A_w J \quad \text{with } J \text{ the current density.}$$

$$N_P = \frac{k_w k_p A_w J}{I_P} \quad \text{and} \quad I_{in} = I_s = \frac{P_{in}}{V_{in}} = \frac{P_{out}}{\eta V_{in}} = DI_p$$

$I_P = \frac{P_{out}}{\eta V_{in} D}$ with I_s the current across the switch generated by the gate signal, linked to the duty cycle.

Generally, manufacturers consider a current increase of 20% due to the magnetizing current.

$$\text{Thus } \boxed{I_P = \frac{1.2P_{out}}{\eta V_{in} D}} \quad (4)$$

II-2-a Core dimensioning

We decided to design the transformer for his limit application. That is why it will be designed for the maximum duty cycle, the minimum input voltage and the maximum current density.

$$N_P = \frac{k_w k_p A_w J_{\max} V_{in\min} \eta D_{\max}}{1.2P_{out}} \quad \text{thus } A_w = \frac{N_P 1.2P_{out}}{k_w k_p J_{\max} V_{in\min} \eta D_{\max}}$$

According to the Faraday´s law:

$$Edt = Nd\phi$$

$V_{in} T_1 = N_p \Delta B A_e$ with T_1 the switch conduction time.

$$A_e = \frac{V_{in\min} T_{1\max}}{N_p \Delta B}$$

$T_{1\max} = D_{\max} T = \frac{D_{\max}}{f}$ with T the complete switching period.

$$\text{Thus } A_e = \frac{V_{in\min} D_{\max}}{N_p \Delta B f} \quad (5)$$

So we have the design ratio that will give us the core that we need to build the transformer.

$$\boxed{A_e A_w = \frac{1.2P_{out}}{k_w k_p J_{\max} f \Delta B \eta} \times 10^4} \quad (6) \text{ thus } \boxed{A_e A_w = 1.1 cm^4}$$

We refer this value in a core table. No value corresponds directly to this one. We decide to oversize the transformer core thus it will prevent a too high temperature rise. The present design assumes that natural convection will cool the transformer.

We chose $A_e A_w = 2.84 cm^4$. This value matches with the **E-42/15** type core (cf. volume of components appendix 1). It's a core made by a São Paulo factory. Besides the table also gives us also $A_e = 1.81 cm^2$

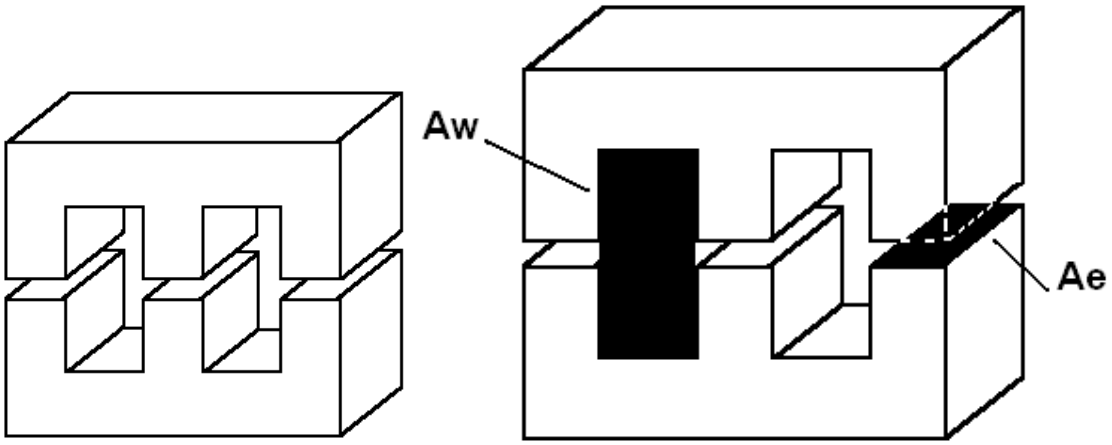

Figure 13: Core Geometry of the transformer generally used.

II-2-b Number of turns

We need to determine the number of turns of the single-phase three windings Forward transformer, according to (5).

$$\boxed{N_P = \frac{V_{in\min} D_{\max}}{A_e \Delta B f}} \quad (7)$$

$\boxed{N_P = 39.8}$ **45 turns** is adopted.

Indeed we have voluntarily overdesigned our transformer in choosing **E-42/15** type core. Thus, it allows us to choose a larger turns number so as to reduce the flux density and consequently the magnetic losses in the transformer.($\Delta B = 0.265T$). Nevertheless, the magnetizing current increases.

Secondary turns number must be determined:

$V_{out} = U_1 D = (U_2 - V_F)D$ with V_F the voltage drop into the D_1 diode.

$$V_{out} = V_{in} D \frac{N_S}{N_P} - V_F D$$

$$V_{in} D \frac{N_S}{N_P} = V_{out} + V_F D$$

$$\frac{N_S}{N_P} = \frac{V_{out} + V_F D_{\max}}{V_{in\min} D_{\max}}$$

$\boxed{N_S = N_P \left(\frac{V_{out} + V_F D_{\max}}{V_{in\min} D_{\max}} \right)}$ (8) thus $\boxed{N_S = 9.4}$ **10 turns** is adopted.

Tertiary turns number can be determined.

If we want that the demagnetization was done during the time $T_2 = T_D$ when the duty cycle is maximum, the demagnetized diode time conduction must be $T_2 = (1 - D)T$.

Thus $V_{in}T_1N_P = V_{in}T_2N_d$

$$\frac{N_P}{N_d} = \frac{T_2}{T_1} = \frac{T}{T_1} - 1$$

$\frac{N_P}{N_d} = \frac{1}{D_{\max}} - 1$ thus $\boxed{N_d = \frac{N_p D_{\max}}{1 - D_{\max}}}$ (9) $\boxed{N_d = 36.8}$ **37 turns** is adopted.

According to (3) $V_{out} = mDV_{in}$ we can now calculate the optimal value of the duty cycle we will use in our forward converter in order to comply with the specified output parameters.

$$D = \frac{V_{out}}{mV_{in}}$$

So $D = 0.3$

When we simulate the circuit in *PSIM* with $D = 0.30$ we find $V_{out} = 19.7V$. Nevertheless we will choose $\boxed{D = 0.31}$ in order to be more precise because it gives us $V_{out} = 19.9V$ through the simulation so output power is more precisely met.

II-2-c Wires diameter

Now we need to calculate the Root Mean Square (RMS) currents in each winding in order to choose the proper wires diameter.

Secondary RMS current:

$$I_{rmsS} = \frac{I_{out}}{\sqrt{2}} \qquad I_{rmsS} = 3.5A$$

Primary RMS current:

According to (4) $I_P = \frac{1.2P_{out}}{\eta V_{in} D}$ $I_P = 1.4A$

So $I_{rmsP} = \frac{I_P}{\sqrt{2}}$ $I_{rmsP} = 0.98A$

Tertiary RMS current:

Usually manufacturer use the following ratio:

$$I_{rmsd} = \frac{I_{rmsP}}{10}$$

$$I_{rmsd} = 0.098$$

We need to use the American Wire Gauge (AWG) table (volume of components appendix 2) to determine for each winding the diameter of the wire. Nevertheless theses values do not directly match with the table.

AWG table gives: $\begin{cases} AWG_P = 23 \\ AWG_S = 18 \\ AWG_d = 33 \end{cases}$ Yet we have voluntarily oversized the wire diameter in order to reduce the skin effect.

Indeed the skin effect shows that 99% of AC current is contained in the extreme part of the wire where the reactance χ is not so high. We can evaluate the portion of where the current is contained with $\Delta = \frac{7.5}{\sqrt{f}}$. Even if our frequency is not too large we need to pay attention to this phenomenon. Indeed, wire impedance $Z = R = \frac{\varphi \times l}{S}$ where φ is the material volume weight, l wire length and $S = f(\Delta)$ the surface that AC current use in the wire (which is function of Δ). Besides, Joule losses are given by: $P = RI^2$. So we understand that if the wire area effectively carrying the current increases, Joule effect is reduced. That is why we choose $AWG_P = 22$, $AWG_d = 18$ and $AWG_d = 28$. The other reason why we oversize our wire diameter is that it is difficult to work with a too small diameter on such a small core. It is a mechanical problem; manufacturers can have problems to construct the transformer.

II-2-d Measurement of the transformer's losses

We built the transformer and then started to test it. As is said at the beginning we do not take care about losses in order to design first. Nevertheless, even if the losses in the power transformer are not too important for the design, we need to measure losses to know if the magnetizing current is not too high. In fact to do theses measurement in transformer we must put an air gap ($g = 0.1mm$) for two reasons: The first one is that it will prevent saturation. The second is that it will provide us with an accurate measurement of the magnetizing inductance. The value of the air gap is low in order not to have a too small magnetize inductance.

We measure the leakage inductance $L_{Leakage}$ with $L_{Leakage} = L_1 + \left(\frac{N_P}{N_S}\right)^2 L_2$ with

L_1 : Primary inductance.

$\left(\frac{N_P}{N_S}\right)^2 L_2$: Secondary inductance refers to the primary side.

First we measure L_1 by putting the secondary circuit in short circuit and then we measure L_2 by putting the primary circuit in short circuit. Finally we make the calculation of the leakage inductance. Experimental measurements give us $L_{Leakage} = 33\mu H$. Besides, tests also give magnetizing inductance M, we put the circuit in open circuit and measure $M + L_1$ at the

primary. But because $M \geq\geq L_l$ so we obtain $M = 1.9mH$. So we are able to calculate the magnetized current and the power losses in the leakage inductance.

$$V_{in}dt = MdI_m$$

$$\boxed{I_m = \frac{V_{in}T}{M} = \frac{V_{in}D_{\max}}{Mf}} \quad (10)$$

$\boxed{I_m = 1.4A}$ It is a small value as expected. Indeed, in a forward converter the demagnetizion current is small.

Thus, now we can measure the power stored in the leakage inductance when the switch is closed. In order to understand how the calculation is made we can describe the circuit through an equivalent circuit as is shown in the following diagram.

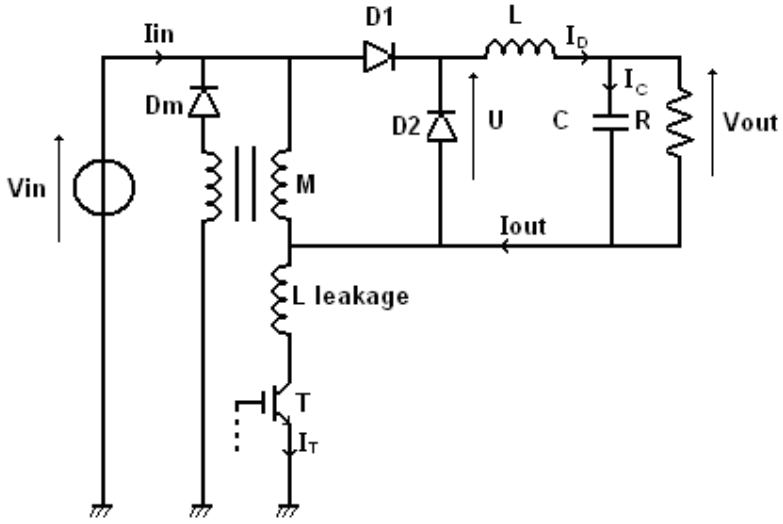

Figure 14: Equivalent circuit of the Forward converter when the transistor is blocking.

$$\boxed{P_{Leakage} = \frac{1}{2}L_{Leakage}\left[I_{out}\left(\frac{N_S}{N_P}\right) + I_m\right]^2 \times f} \quad (11)$$ (Secondary current is referred to primary side).

$$\boxed{P_{Leakage} = 5.2W}$$

This power is an approximation, since we simplified the circuit. Nevertheless, it is not too high.

II-2-e Thermal dimensioning

A thermal calculation of the transformer is needed. Thus it will tell us if the transformer is well designed. Indeed, if the maximum temperature that rises into the transformer is less than the maximum temperature authorized by the component it means that the design is successful.

To do the thermal-calculation of the transformer we will use simplified equations that are usually used by power electronic manufacturers.

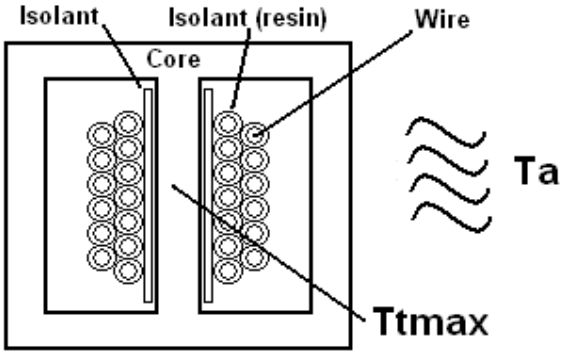

Figure 15: Repartition of temperature in the transformer.

First of all we need to calculate the volumetric magnetic power losses into the transformer.

$P_{C1} = \Delta B^{2.4}\left(K_h f + K_e f^2\right)$ with $\begin{vmatrix} K_h = 4.10^{-5} \\ K_e = 4.10^{-10} \end{vmatrix}$ which are experimental constants.

$$\text{Thus } P_{C1} = 0.124 W / cm^3$$

Yet we need to calculate all the magnetic losses into the central core that is why we measure his volume. V_e

$$V_e = 5.7\left(A_e A_w\right)^{0.68} \quad V_e = 8.7 cm^3$$

So the magnetic power losses are:

$$P_C = P_{C1} V_e \quad P_C = 1.1 W$$

Now we are going to calculate the primary winding losses:

$P_{WP} = N_p l_1 R_{PJ} {I_{rmsP}}^2$ with $l_1 = 4\sqrt{A_e} = 5.4 cm$ length of one winding around the central core and R_{PJ} the resistance per meter given by the table at $100^0 C$ $R_{PJ} = 0.000708 \Omega / cm$

$$P_{WP} = 0.17 W$$

Besides we do the same for the secondary:

$$P_{WS} = N_S l_2 R_{SJ} {I_{rmsS}}^2 \text{ with } l_2 = l_1 \text{ and } R_{SJ} = 0.000280 \Omega / cm$$

$$P_{WS} = 0.18 W$$

Thus the total losses into the transformer are:

$$P_{Transfolosses} = P_{WP} + P_{WS} + P_C$$

$$P_{Transfolosses} = 1.42W$$

We need to find the Thermal resistance of our core that we used to build the transformer.

$$R_T = \frac{23}{(A_e A_w)^{0.37}}$$

$$R_T = 18.3°C/W$$

Finally we know that the Thermal equivalent equation is:

$$\boxed{\Delta T = P_{Transfolosses} R_T} \quad (12)$$

We consider being in the worst situation it means that the ambient air is $T_a = 50°C$. Thus we can find the maximum temperature that can rise in our transformer:

$$T_{T\max} = T_a + P_{Transfolosses} R_T$$

$$\boxed{T_{T\max} = 76°C}$$

This temperature is very far from the maximum temperature allowed in, both, wires and magnetic core, which is $150°C$. So we can say that our transformer is well designed.

II-3 Output Inductor Design

The output Inductor is a very important component of the forward converter circuit. Indeed it filters the AC component and delivers the DC component of the current that will supply the load.

II-3-a Determination of the inductance's value

Thanks to the Kirshoff law, when the switch is conducting we have:

$$\Delta I_L = \frac{U_2 - V_{out}}{Lf} T_1$$

$$\Delta I_L = \frac{\left(\frac{N_S}{N_P} V_{in}\right) - \left(\frac{N_S}{N_P} D_{\max} V_{in}\right) - V_F}{Lf} D_{\max}$$

$$\boxed{L = \frac{\left[\left(\frac{N_S}{N_P}V_{in}\right)(1-D_{\max}) - V_F\right]D_{\max}}{\Delta I_L f}}$$ (13) with ΔI_L the current peak to peak, $\Delta I_L = 0.4 I_{out}$ is a simplified relation used by manufacturers. $\Delta I_L = 2A$

$$\boxed{L = 155\mu H}$$

II-3-b Determination of the inductor core

The inductor core must be determined and then the inductor number of turns. This method is actually the same as for transformer turn.

The expression of the flux gives us:

$\Phi = LI_{PK} = B_{\max} A_{eL} N$ with N inductor number of turns, A_{eL} useful inductor windings area over the core or inductor central surface of the core and I_{PK} the maximum current that goes through the inductor $I_{PK} = I_{out} + \frac{\Delta I_L}{2} = 6A$.

$$\boxed{N = \frac{LI_{PK}}{B_{\max} A_{eL}}}$$ (14)

Like for the transformer $NI_{PK} = J_{\max} k A_{wL}$ with k inductor winding factor between primary winding area and window area.

$$\text{Thus } \frac{LI_{PK}}{B_{\max} A_{eL}} = \frac{J_{\max} k A_{wL}}{I_{PK}}$$

$$\text{So } \boxed{A_{eL} A_{wL} = \frac{LI_{PK}^{\ 2}}{k B_{\max} J_{\max}}}$$ (15)

$\boxed{A_{eL} A_{wL} = 0.59 cm^4}$ This value matches with the **E-30/14** type core (volume of components appendix 1).

Thanks to tables $A_{eL} = 1.20 cm^2$

And according (14) $\boxed{N = 25.8}$ **26 turns** is adopted for inductor.

Now we need to calculate the RMS current in the winding in order to choose wire diameter.

II-3-c Determination of the inductor's wire and air gap

Inductor RMS current:

$$I_{PK} = I_{rmsL} = 6A$$

Thus, thanks to the wire table (volume of components appendix II) $AWG_L = 16$. We have chosen less than what the table gives us because in fact $I_{rmsL} \leq I_{PK}$

Finally the Air Gap ($\lg$) into the inductor is the last thing to design. Indeed Air Gap is the place where most parts of inductor energy is stored. Air gap is linked to inductance and reluctance by the equation that follow.

$$\boxed{\lg = \frac{N^2 \mu_0 A_{eL}}{L}} \quad (16) \quad \text{with } \mu_0 = 4\pi.10^{-7} usi \text{ and } \mathrm{Re}\, l = \frac{\lg}{\mu_0 A_{eL}} \text{ the reluctance.}$$

$$\lg = 0.65mm$$

Besides, we designed the output inductor and tested it in order to know if the design matches with what we built. First we need to measure the inductance. With the Air Gap value of $\lg = 0.6478mm$ we obtained $L = 127\mu H$.

Thus we notice that if we reduce the Air gap we will increase the inductance. After further manipulations we chose $\boxed{\lg = 0.4mm}$ and them we obtained $\boxed{L = 158\mu H}$ which corresponds to just 102% of the value of the inductance calculated.

II-4 Choice of the INEP components.

We will not build ourselves any components that we would select to conduct our project. For example diodes, switches, capacitors, resistors and integrated circuit. We will choose them from commercially available components in order to get the appropriate ones. Yet, in order to speed up the prototyping process, we have to choose components from the *INEP* workshop. Thus, some components will be oversized in order to match with standard manufacturer values. Besides it will save money to choose standard manufacturer components (since they are very cheap), rather than ordering accurate ones to manufacturer. Finally it will also give good result in simulation.

There are three fundamental parameters to choose diodes and switches:

- Switching frequency.
- Rated voltage.
- Average, RMS current and thermal calculation.

For a resistor we need to specify two fundamental parameters:

- Resistance.
- Power losses.

The current that flows through these components is responsible for losses and temperature rise in junction. Thus depending on the current value, thermal dimensioning may be needed. Finally for capacitor we need the capacitance value and the rated voltage.

Thanks to *PSIM* software, we can have access to RMS and average currents and voltage peaks. So, in all this part we will give value that will be obtained through simulation. Besides we will choose the most accurate components according to this simulation. Then simulate again to see if it matches with the expected results.

II-4-a Output Capacitor Design

The aim of the output capacitor is to absorb the AC current component in order to prevent it from flowing through the resistance. Thus the current that flows through the output load is only a DC current. Nevertheless the output capacitor can't divert the entire AC current component from the output inductor. That is why if we look very accurately to output current it still has some oscillations at the switching frequency.

The design of the output capacitor requires some specific values. Indeed we cannot build ourselves a capacitor which is too complicated. Thus we need the capacitor voltage V_C, the capacitor peak to peak ΔI_L current, but also the minimum capacitance C that is required for the circuit.

As soon as we know these three values $(V_C, \Delta I_L, C)$ we have to check into tables of a capacitor manufacturer. One of the most famous capacitors manufacturer is ***EPCOS.*** First of all, as in the output inductor design the current peak to peak adopted was $\Delta I_L = 2A$. Thus the same current peak to peak will be adopted for output capacitor design. According to the I_C waveform:

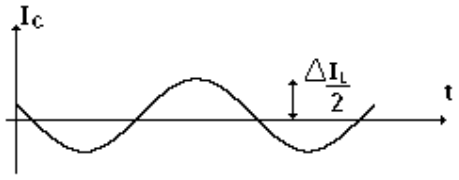

Figure 16: Waveform of the current in the capacitor.

$$I_C = \frac{\Delta I_L}{2}\sin(2\pi ft)$$

$$\frac{\Delta V_C}{2} = \frac{1}{C}\int I_C dt$$

$$\frac{\Delta V_C}{2} = \frac{\Delta I_L}{2C}\int \sin(2\pi ft)dt$$

$$\frac{\Delta V_C}{2} = \frac{\Delta I_L}{4\pi fC}\cos(2\pi ft) \text{ thus at the beginning for } t = 0$$

$C = \frac{\Delta I_L}{2\pi f \Delta V_C}$ besides usually to design capacitor usually manufacturer take $\Delta V_C = 0.01 V_{out}$

Thus we obtain. $\Delta V_C = 0.2V$ and $C = 32\mu F$

We consider that $V_C \cong V_{out}$ with a tolerance to 40% of load variation of the capacitor component.

$$\begin{cases} V_{C\max} = 28V \\ C_{\min} = 32\mu F \\ \Delta I_C = \Delta I_L = 2A \end{cases}$$

Before choosing the capacitor we need to consider the life time of our output capacitor component. Indeed in our study we decided to design a forward converter circuit for computer use. Thus the average life time of a laptop computer is around 10 years. To match with tables and diagram from <u>*EPCOS*</u> (volume of the component appendix 3 and 4) we will choose a life time of 11 years.

Besides we must specify in which ambient temperature the output capacitor will work. Like for the thermal-calculation of the transformer we will consider that the ambient air is at $50°C$ (the worst condition that can face the capacitor).

Thus by using diagram we find the ratio $\frac{\Delta I_L}{I_{AC,R}} = 2$ thus $I_{AC,R} = 1000mA$

($I_{AC,R}$ is the maximum current that flows through the capacitor for the maximum temperature authorized in the component $105°C$).

By using the table of capacitor from <u>*EPCOS*</u> for $V_C = 35V$ and for $I_{AC,R} = 1000mA$ we have to choose the component with $I_{AC,R} = 1260mA$ (nearest value). Thus it gives us the capacitance of output capacitor:

$$\boxed{C = 2200\mu F}$$

Yet we can't have such capacitor to conduct our project because it is too expensive. That is why we will choose in the workshop of the INEP department an output capacitor with

$$\boxed{\begin{array}{l} V_C = 35V \\ C = 220\mu F \\ \Delta I_L = 2A \end{array}}$$

So to respect the information that was given by tables we need to put **10 capacitors** that we chose from the INEP workshop in parallel ($n = \frac{2200}{220} = 10$).

II-4-b Determination of the switch

We need to know the theoretical value that can be applied on the switch. Maximum theoretical voltage applied across the switch is according to (2):

$$U_T = V_{in}\left(1+\frac{N_P}{N_d}\right)\ U_T = 667V\ .$$

So we consider using the **IRFBG20 Mosfet 1000 V/high frequency** (available in the INEP workshop).

Indeed we must choose a MOSFEETMOSFET with maximum voltage higher than the one given by calculation and simulation.

II-4-c Determination of the heat sink for the switch

The MOSFEETMOSFET will have to be cooled in order not to be destroyed. That is why we need to calculate the Joule losses in the MOSFEET:

$$\boxed{P_{Mos} = R_{DS} I_{rmsT}^{\ 2}} \quad (17)$$

with I_{rmsMos} the efficient current that flows through the MOSFEETMOSFET.

This value can be calculated with complicated mathematical equations. Nevertheless we prefer to use *PSIM* software. $I_{rmsT} = 0.92A$. Besides R_{DS} is the MOSFEETMOSFET on-resistance, its value depends on MOSFEETMOSFET's junction temperature. According to diagram (Volume of components appendix 5) this resistance can be determined for a specific junction temperature.

We choose to work in the worst situation that the MOSFEETMOSFET can bear. It means his junction temperature $T_j = 100°C$, this value is usually used by engineers because the MOSFEETMOSFET is still working normally at this temperature. Above this temperature the MOSFEETMOSFET performance gets worst and at 150 degrees it gets destroyed. Most of the time MOSFEETMOSFET junction temperature will be less than this value. Nevertheless, the chosen component needs to be placed in their temperature mechanical limits in order to have a good design. So, $R_{DS} = 1.8 * 11 \approx 20\Omega$. And thus we find:

$\boxed{P_{Mos} = 16.9W}$ of losses.

Now we have estimated the losses in the MOSFEETMOSFET. We need to make a thermal-calculation in order to know if the MOSFEETMOSFET will be able to keep is junction temperature under $T_j = 100°C$. Indeed, is the MOSFEETMOSFET able to evacuate power losses (Joule effect) without an external heat sink or not?

Like it was used for the transformer thermal calculation, according (12):

$$\Delta T = T_j - T_a = P_{Mos} R_{thMos}$$

with R_{thMos} MOSFEET MOSFET total thermal resistance from MOSFEETjunction to ambient, with ambient temperature $T_a = 50°C$.

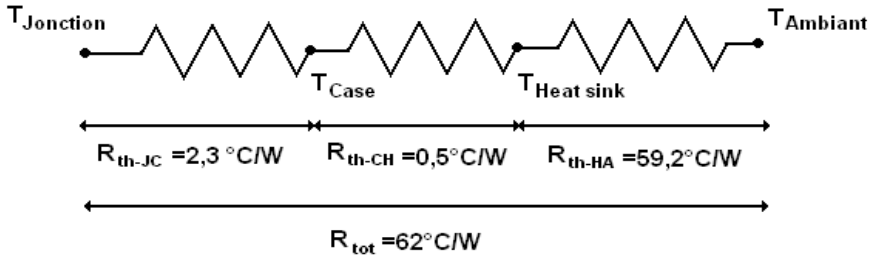

Figure 17: Equivalent circuit of the MOSFEETMOSFET's thermal resistance.

First we are going to calculate the junction temperature into the MOSFEETMOSFET without an external heat sink.

$$T_j = T_a + P_{Mos} R_{thMos}$$

with $R_{thMos} = 62°C/W$ according to diagram

Thus $T_j \approx 1100°C$

So we can see that this temperature is too high and the MOSFEETMOSFET would be destroyed. We understand that we must put an external heat sink in order to reduce MOSFEETMOSFET total thermal resistance. **HS 12643 Heat Sink.** This kind of external heat sink is chosen because it is the smallest one in the *INEP* workshop.

Thus, we choose: ambient air $T_a = 50°C$ and junction temperature $T_j = 100°C$. We need to determine the MOSFEETMOSFET total thermal resistance that matches with the junction temperature needed.

$$\Delta T = T_j - T_a = P_{Mos} R_{thMos} \text{ thus}$$
$$R_{thMos} = \frac{\Delta T}{P_{Mos}} = 2.96°C/W$$

So now we have MOSFEETMOSFET total thermal resistance. As it show in thermal equivalent diagram

$$R_{thMos} = R_{thMosjc} + R_{thMosch} + R_{thMosha}$$

We need to evaluate the external heat sink thermal resistance that we will choose.

$$R_{thMos} = R_{thMosjh} + R_{thMosha}$$

$$R_{thMosha} = R_{thMos} - R_{thMosjh}$$

$R_{thMosjh}$ is MOSFEETMOSFET thermal resistance from junction to external heat sink.

$$\text{So, } R_{thMosjh} = 2.3 + 0.5 = 2.8°C/W$$

$$R_{thMosha} = 0.16°C/W$$

Now if we check the diagram, (volume of component appendix 6) that gives us thermal power evacuated by this external heat sink for ΔT . We can see that this external heat sink is able to evacuate $12.5W$. Yet the power that has to evacuate MOSFEETMOSFET is $16.9.W$. So it is necessary to put a fan while using this external heat sink to provide thermal resistance that we calculate before. Thus we use diagram that gives us the air speed required by fan to respect such thermal resistance. In our case we can seen that air speed is $6ms^{-1}$.

In fact in an open system configuration it is very difficult to predict the air speed. This air speed is too important for such a small application. The possibility that can be adopted to reduce air speed is to use two MOSFEETMOSFETs in parallel. Indeed if the two MOSFEETMOSFETs are put in parallel the equivalent interne resistance will be divided by two. $R_{DSeq} = \frac{R_{DS}}{2}$ so the power losses calculated before will be reduce by two.

$$\boxed{P_{Moseq} = 8.45W}$$

Besides we can wonder if we still need an external heat sink for these two MOSFEETMOSFETs. Thus we calculate:

$$T_j = T_a + P_{Moseq} R_{thMos}$$

$$\text{with } R_{thMos} = 62°C/W \quad T_j \approx 574°C$$

this temperature is still too high and the MOSFEETMOSFETs will be destroyed. Thus the external heat sink chose before is still needed.

We use diagram in (volume of component appendix 6) that gives us thermal power evacuated by this external heat sink for ΔT . We need to evacuate $8.45W$ (external heat sink is able to evacuate $12.5W$). So we do not need to put a fan to respect the MOSFEETMOSFET maximal junction temperature that we have chosen.

To conclude we will adopt MOSFEETMOSFET parallel solution in order to avoid using a fan in the circuit.

II-4-d Clamping Circuit Design

The equivalent circuit that we introduced before (diagram 14) can't work in reality. Indeed the Leakage inductance stores energy that it will give to the switch in a very short period of time when it is opened. This energy delivering into the switch will create a huge voltage across it and will be able to destroy the switch. The temperature inside the switch will rise to high value and thermal transfer into the silicon will not be efficient to transfer heat to ambient air. So the switch will blow. That is why we need to use a clamping circuit in order to divert this energy. It we will be designed for the maximum duty cycle.

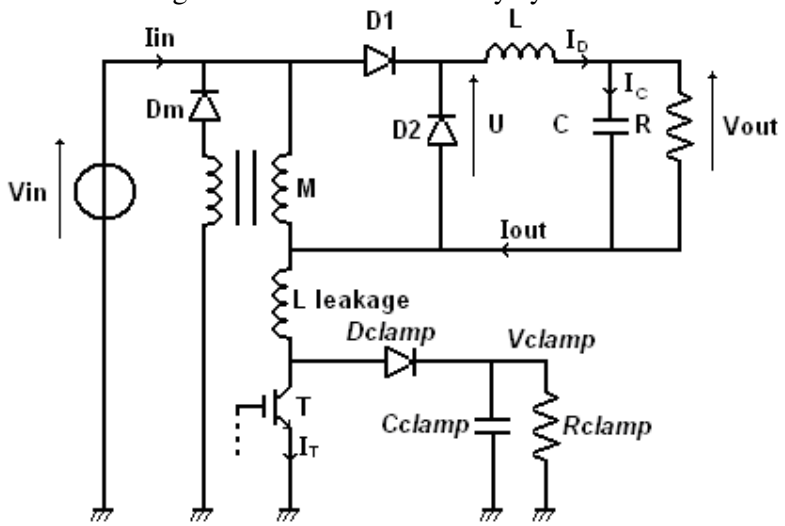

Figure 18: Equivalent circuit of the Forward converter when the transistor is blocking with the clamping circuit.

The figure that follows shows the importance of the clamping circuit in order to limit the voltage across the switch due to leakage inductance. We need to design the clamping circuit and especially the clamping resistance that will limit the voltage across the switch.

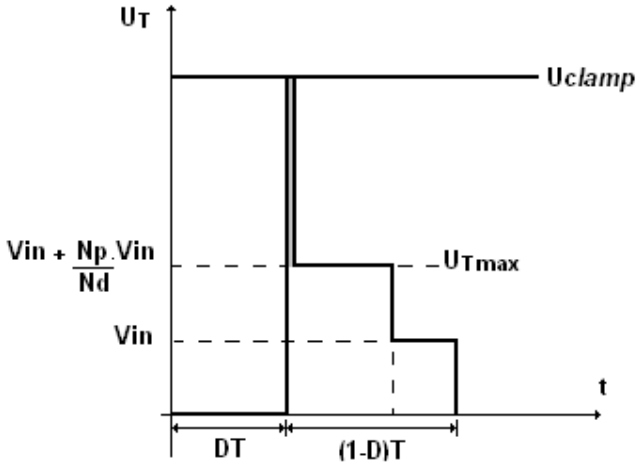

Figure 19: wave form of the IGBT.

In fact the power delivered to the clamping circuit is more than the power stored into the leakage inductance. $P_{clamp} = KP_{Leakage}$ with K a constant given by the expression :

$$K = \frac{1}{1 - \frac{2V_{in}}{U_{clamp}}}$$

We must choose the voltage clamping that we would like to expect in the clamping circuit. The theoretical maximum voltage applied across the switch is $U_T = 667V$. We consider that difference between $U_{T\max}$ and U_{clamp} when the impulsion is done will be $115V$ (value that can support the switch chosen). Thus $U_{clamp} = 781V$. So $K = 4.3$ and $P_{clamp} \approx 22W$

Besides (16) give us $P_{clamp} = \frac{U_{clamp}^{\ 2}}{R_{clamp}}$ thus we find the theoretical value the clamping resistor:

$$\boxed{R_{clamp} = 27.7k\Omega}$$

Then we simulate the circuit with *PSIM* and we obtain the result that follow:

$$\text{For } R_{clamp} = 28k\Omega \quad U_{clamp} = 714V \text{ and } U_{T\max} = 664V$$

Thus the difference between these two voltages is less than $115V$ so we will adopt:

$$\boxed{R_{clamp} = 28k\Omega}$$

Then we must select diode and capacitor. According to simulation diode rated voltage and average current are:

$$U_{Dclamp} = 707V \text{ and } \overline{I_{Dclamp}} = 0.027A$$

Then we choose Diode type **MUR1100/1000V/1A/high frequency**. Because $\overline{I_{Dclamp}}$ is very small in comparison with $1A$. We understand that the power losses will be very small in it, so any external heat sink is required. For the capacitor we can calculate theoretically the value of the capacitance.

$C_{clamp} = \frac{P_{clamp}}{fU_{clamp}\Delta V}$ with $\Delta V = 10V$ (voltage peak to peak), value usually taken by manufacturers. Thus we obtain $C_{clamp} = 56nF$

So, we choose $\boxed{C_{clamp} = 60nF}$ which is an industrial value.

II-4-e Choice of the diodes

Aims of $D1$ and $D2$ Diodes are to prevent negative current to flow through transformer secondary and to allow freewheeling during demagnetizion time. Dm aim is to allow demagnetization into the transformer.

Theoretical voltage into the secondary is $U_2 = \frac{N_S}{N_P}V_{in} \approx 67V$ and $U_{D2} \le U_2$. Besides, the maximum voltage that can drop theoretically into Dm diode is $U_{Dm} = 2V_{in} = 600V$ thus we

have to choose a diode with maximum rated voltage is equal to $2.5V_{in} = 750V$ for safety reason.

Rated voltage and average current of these diodes given by simulation are:

$$\text{For } D1\ U_{D1} = 81V \text{ and } \overline{I_{D1}} = 1.7A$$
$$\text{For } D2\ U_{D2} = 65V \text{ and } \overline{I_{D2}} = 3.35A$$
$$\text{For } Dm\ U_{Dm} = 540V \text{ and } \overline{I_{Dm}} = 0.13A$$

Thus we choose for $D1$ and $D2$ **DIODE MUR810/100V/8A/high frequency** and for Dm **DIODE MUR1100/1000V/1A/high frequency.**

II-4-f Diode thermal calculation

It is no use making a thermal calculation for Dm diode because $\overline{I_{Dm}} = 0.13A$ is very small compare to $1A$.
But we must calculate power losses across $D1$ and $D2$:

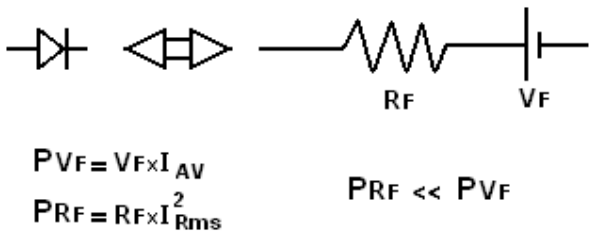

Figure 20: Equivalent representation of a diode.

$P_{D1} = V_F \overline{I_{D1}}$ with V_F the voltage drops into the diode. $V_F = 1V$ (volume of components appendix 6) and $P_{D2} = V_F \overline{I_{D2}}$.

$$\boxed{\begin{aligned} P_{D1} &= 1.7W \\ P_{D2} &= 3.35W \end{aligned}}$$

In fact tables do not give us diode total thermal resistance junction-ambient air. Nevertheless the diode used has a similar structure as the MOSFEETMOSFET. That is why we will choose as an approximation the following:

$$R_{thD1} = R_{thD2} = R_{thMos} = 62°C/W$$

$$\text{and } R_{thD1\,jh} = R_{thD2\,jh} = R_{thMosjh} = 2.3 + 0.5 = 2.8°C/W$$

First we are going to calculate the junction temperature in $D1$ and $D2$ diodes without an external heat sink.

$$T_{j1} = T_a + P_{D1} R_{thD}$$

Thus $\boxed{T_{j1} \approx 155°C \quad T_{j2} \approx 258°C}$

So we can see that temperatures which can rise into diodes without external heat sink being too huge for $D1$ and $D2$ diodes. They will be destroyed. Like for the MOSFEET we need to put external heat sink in order to put diodes into the worst situation that can occur without destroying it. For the same reason we choose **HS 3512 Heat Sink**.

Ambient air $T_a = 50°C$ and maximum junction temperature $T_{jD} = 100°C$

$$\text{So, } \Delta T = T_{jD} - T_a = 50°C$$

Total thermal diode resistance is given by:

$$\begin{cases} R_{thD1} = \dfrac{\Delta T_D}{P_{D1}} = 29.4°C/W \\ R_{thD2} = \dfrac{\Delta T_D}{P_{D2}} = 14.9°C/W \end{cases}$$

We need to evaluate external heat sink thermal resistance in order to respect maximum junction temperature.

$$R_{thD1ha} = R_{thD1} - R_{thD1jh}$$

$$\text{Thus we obtain} \begin{cases} R_{thD1ha} = 26.6°C/W \\ R_{thD2ha} = 12.1°C/W \end{cases}$$

Now if we check the diagram, (volume of components appendix 7) that gives us thermal power evacuated by this external heat sink for ΔT_D . We can see that this external heat sink is able to evacuate $5W$. Thus we understand that the heat sink is oversized for these diodes because the maximum power that diodes have to evacuate is $3.35W$. Nevertheless we keep this external heat sink because it is the smallest one that we can find in the *INEP* workshop.

Yet if we had wanted to save money we would have reduced the size of the external heat sink just to match with an evacuate power of $3.5W$.

External heat sink use fins in order to increase their surface to deliver to ambient air more heat. So reducing the surface will reduce the power evacuated by the heat sink.

III Auxiliary Power Supply (Gate driver circuit)

The auxiliary power supply creates the gate signal for the transistor of the forward converter in order to control the commutations.

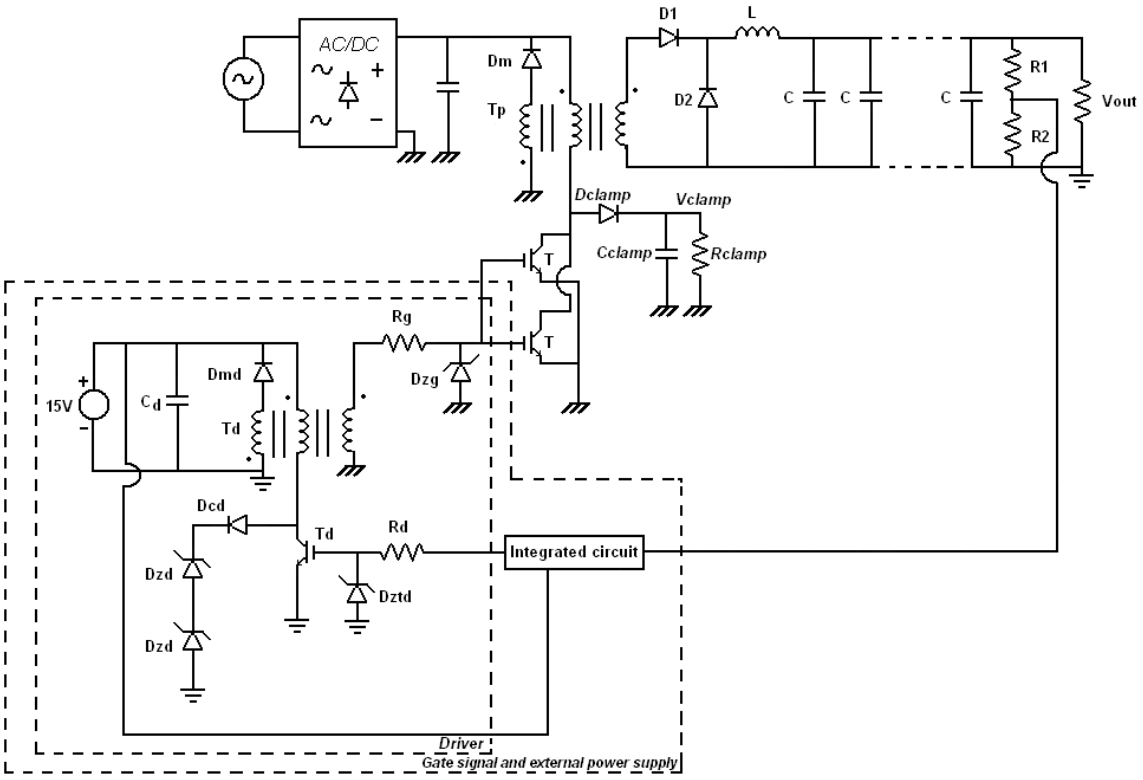

Figure 21: The auxiliary circuitry.

III-1 Driver and integrated circuit

Driver and integrated circuit are components needed to create the gate signal that commands switching of the power stage. Nevertheless driver and integrated circuit also need a control system provide a well regulated output voltage. Yet, in a first phase, we will design the gate driver integrated circuit without feedback control. Indeed we will test these two components over the power stage and manage the duty cycle thanks to a variable resistor. In order to realize an auxiliary power supply we will follow these steps:

- ✓ Gate driver design.
- ✓ Choice of the integrated circuit.
- ✓ Auxiliary power supply test.

III-2 Gate driver design.

To keep the isolation between the input and the output of the power stage, we need to design a driver in order to assure this function (figure 21). Thus we understand that if we want to provide isolation to integrated circuit we need to design an isolated gate driver.

As we can see the driver circuit looks like a small forward converter, supplied by a small power application of $15V$. This value comes from maximum gate to source voltage of switch power $V_{GS} = 20V$ (volume of components appendix 5). This small power will also supply the integrated circuit and then needs to be isolated. We could have designed this small power supply but it would have taken too much time. We will use a small, commercially available power supply.

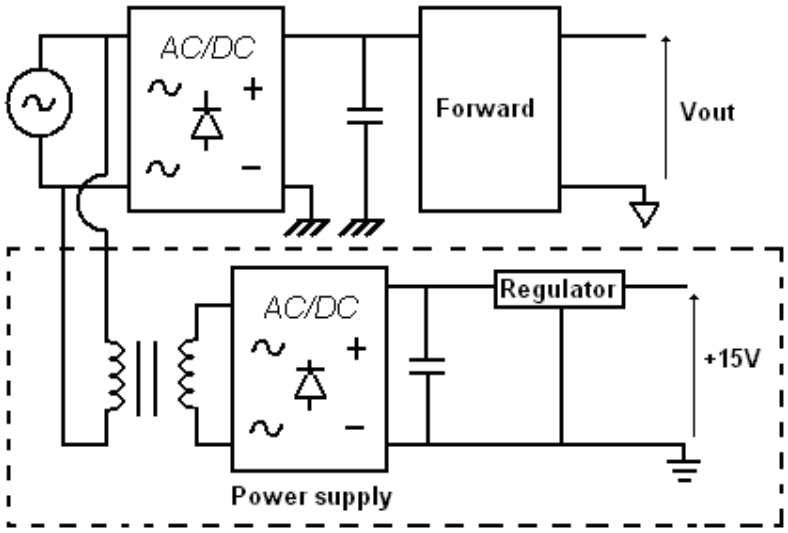

Figure 22: External power supply scheme.

It uses a small isolated transformer at low frequency ($6kHz$) that provides small power ($\approx 2W$). Now we must design our driver. It looks like a small forward transformer which doesn't use an output inductor and an output capacitor. We will use the same equation as used in part II to design all the component of the driver stage. First we need to give project data that will be used to design this small circuit:

$V_{ind} = V_{in\min d} = 15V$	$V_{outd} = 15V$	$\eta = 0.8$	$k_w = 0.4$	$J_{\max} = 450A/cm^2$
$P_{in} = 6.25W$	$P_{outd} = 5W$	$f = 50kHz$	$k_p = 0.5$	$\Delta B = 0.3T$
$I_{ind} = 0.42A$	$I_{outd} = 0.33A$	$D_{\max} = 0.45$	$k = 0.7$	$B_{\max} = 0.3T$

These data are close to the reality. Most of them come from the second part data and from software simulation. Before starting the transformer calculation we need to precise the data value chosen and notably why the output power of the driver is $P_{outd} = 5W$. The power needed for the gate of power stage switch is the same as the power needed to load the capacitor inside

the MOSFEET gate. We have access to the capacitance according to switch table (volume of components appendix 5). $C_{iss} = 500\,pF$

Thus $P_{outd} = \frac{1}{2} C_{iss} V_{GS}{}^2 f = 2.8.10^{-3} W$. It is too small a power value. We choose $\boxed{P_{outd} = 5W}$.

Choosing this power means that we are going to oversize again the driver transformer. Oversizing the transformer is needed for two specific reasons. First if we design too accurately our transformer we will face mechanical problem to build it. Second *INEP* workshop doesn't have too small core transformer. Besides we keep the other values from the power stage design because our transformer won't be accurate, it doesn't matter if we keep the same values.

III-2-a Design of driver transformer core

As was done in the second part we use the same equation (6). $\boxed{(A_e A_w)_d = 0.056 cm^4}$

We chose $(A_e A_w)_d = 0.08 cm^4$ this value matches with the **E-20** type core (volume of components appendix 1). So, $A_{ed} = 0.312 cm^2$

III-2-b Number of wire turns

According to (7) $\boxed{N_P = 14.4}$ **15 turns** is first adopted. To simplify the design we choose to have the same input and output voltage in the driver. So, $N_P = N_s = N_d = 15$. Even if the number of turns is the same the demagnetization will be fulfilled.

III-2-c Wires diameter

We have the same RMS current (efficient current) in each winding. $I_{rms} = \frac{I_{outd}}{\sqrt{2}} = 0.23A$.

So, $\boxed{AWG_{driver} = 29}$. We also reduce the skin effect because we have oversized our design.

III-2-d Measure of the driver transformer's losses

We put an air gap $g = 0.3mm$ in the transformer that we built. And we measure inductances $L_{dLeakage} = 12.8\mu H$, $M_d = 19.8\mu H$ and (10) give us $I_{md} = 7A$. So the magnetized current is too important for such a small application. It will destroy our driver circuit. The only way to reduce such current while keeping the same air gap is to increase the number of turns. We proceed with the same equation (16) as for the input inductor.

$M_d = \frac{N^2}{\mathrm{Re}\, l}$ with $\mathrm{Re}\, l$ the reluctance of the core. Thus $\mathrm{Re}\, l = 11.5.10^6$ is calculated for 15 turns. So we can evaluate the magnetizing inductance needed to design transformer with having a magnetized current of $1A$.

$$M_d \geq \frac{V_{ind} D_{\max}}{I_{md} f} = 137\mu F$$

Finally $\boxed{N = \sqrt{M_d \operatorname{Re} l} = 40}$. So we build a new driver transformer with the same characteristics but we adopt **40 Turns and an air gap.** Finally, we test it and we obtain. $L_{dLeakage} = 32.2\mu H$, $M_d = 138\mu H$ and $I_{md} = 0.97A$ and we get $\boxed{P_{dLeakage} = 1.4W}$ these losses stored in the leakage inductance are not too high for this small application.

III-2-e Heat calculation

Driver transformer is over designed for an output power 2000 times higher than it is needed. That is why it is not required to make a thermal calculation. We truly know that the temperature into the transformer will never rise to the maximum temperature allowed by the component even if it the worst situation (maximum ambient air temperature).

III-3 Determination of the driver switch

As was done in part II we will choose components from the *INEP* workshop. That is why some component will be over size to match with manufacturer values. Driver is a very small power application thus it will be useless to make thermal calculation for components.

The driver switch is connected to the integrated circuit. Its commutation state changes, because of the integrated circuit. Thus it will provide the commutation operation of the power stage switch. Theoretical maximum voltage applied across the switch is: $U_{Td} = 2V_{ind}$ $U_T = 30V$. Efficient current that flows through driver switch is $I_{rmsTd} = 0.29A$
RMS current is so small that thermal calculation is useless and we don't need to put an external heat sink. So we consider using an **IRF532/MOSFET/ 100V/high frequency** (available in the INEP workshop).

III-4 Driver circuit protection Design

Like in part II we have to design a protection circuit, (figure 21) notably for driver switch (D_{cd}, D_{Zd}) but also for the gate power stage switch (D_{ZG}, R_G) and gate driver switch (D_{Ztd}, R_d).
We will use software simulation to get the required electrical values, and then we will choose the closest components needed available in the *INEP* workshop.

III-4-a Switch gate power stage protection

The power stage switch gate must be protected since characteristics of the power stage switch prevent us from applying on it more than $20V$ (volume of components appendix 5). Thus we must select a ZenerZener diode to prevent high voltage rising and a resistor. So we want to have a maximum voltage of $20V$ applied to the gate. Besides according to simulation $U_{ZG} = 14.8V$ and $\overline{I_{RG}} = 0.2A$ thus we choose **Zener Diode/20V/1A/high frequency** (D_{ZG})**.**

The resistor resistance is given by the equation: $t_r = 2.2 C_{iss} R_G$ with $t_r = 17ns$: rise time given by MOSFET characteristic, $C_{iss} = 500\,pF$ the capacitance of interne gate capacitor (inside the power stage switch).
So, $R_G = 15.4\Omega$. Yet this value is not a commercial value. Thus we choose $\boxed{R_G = 22\Omega}$. Besides, there is another parameter to select the appropriate resistor. We must know the losses expected into this resistor. According to the introduction of part III, fixed output power to design driver circuit is $5W$. We expect that power losses in the resistance must be 20 times less than this. Power losses in the resistor must be $\boxed{2.5.10^{-1} W}$.

III-4-b Driver switch protection

We will use a standard diode (D_{cd}) and a ZenerZener diode (D_{Zd}) in this circuit. The aim of Zener diode is to protect driver switch from high voltage rising. Diode rated voltage and average current are: $U_{cd} = 13.3V$ and $\overline{I_{cd}} = 0.002A$. Thus we choose **MUR810/100V/1A/high frequency** for the standard diode.

We want to have a maximum voltage of $40V$ applied to the driver switch. Besides thanks to simulation rated Zener voltage is $U_{Zd} = 40V$ and $\overline{I_{cd}} = 0.002A$. So, we choose **Zender Diode/40V/1A/high frequency** for the Zener diode.

III-4-c Driver switch gate protection

As in power stage the gate of this small switch must be protected. We proceed in the same way and taking the same component ($R_d = R_G$ and $D_{Ztd} = D_{ZG}$). Even if it is oversize we are sure that the gate will be protected, besides they are the smallest components available in *INEP*.

III-4-d Driver demagnetizion diode.

As in power stage this diode allows demagnetization of the driver transformer. The maximum voltage that can drop theoretically into Dmd diode is $U_{Dmd} = 2V_{ind} = 30V$ thus we have to choose a diode with maximum rated voltage is equal to :

$$2.5V_{in} = 75V$$

Rated voltage and average current of these diodes given by simulation are $U_{Dmd} = 30V$ and $\overline{I_{Dm}} = 0.004A$ so we choose **MUR810/100V/1A/high frequency.**

III-5 Integrated circuit.

The PWM control integrated circuit provides the duty cycle and the elements to implement the control for a basic dc-dc converter. In fact the duty cycle is generated by the comparison between a triangular signal and a continued signal. Thus Integrated circuit is a very complicated component since it uses miniaturized transistors and comparators. We will choose one from the *INEP* workshop. The main one available and suitable for this kind of application is: **INTEGRATED CIRCUIT UC3525.**

First we are going to design the external components needed to connect the integrated circuit to the power circuit. These external components enable us to settle the integrated circuit operating conditions. To fulfill this design we will use integrated circuit characteristics. In the first design a variable resistor (R_P) will be used to control manually the duty cycle and see if results expected by simulation are accurate as it can be seen in the figure 23.

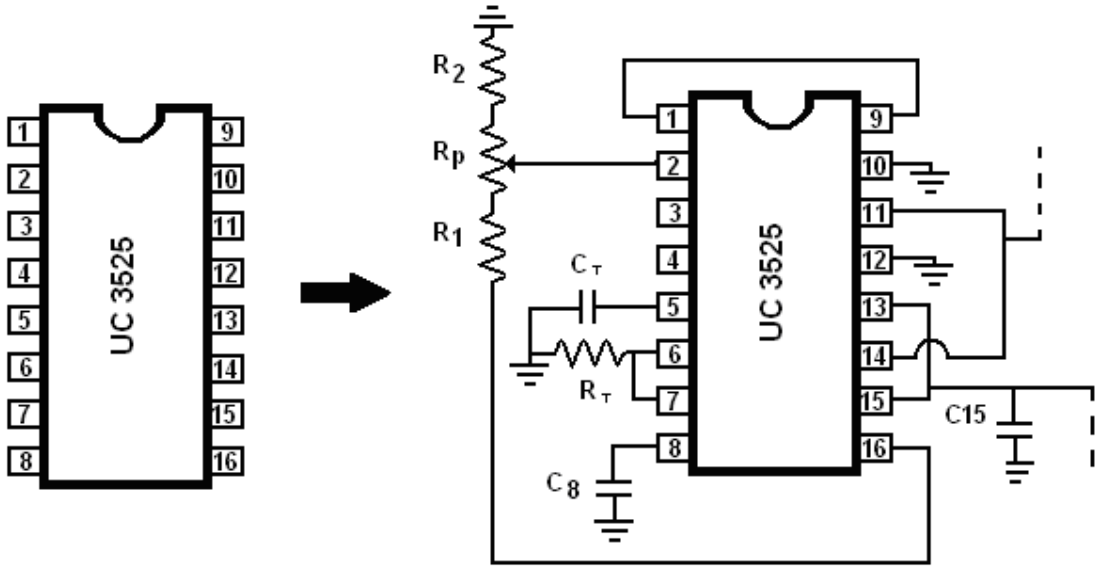

Figure 23: The PWM integrated circuit.

$C_8 = 5\mu F$, $C_{15} = 1\mu F$ and $R_T = 2.86k\Omega$ are given by the integrated circuit tables (volume of components appendix 8). The component C_T Ct and R_T fixed the frequency for the integrated

circuit. Indeed we prefer to fix R_T because resistor variation is less important than capacitor variation. Thus thanks to the relation given by manufacturer $C_T = \frac{1}{f(0.7R_T)} = 0.01\mu F$

R_2, R_P, R_1 compose the scheme of the variable resistor. In fact the value given to this resistor will correspond to the maximum and the minimum value that the duty cycle can take.

Thus the duty cycle will evaluated between these two limit values. In order to create the time D of the duty cycle the integrated circuit compare a triangular signal with a gate signal V_O (figure 24).

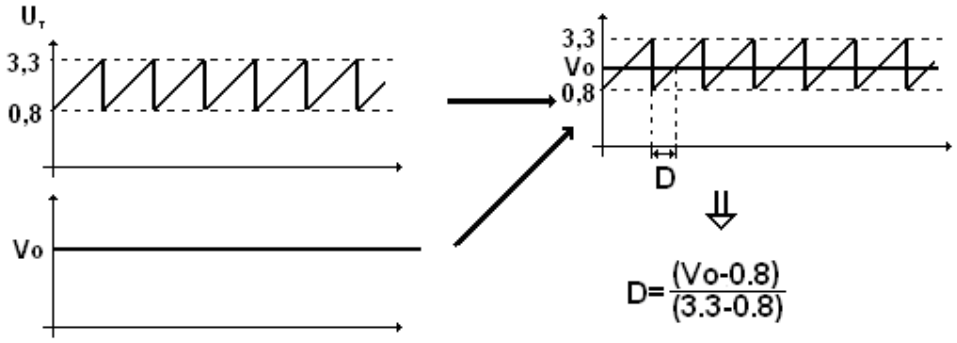

Figure 24: Generation of the duty cycle.

So, thanks to the characteristics of the integrated circuit we can find the value of R_2, R_P, R_1 (figure 23).

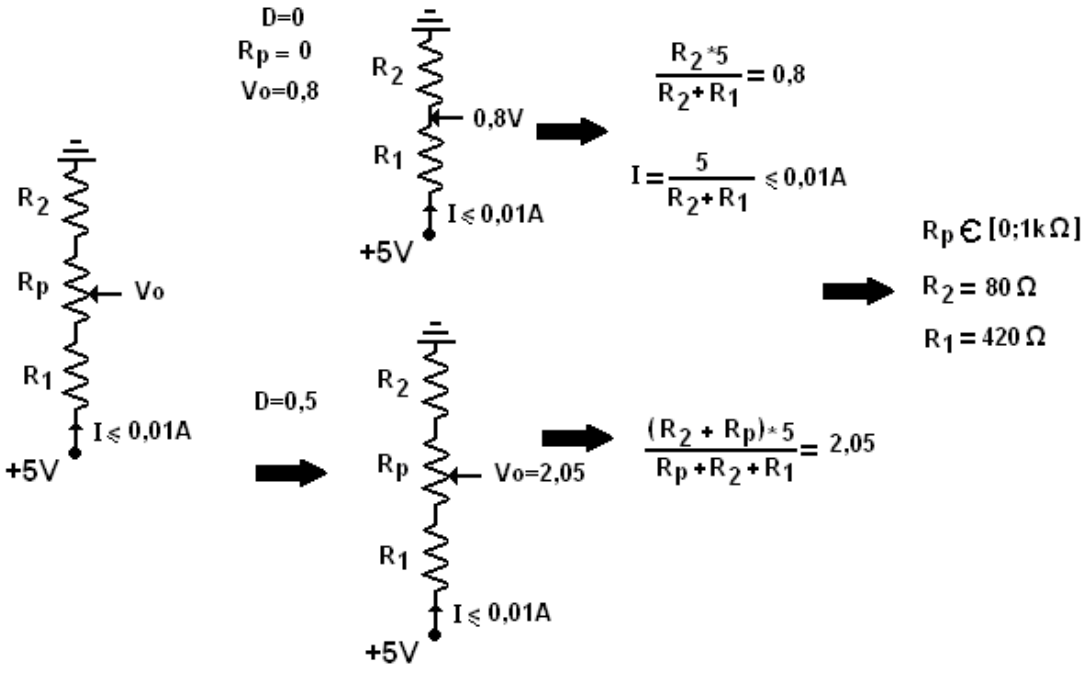

Figure 25: Calculation of the resistor for the integrated circuit.

For more safety we will take the double for all the resistors. To conclude the different connections are given in the volume of components appendix 8. Then we could give the last scheme (figure 26) to the technicians and then confirm our result with our prototype.

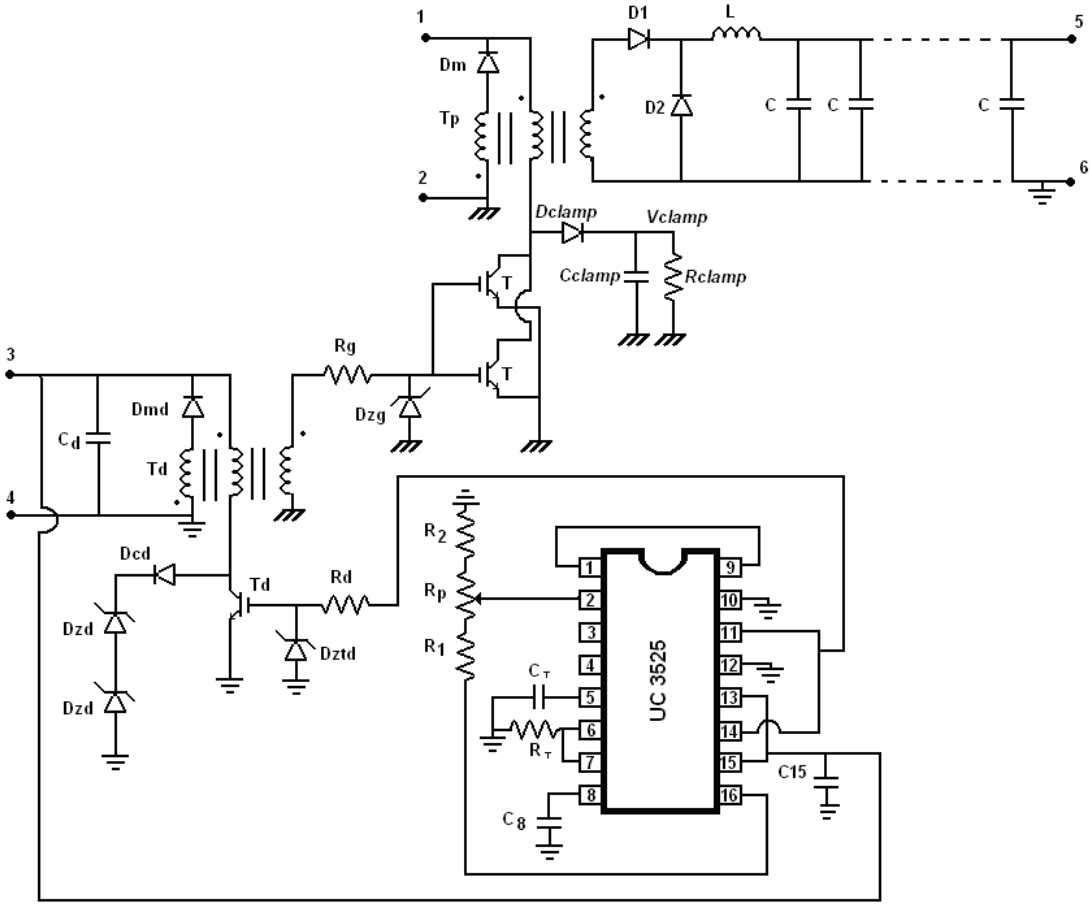

Figure 26: General scheme for the technicians.

IV Test of the laboratory prototype

We start to test the built prototype. We proceed step by step in order to prevent the destruction of components if we need to adjust some value. Thus we connected each part of the full circuit one by one.

IV-1 PWM integrated circuit test

First we test the IC that will provide the duty cycle. After observing waveform of the IC we noticed that we were at saturation in the driver. The duty cycle was higher than 0.5 because the first value chosen for the variable resistor was too high. We decided to limit the duty cycle from 0 to 0.5 through an easy operation. Indeed there are two outputs of the IC that provide duty cycle. Both are displaced of $180°$. Thus, if we connect both of them together the duty cycle will be generated between 0 and 1. Besides each output has the same frequency. Thus if we sum both by connecting them together the frequency will be the half.
So we decided to short circuit the 14 output and thus to multiply frequency by two in order to keep the same frequency. So we find the new capacitor $C_T = \frac{1}{2f(0.7R_T)} = 0.05\mu F$ that we must include in our IC (we kept the same resistor R_T).

After testing it again we notice that the transformer driver was never saturated for different values of the variable resistor because the duty cycle was now limited between 0 and 0.5.

IV-2 Driver circuit test

In the driver we faced only one problem with the resistor R_G. Indeed we under evaluated the power losses in this resistor. The losses are given by (16) $P_G = \frac{V_G{}^2}{R_G}$. In fact maximum value that can reach V_G is less than $15V$ since the driver transformer has a turn ratio of 1. So the losses that can support this resistor is $P_G \approx 5W$ which is too high since the driver circuit was designed to provide $5W$. The resistor used can only withstand $1W$. So it would be destroyed. The losses come from the discharge of the inner capacitor of both power stage switches and provide a negative current through the resistor. One option to reduce these losses and so to minimize this negative current is to integrate into the PC board the scheme that follows.

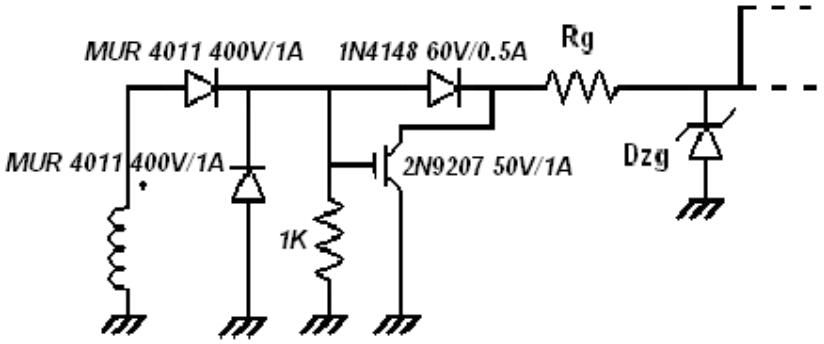

Figure 25: Scheme to reduce losses of Rg.

This option is usually used by manufacturer as soon as they want to reduce power losses into the driver circuit. So the current that follows must be very low and the component used must support higher voltage than the voltage provided by the dc supply. Thus this option helps to divert the negative current into another resistor higher than R_G and thus, drastically reduces the losses in the circuit.

IV-3 Power stage test

Then we tested the main part of the converter. First we noticed that to have accurate results we need to connect a high capacitor in parallel in input. Indeed, the wires used to connect input converter to grid are too long and have an inductance. Thus to cancel the voltage drop effects of this inductance we connect a $1\mu F$ capacitor very close to the PCB dc input terminals.

We started to supply the power stage and run it at half power. Thus we checked the heat of component to see if nothing was burning. What appeared in half power is that the resistor in the clamping circuit was rising to a very high temperature without being destroyed but for more safety we decided to put several resistors in parallel (with the same total value) in order to reduce the heat. Thus we checked thanks to an oscilloscope all the fundamental waveforms and we saw that the converter was delivering $20V$ in output and the waveform was the ones expected as in the figure 10.

Finally we run the power stage to full power for different value of the duty cycle, input voltage or output current (by changing the load) and took the different values (appendix 1).
It gave us an access to the efficiency of our prototype which is the most important parameter to define if the design is accurate or not.

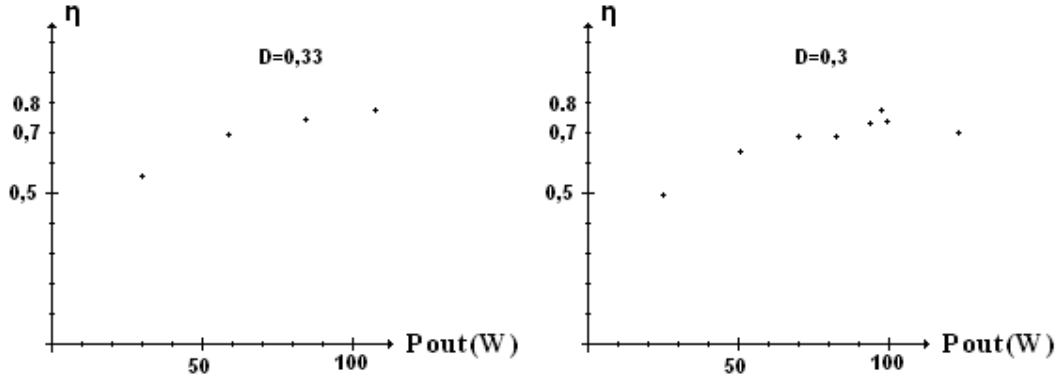

Figure26: Efficiency functions of output power.

We can see that to have the exact value of $20V$ in output for $300V$ in input the duty cycle must be $D = 0.31$ unless the efficiency is $\eta = 74\%$. We obtained the best efficiency around 77% around the input values which were used for the design of our forward. The efficiency reach its limit around Pout=100W which was expected.

So, we succeed in the realization of our forward converter because the experimental tests showed that waveforms and values were close to the ones which were expected.

V Control design and final test

Forward converter provide dc supply to very sensitive electronic loads. Thus if the voltage deliver to this electronic load (in our case a laptop computer) changes too much they can be destroyed.

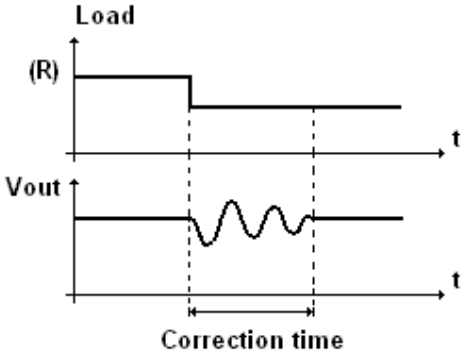

Figure29: Efficiency functions of output power.

That is why a control circuit is needed to adjust the duty cycle as soon as a parameter changes in order to keep always the same value of the output voltage.

Voltage can change if input voltage changes, if the load changes, if the temperature changes. To conclude the output load is intolerant to output voltage variation. That is why an accurate control is needed.

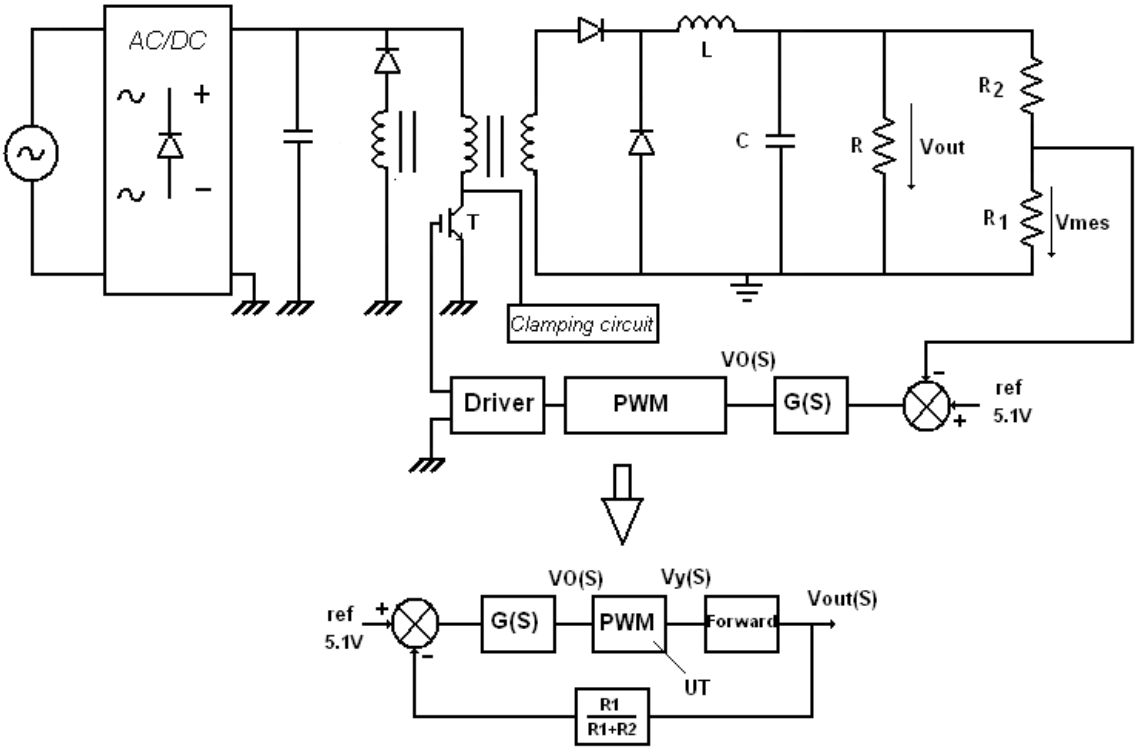

Figure30: Appropriate representation for the transfer function

We simplify the circuit by an equivalent circuit which is the appropriate representation in order to deduce main transfer function of the control circuit (figure 30).

In this process we need to deduce the transfer function of the power stage. After analysis his bode representation, we can deduce the type of controllercontroller that we need. Indeed the controllercontroller will help to have a full system stable and as fast as possible.

V-1 Pulse with modulator (PWM)

The PWM is a component inside of the integrated circuit (input points 1 and 2, both connected to output 9.). It aims is to compare an ideal voltage with voltage that is required at the power stage output. A reference voltage is provided by the IC. According to the table (volume of components appendix 8) the reference voltage is $5.1V$. Resistors R_1 and R_2 are needed to connect the output load to the PWM. We must determine resistors, the calculation is made for $V_{out} = 20V$ $\frac{V_{mes}}{V_{out}} = \frac{5.1}{20} = \frac{R_1}{R_1 + R_2} = 0.25$, besides we also want to limit the power losses of theses resistors

$$\frac{V_{mes}{}^2}{R_1} + \frac{(V_{out} - V_{mes})^2}{R_2} \leq \frac{1}{8}$$

So we deduce $R_1 = 816\Omega$ and $R_2 = 2384\Omega$. Later commercial values will be used and we will connect these resistors to the PC board.

V-2 Power stage transfer function

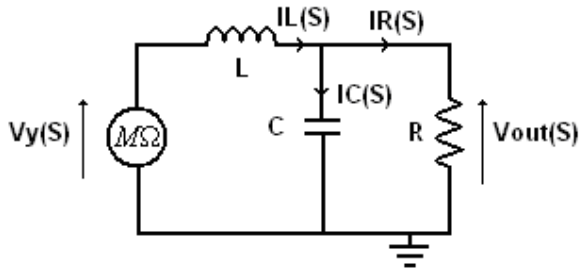

Figure31: Equivalent scheme of the forward transformer.

We use Laplace transform of the electrical equations giving by the equivalent circuit. Main equation provided by Kirchhof's law:

$$i_R(s) = \frac{V_{out}(s)}{R},\ i_C(s) = sCV_{out}(s),\ i_L(s) = i_C(s) + i_R(s) = sCV_{out}(s) + \frac{V_{out}(s)}{R}$$

$$V_L(s) = sLi_L(s) \text{ and } V_L(s) = V_y(s) - V_{out}(s).$$

$$\frac{V_{out}(s)}{V_y(s)} = \frac{1}{1 + s\frac{L}{R} + s^2LC}$$

Besides $V_y(s) = D(s)V_{in}\frac{N_S}{N_P}$ (main expression of the forward converter giving by (3)).

The IC provides the duty cycle (scheme 24) $D(s) = \frac{V_O(s)}{U_T}$.

Thus we obtain the transfer function of this two blocs:

$$\boxed{\frac{V_{out}(s)}{V_O(s)} = \frac{\frac{V_{in}}{U_T} \times \frac{N_S}{N_P}}{1 + s\frac{L}{R} + s^2LC}}$$

We will design the controller for the worst situation. It appears when $R \to +\infty$, it means that $P_{out} \to 0$. So the main transfer function that we will study is

$\boxed{H(s) = \frac{V_{out}(s)}{V_O(s)} = \frac{\frac{V_{in}}{U_T} \times \frac{N_S}{N_P}}{1 + s^2LC}}$ (18) his cut frequency is $f_o = \frac{1}{2\pi\sqrt{LC}} = 272Hz$ and his static gain is $K = \frac{V_{in}}{U_T} \times \frac{N_S}{N_P}$ ($U_T = 2.4V$ is the triangular voltage provided by the IC manufacturer).

This transfer function is a second order. The scheme that follow show the bode representation of $H(s)$, and the Bode representation in open loop wished to have a full system stable and fast.

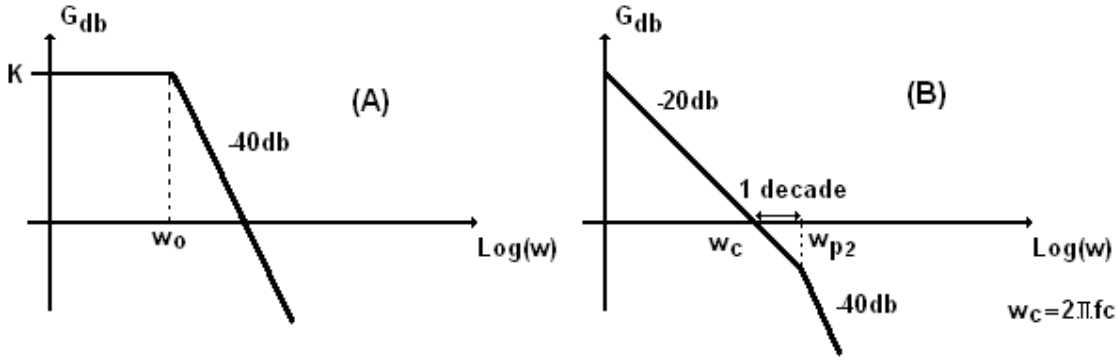

Figure32: (A) Bode diagram of the power stage (B) Ideal Bode diagram for a fast and stable system.

The cut frequency wishes is fix by us, but it has to respect the Shannon's theorem.

$$f_c \approx \frac{f}{10} \leq \frac{f}{2}(Shannon) \text{ so } f_c = 5kHz .$$

So to obtain this ideal Bode diagram we must add a controller before the PWM.

V-3 Controller transfer function

The controllercontroller aims is to provide stability and rapidity to the full system. That is the most important element of the control circuit. Thus we must design this component to get an a bode diagram close from the ideal one. In a forward converter, the controller usually used by manufacturers is the one that follow (figure 31).

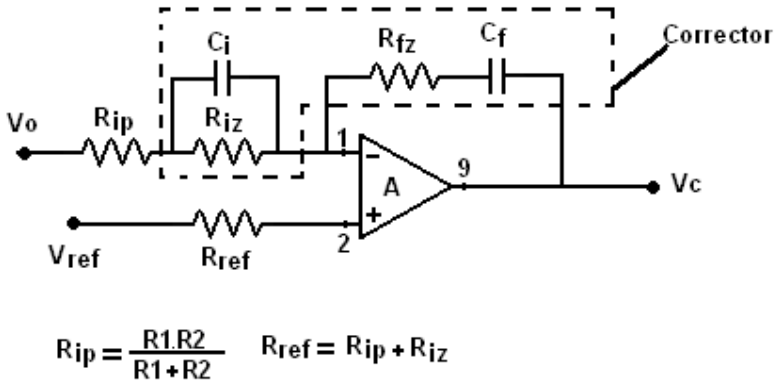

Figure33: Scheme of the controller.

Manufacturers choose this type of controller because its Bode diagram is appropriate to obtain a full system stable and fast.

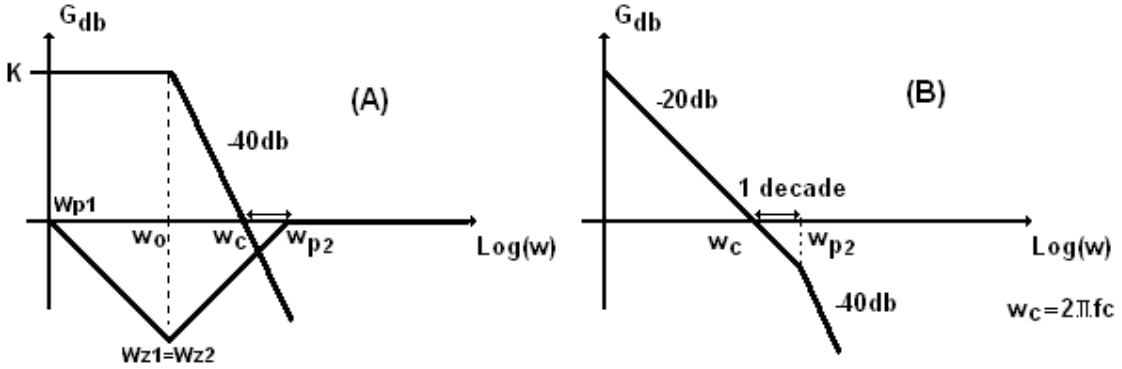

Figure34: (A)Bode diagram of power stage and controller (B)Sum of the two Bode diagram from (A)

The controller transfer function is $\boxed{G(s)=\dfrac{(1+R_{iz}C_i s)(1+C_f R_{fz} s)}{C_f s(R_{ip}+R_{iz})(1+C_i s\dfrac{R_{ip}R_{iz}}{R_{iz}+R_{ip}})}}$ (19)

This expression comes from the circuit analysis that we won't detail. We have to determine the different components of this controller C_i, R_{iz}, R_{fz}, C_f.

We must use equations given by transfer function and Bode diagram analysis.

Thus we obtain four equations:

$$f_{P1}=0,\quad f_{Z1}=f_0=\frac{1}{2\pi C_i R_{iz}},\quad f_{Z2}=f_0=\frac{1}{2\pi C_f R_{fz}},\quad f_{P2}=10f_C=\frac{1}{2\pi C_i(\dfrac{R_{ip}R_{iz}}{R_{iz}+R_{ip}})}$$

$$G_{dB}(G(f_c))=\frac{1}{G_{dB}(H(f_c))}.$$

By using MAPPLE software we solve this system of equations. So we obtain $C_i=5.3nF$, $R_{iz}=111k\Omega$, $R_{fz}=91k\Omega$, $C_f=6.4nF$, $R_{iP}=607\Omega$, $R_{ref}=111{,}6k\Omega$.

Beside we need to take commercial values so we will adopt: $R_1=820\Omega$, $R_2=2200\Omega$, $C_i=5.6nF$, $R_{iz}=120k\Omega$, $R_{fz}=82k\Omega$, $C_f=6.8nF$ and $R_{ref}=120k\Omega$. R_{iP} is replace by R_1 and R_2 in parallel.

V-4 Final test.

Before building the control circuit we test elements by numerical simulation to check if the control is operating well. Thus we can see that the designed circuit is working. Indeed if output load change quickly the control changes rapidly the duty cycle in order to still deliver $20V$ in output. Besides the time correction is small. So we built the controller and test it on the PC board. We can see that the control is operating, the output voltage was regulated and fixed at $20V$ even if the load changes. Nevertheless we were not able to supply the circuit with more than $V_{in}=180V$. Indeed noise appears into the output inductance. The noise was

produce by too high frequency, which makes the inductance core tremble. Thus one solution to reduce noise is to filter high frequency emissions by adding another capacitor in parallel of R_{fz} and C_f.

By adding this new capacitor we create a new pole in system transfer function that cut high frequency at $f_c = 2kHz$. (Simulation allow us to measure the value of the frequency cut) First we used $C_+ = 100nF$. We notice that noise disappeared and regulation was sill working. Nevertheless response to fast load changes was too slow (more than $10ms$). We made a new numerical simulation to find the appropriate value and to have a rapid answer to load variations. $C_+ = 1nF$. Finally we test the circuit again. We see that noise disappeared and control was properly operated.

Besides it was much faster to a load variation than with $C_+ = 100nF$.

To conclude control operates well its main function: to provide quickly the appropriate duty cycle even if the output load change in order to still have $20V$ in output. This is the end of the full design of a Forward converter.

CONCLUSION

The design of a Forward converter demands great precision when calculating the different parameters and restrictions that will have to be applied when conceiving the model. The first step of the design was the understanding of the Forward converter. The comprehension of the different waves forms and the link between the transformer, the duty cycle and the input and output voltage. Once this had been done it was possible to proceed to the forward design and to see that the transformer was really the heart of the converter. During this phase we went step by step to design all the circuit elements such as output capacitor and inductor, diodes, switches, clamping circuit, driver and integrated circuit. We saw that each problem's solution made a new one appears which had to be solved to proceed to the other step. The design appears like a compromise of plenty parameters and can't be totally accurate. Indeed during this phase we have to choose commercial values components not too far from the numerical results. We oversized some components not to face mechanical problems. Finally we made thermal calculations in order to check if components would not have been destroyed as soon as they are supplied.

The laboratory test shows us how the numerical simulation first used in design was powerful. Indeed it allows to predict waveforms and to have a first idea of how the components will react. Besides, during test we faced some problems that showed that at some points, the circuit was wrong. Numerical simulation completed by laboratory test helped us to solve these problems. Finally the control of the full system was the last part we studied. Indeed it appeared that the control was the brain of the converter.

The control provides the security of the converter, it checks if values expected are fulfilled and adjust parameters if the nature of the circuit changes.

To conclude this project allows us to understand how engineer works to design and realize a complex power electronics system. Besides we learned how to work with numerical simulation and calculation softwares, we understanded the method to solve problems in the design stage but also in the test stage of a project. Thus, one of the best proofs is that we finally arrived to good results for this system that we entirely calculated and realized. Besides, this type of power electronics szstem is used today in plenty of consumer electronics such as laptop computer but also electric engines. It is the first step to introduce to more and more complicated system.

APPENDIX

Appendix 1: Table of values from experiment of our forward

Input parameters			Output values				
D	**Iout(A)**	**Vin(V)**	**Vout(V)**	**Iin(A)**	**Pin(W)**	**Pout(W)**	**η**
0,4	**7,2**	**247**	**19,3**	**0,75**	**185**	**138**	**74,6%**
0,4	**3,85**	**252**	**20,5**	**0,43**	**108**	**79**	**73,1%**
0,33	**1,35**	**285**	**21,9**	**0,19**	**54**	**29,5**	**54,5%**
0,33	**2,7**	**285**	**21,6**	**0,29**	**84**	**58,4**	**69,5%**
0,33	**4**	**285**	**21,1**	**0,4**	**114**	**84**	**73,6%**
0,33	**5,2**	**285**	**20,8**	**0,49**	**140,5**	**108**	**76,8%**
0,3	**1,2**	**300**	**20,8**	**0,17**	**52**	**25**	**49%**

0,3	**2,5**	**300**	**20,2**	**0,26**	**78**	**50,5**	**64,8%**
0,3	**3,6**	**300**	**19,7**	**0,35**	**105**	**70**	**67,5%**
0,3	**4,5**	**300**	**18,5**	**0,41**	**123**	**83,2**	**67%**
0,3	**4,8**	**300**	**19,6**	**0,43**	**129**	**94**	**73%**
0,3	**4,9**	**300**	**19,9**	**0,42**	**126**	**97**	**77%**
0, 3	**5,5**	**300**	**18**	**0,47**	**134**	**99**	**73,8%**
0,3	**6,5**	**300**	**18,4**	**0,56**	**168**	**119**	**70%**
0,31	**5**	**300**	**20**	**0,45**	**135**	**100**	**74%**

Bibliography

Classical Referencies

[1]Ivo Barbi, 2007. – Electrônica de Potência: Projetos de fonts chaveadas, Florianópolis, Ediçao do Autor.
[2] Presses Polytechniques et Universitaires Romandes, Philippe Barrade, 2006. – Electronique de Puissance : Méthodologie et Convertisseurs Elémentaires.
[3] R.R Donnelly and Sons Compagny, Abraham I. Pressman, 1991. – Switching Power Supply Design.
[4] M. Charpentier lesson, Ecole Navale. – Electronique de Puissance.
[5] Herbert P. Neff, Jr. lesson, University of Tennessee. – Introductory Electromagnetics.

Web Sites

[6] http://www.ivobarbi.com/PDF/LabPotencia08-01/UC3525.pdf
[7] http://www.ivobarbi.com/PDF/LabPot08-02/Circuitos%20de%20Comando_2008.2.pdf
[8] http://www.ivobarbi.com/PDF/LabPotencia08-01/Grampeadores.pdf
[9] http://www.datasheetcatalog.org/datasheet/irf/irfbg20.pdf
[10] http://www.datasheetcatalog.org/datasheet/motorola/IRF532.pdf
[11] http://www.datasheetcatalog.org/datasheet/SGSThomsonMicroelectronics/mXtwqrx.pdf

[12] http://www.datasheetcatalog.org/datasheet/SGSThomsonMicroelectronics/mXtxuvq.pdf
[13] http://www.epcos.com/inf/20/30/db/alu_03/03710385.pdf
[14] http://www.hsdissipadores.com.br/catalogo.pdf
[15] http://www.digchip.com/datasheets/parts/mu/parts_mu07.php
[16] http://www.digchip.com/datasheets/parts/datasheet/284/MUR1100.php