STUDY OF A SINGLE-PHASE SINUSOIDAL INVERTER FOR NONLINEAR LOADS
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Introduction

Inverters are a very common application of power electronics. The aim is to obtain a sinusoidal current or voltage from a continuous source in order to supply power to any kind of load. Nowadays almost all modern loads are nonlinear loads, which can have very disturbing effects on the quality of the output and the plant itself.

This project aims to design an inverter power supply using Insulated Gate Bipolar Transistors (IGBT). The plant has to provide a power of 3 kVA to a nonlinear load using a continuous voltage source of 250V.

First the general structure of such a plant will be studied for linear loads without feedback control. Then, a voltage compensator will be designed in order to improve the output signal and to provide a feedback. Finally nonlinear loads and their effects on the inverter will be studied. At the same time the effects of different parameters on the output waveforms will be examined.

The inverter parameters obtained after proceeding like this will be the base for the practical work.

PART I

1. Introduction

This first part of the study starts off with a general reminder of how full-bridge inverters work. The comprehension of the principles of operation of this type of converter is important to be able to proceed with the design of a voltage inverter.

The next step will be to explain two of the modulation strategies generally employed, in order to choose the right method. The choice of the modulation strategy is very important for the quality of the filtering of the output voltage. In fact the aim is to isolate the fundamental of the output signal as much as possible, by increasing the frequency of the harmonics. This will make it easier to filter the fundamental in order to obtain a sinusoidal output voltage close to the carrier signal used.

Before proceeding to the study and the design of the filter employed, the different modulation strategies will be simulated in order to verify the theory.

2. Principles of operation of a full-bridge inverter

There are different ways to invert voltage when working with a single-phase system: a push-pull inverter, a half-bridge inverter or a full-bridge inverter (with four switches). This study will focus on the full-bridge inverter.

In the beginning of the research, perfect operating conditions for the full-bridge inverter are assumed. That means the switches used are perfect and do not cause any losses. Furthermore an ideal load is used that absorbs an alternative current.

Using semiconductors, it is important to take the characteristics of the source and connection rules into consideration.

When designing a full-bridge converter, it is important to employ an input source whose nature is different from the one of the load. That means a source that provides a continuous
voltage has to be used, as the load will be working with alternative current. In fact consider the load can be considered as a source. In order to respect the uniqueness of potential in a point, it is forbidden to connect two voltage sources one to the other. The effect would be a short circuit that would cause a very strong or theoretically unlimited current.

The general design of a full-bridge inverter consists of four switches powered by a direct voltage source (fig. 2.1). The switches $S_1$, $S_2$ and $S_3$, $S_4$ compose two commutation cells $C_1$ and $C_2$. The switches of one commutation cell cannot be closed at the same time, for the reason explained before. Whenever $S_1$ is closed $S_2$ will be open, for example.

![Fig. 2.1: General design of a full-bridge inverter](image)

3. Modulation strategies

Several types of modulation exist, but for this project the Pulse-Width Modulation (PWM) has been preferred. The PWM permits to reduce significantly the harmonics of the output signal, which is important for improving the output waveform. In fact the PWM compares a triangular wave to a sinusoidal reference signal. This comparison determines the impulsions used to command the semiconductors. The term PWM is employed because the width of the pulses depends on the amplitude of the sinusoidal reference signal (fig. 3.1). Increasing the frequency of the triangular signal allows to increase of the number of pulses. A higher number of impulsions means a higher frequency of the harmonics, which are therefore more distant from the fundamental. The easier it is to filter the output signal, the smaller and lighter the filtering devices can be designed, therefore allowing to lessen the costs. This makes it easier to filter the harmonics and to obtain a good sinusoidal waveform. For that reason, it is good to work with a very high frequency, even if it is limited by the commutation capacitance of the semiconductors.

Two types of modulation strategies had to be chosen from: the 2-level and the 3-level modulation.

The 2-level modulation employs one sinusoidal reference signal and one triangular signal to set the number and the width of the pulses. Only two states are possible:

- **Status 1:** $S_2$, $S_4$ are conducting and $S_1$, $S_3$ are blocking: $V = U$
- **Status 2:** $S_3$, $S_1$ are conducting and $S_2$, $S_4$ are blocking: $V = -U$

If $t_1$ is the time where $V = U$ and $t_2$ where $V = -U$, the whole period $T$ of the signal is:

$$T = t_1 + t_2$$
3-level modulation uses either a second triangular or a second sinusoidal signal which is delayed by $\pi$ in order to create a third status, where $S_1$, $S_3$, or $S_2$, $S_4$ are closed at the same time (i.e. $V=0$) (fig. 3.2). On figure 3.2, 1 represents the pulses due to the first sinusoidal and 2 those due to the second sinusoidal reference signal. 3 is the comparison of 1 and 2 and the actual commuting signal.

More precisely, the states of the 3-level modulation are the following:

- $0 < \omega t < \pi$: $S_1$ closed and $S_2$ blocking
- $\pi < \omega t < 2 \cdot \pi$: $S_2$ closed and $S_1$ blocking
- $\beta < \omega t < \pi + \beta$: $S_4$ closed and $S_3$ blocking
- $\pi + \beta < \omega t < 2 \cdot \pi + \beta$: $S_3$ closed and $S_4$ blocking

The variable $\beta$ is called lag angle. This angle can be set to values between 0 and $\pi$, which allows to control of the value of the output voltage. When $\beta = 0$, a 2-level modulation is employed.

This modulation strategy has the same effect as increasing the frequency of the carrier signal. I.e., the number of pulses is twice as high as when using a 2-level modulation. Therefore the harmonics are more distant from the fundamental, which makes it easier to filter the signal (appendix A, FFT 2- and 3-level output signal).
For our project we have chosen the 3-level modulation strategy.

In this specific case, each switch is composed of an IGBT (Insulated Gate Bipolar Transistor) with a diode (fig. 3.3 and 3.4). The IGBTs are relatively new devices that have small switching losses and permit to work with high frequencies (generally from 1 to 30 kHz).

An IGBT is a transistor, which consists of a collector, a transmitter and a gate that permits to control its conducting and blocking status. This type of transistor supports high currents and therefore to control high power devices. Moreover they are quick switching devices that permit to work with high frequencies. Those characteristics allow to conceive smaller and lighter devices at lower costs compared to conventional transistors (e.g. GTO).

4. Simulation

In order to simulate the operation of a full bridge inverter, the software Orcad Capture CIS Version 9.2 was employed. First the inverter was designed with four IGBTs. Then an open loop simulation of a 2-level modulation was made, before executing the 3-level simulation with two triangular signals and the sinusoidal reference signal. All simulations were carried out with a linear load.

The aim of the simulation was a better understanding the topic of the work to be done and to establish a certain familiarity with the software and the simulation procedures. The results of the simulation and the design of the inverter are displayed in the appendices (appendix A).

5. Filter analysis

As the output of the inverter is not a perfect sinusoidal curve, a filter has to be placed between the inverter and the load. This filter has a very simple structure as it is composed of a capacitor and an inductor (fig. 5.1). The inductor permits to eliminate the ripple of the current and the capacitor eliminates the output voltage ripple. The aim of this high-frequency-filter is to get rid of the harmonics and to keep only the fundamental. As explained before, the modulation method is important to assure good filtering results.
The linear resistive load connected to the filter will called $R_L$. The transfer function of the filter is therefore:

$$F(j\omega) = \frac{V_{se}}{V_{if}} = \frac{1}{1 + \frac{j\omega L_F}{R_L} + (j\omega)^2 L_F C_F} \quad (5.1)$$

which can be written under its standardized form, using the Laplace method ($s = j\omega$):

$$F(s) = \frac{V_{se}}{V_{if}} = \frac{1}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}} \quad (5.2)$$

with $\omega_0 = \frac{1}{\sqrt{L_F C_F}}$ and $Q = \frac{R_L}{\sqrt{L_F C_F}}$.

Using the Bode diagram shows that this type of assembly composes a low pass filter permitting to keep only the fundamental of the input signal (see bode diagram, fig. 5.2). $Q$ is called the quality factor, which permits to control the peak at the corner frequencies $f_0$.

![Bode diagram of a LC low pass filter](image)

To build the low pass filter, several conditions have to be taken into consideration. Firstly, big variations of the current passing through the filter have to be avoided in order to preserve the inductor. In order to obtain this, a maximum admissible current $\Delta_{l_{\max}}$ was compulsory.

For $t \in [0;\pi]$, there are two states:

$$\begin{align*}
V_{if} &= E \\
V_{if} &= 0
\end{align*}$$

The general expression of the inductor voltage is:

$$L_F \frac{di}{dt} = V_{if} - V_{se}(\theta) = V_{if} - V_{se} \sin(\theta) \quad (5.3) \quad \theta \in [0;2\pi]$$

(5.3) leads to two equations:

$$\begin{align*}
L_F \frac{di}{dt} &= E - V_{se} \sin(\theta) \\
L_F \frac{di}{dt} &= V_{se} \sin(\theta)
\end{align*} \quad (5.4)$$
\[
\begin{align*}
L_F \frac{\Delta I_{\text{max}}}{\Delta t} &= E - V_{oF} \sin(\theta) \\
L_F \frac{\Delta I_{\text{max}}}{\Delta t} &= V_{oF} \sin(\theta)
\end{align*}
\]

(5.5)

In fact during \( t_1 \in [0; \pi] \), \( V_{oF} = E \) and during \( t_1 < t_2 \leq \pi \), \( V_{oF} = 0 \), with \( t_1 + t_2 = \frac{T_s}{2} \) (5.6)

Using \( t_1 \) and \( t_2 \) instead of \( \Delta t \) in (5.5), leads to:

\[
t_1 = \frac{L_F \cdot \Delta I_{\text{max}}}{E - V_{oF} \sin(\theta)} \quad \text{(5.7)} \quad \text{and} \quad t_2 = \frac{L_F \cdot \Delta I_{\text{max}}}{V_{oF} \sin(\theta)} \quad \text{(5.8)}
\]

Applying (5.7) and (5.8) in (5.6) one finally obtains:

\[
T_s = 2 \left[ L_F \cdot \Delta I \cdot \left( \frac{1}{E - V_{oF} \sin(\theta)} - \frac{1}{V_{oF} \sin(\theta)} \right) \right] = 2 \left[ L_F \cdot \Delta I \cdot \left( \frac{E}{(E - V_{oF} \sin(\theta)) \cdot (V_{oF} \sin(\theta))} \right) \right]
\]

The relation between the minimum value of the filter inductor \( L_{F\text{min}} \) and the switching frequency, the sinusoidal output signal and the input voltage is:

\[
L_F = \frac{T_s}{2\Delta I_{\text{max}}} \cdot \left( \frac{E}{(E - V_{oF} \sin(\theta)) \cdot (V_{oF} \sin(\theta))} \right)
\]

(5.9)

One can show that the minimum value for \( L_F \) to be employed is obtained when \( \theta = \frac{\pi}{4} \).

Moreover, the voltage ripple must be minimized. This implies the usage of a minimum capacitance \( C_{F\text{min}} \). Two restrictions are imposed.

The first one is a maximum variation of the output voltage ripple \( \Delta V_{\text{Ripple}} \) accepted that corresponds to a fixed percentage of the actual output voltage. Using the basic equations \( q = C_F \cdot V \) and \( q = \frac{1}{2} \cdot \Delta I \cdot t \) (in this case \( V = 2 \cdot \Delta V_{\text{Ripple}} \) and \( t = \frac{T_s}{4} \)), one can show the following equation that fixes a first minimum value to be chosen in order to determine the capacitance:

\[
C_{F\text{min}1} = \frac{\Delta I_{\text{max}}}{4} \cdot \frac{1}{\frac{T_s}{4} \cdot \Delta V_{\text{Ripple}}}
\]

(5.10)

The other condition to be respected is that the corner frequency must be at least 10 times smaller than the frequency of the output voltage ripple. Therefore the second relation is:

\[
C_{F\text{min}2} = \frac{100}{(2\pi f_0)^2 \cdot L_F}
\]

(5.11)
Those two equations ((5.10) and (5.11)) determine the minimum value of the capacitance. It is important to note that the capacitor, as well as the inductor, influences directly the Total Harmonic Distortion (THD). This fact has to be taken into consideration when dimensioning the filter, as the aim of the project is to have a $\text{THD} \leq 5\%$.

Different minimum inductance and capacitance values were calculated with the software Mathcad 2001 Professional using random values for the different parameters needed. An example of the calculating method used in order to find specific values of the inductance and the capacitance is added in appendix D.

6. Conclusion

After quick explanation of the general functioning of a full-bridge inverter, the study of the modulation strategies showed the advantages of the 3-level modulation. In fact this modulation together with an increased frequency of the carrier signal permits to obtain harmonics that are distant enough from the fundamental to ensure a good filtering. This fact allows to design cheaper, lighter and smaller filters. Simulating the inverter with Orcad and the filter design with Mathcad confirmed the theoretical approach and the method used to obtain satisfying results.

PART 2

7. Introduction

Designing an inverter, one has to follow certain steps and procedures. The first part of the work consists of designing a filter and to find the respective overall transfer function in an open loop setting (inverter + filter). Once this is done, one can go on with a closed loop study of the entire system. That means that the output voltage $V_{of}$ passes through a transducer before being compared to a sinusoidal reference signal. A controller checks the result of the comparison.

Having done the design of the filter in the first part of our study, the next step will be to determine the overall transfer function of the inverter and the filter. Finally, the voltage compensator (controller) will be designed.

![Fig. 7.1: Scheme of the plant](image-url)
8. Expression of \( V_{if} \) depending on the modulation strategy

In order to calculate the transfer function the same simplified presentation of the inverter-filter system as in part 1 (fig. 8.1) will be used.

![Simplified full-bridge inverter](image)

Fig. 8.1: Simplified full-bridge inverter

\( B_{1,2} \) and \( B_{3,4} \) represent the branches composed of \((S_1 \text{ and } S_2) \) and \((S_3 \text{ and } S_4) \) respectively. The two switches of one branch cannot conduct at the same time, as we explained in chapter 2. One can therefore consider that the switches of one branch are operating in a complementary manner. Defining the duty cycle \( D_x \) (with \( x \in \{1, 2, 3, 4\} \)) of a switch as \( D_x = \frac{t_{on}}{T_s} \) \((0 \leq D_x \leq 1)\) (8.1), leads to: \( D_2 = 1 - D_1 \) (8.2) and \( D_4 = 1 - D_3 \) (8.3).

Moreover, one can show that the expression of the average voltage at a and b are:

\[
\begin{align*}
V_a &= E \cdot d_1(t) \\
V_b &= E \cdot d_3(t)
\end{align*}
\tag{8.4}
\]

Working with very high frequencies, those average values of the voltages can be used to find the equation: \( V_{if} = V_a - V_b = E \cdot (d_1(t) - d_3(t)) \) (8.5), where \( d_1(t), d_3(t) \) are functions linked to the duty cycles of each branch. In fact, \( d_1(t) \in [-1; 1] \) is a variable representing the duty cycle of each branch.

As a sinusoidal waveform is desired, one can write:

\[
V_{if} \sin(\omega t) = E \cdot (d_1(t) - d_3(t))
\tag{8.6}
\]

One can prove that in 2-level and in 3-level modulation: \( d_3(t) = 1 - d_1(t) \) (8.7)

Replacing (8.7) in (8.6):

\[
\begin{align*}
d_1(t) &= \frac{1}{2} \left(1 + M \sin(\omega t)\right) \\
d_3(t) &= \frac{1}{2} \left(1 - M \sin(\omega t)\right)
\end{align*}
\tag{8.6, 8.7}
\]

10
M is the modulation index defined by:

\[ M = \frac{V_\text{af}}{E} \]  

(8.8)

Defining the modulation function as:

\[ d(t) = M \sin(\omega t) \]  

(8.9)

Finally:

\[ V_\text{af} = d(t) \cdot E \]  

(8.10)

9. Transfer function of the full-bridge inverter including the filter

Chapter 8 proved that the expression of \( V_\text{af} \) is the same no matter what type of modulation strategy is used. The overall transfer function of the plant will now be calculated.

\[ F(s) = \frac{V_\text{af}}{V_\text{af}} = \frac{1}{1 + \frac{s}{\omega_0} + \frac{s^2}{Q_0 \omega_0}} \]  

(5.2) with \( \omega_0 = \frac{1}{\sqrt{L_p C_F}} \) and \( Q = \frac{C_F}{L_F} \)

One can assume that \( R_L \approx \infty \), thus:

\[ F_{\infty}(s) = \frac{1}{1 + \frac{s^2}{\omega_0^2}} \]  

(9.1)

Using (8.10) in (9.1):

\[ G(s) = \frac{V_\text{af}}{d(t)} = \frac{E}{1 + \frac{s^2}{\omega_0^2}} \]  

(9.2)

The definition of the modulation function is:

\[ d(t) = \frac{V_{af}}{V_p} \]  

(9.3)

Using (9.3) with (9.2), leads to the final expression of the transfer function:

\[ G_{\text{final}}(s) = \frac{V_\text{af}}{V_{oc}} = \frac{E}{V_p} \cdot \frac{1}{1 + \frac{s^2}{\omega_0^2}} \]  

(9.4)

The filter design in an open loop circuit was simulated with Orcad Capture CIS Version 9.2 using the results of chapters 8 and 9 as well as the minimum capacitor and inductor values calculated with Matchcad 2001 Professional (appendix D). Figures 9.1 and 9.2 show the open loop simulation results for the inverter combined with the filter.
10. Characteristics of the voltage compensator

The voltage compensator is an important tool to control the value of the output voltage. As shown on figure 9.1, there are several components with a transfer function in the setting. The open loop transfer function (OLTF) is desired to present the following Bode diagram:
The crossing frequency $f_c$ is set to $\frac{1}{4}$ of the switching frequency. I.e.: 
$$f_c = \frac{f_s}{4}$$

The pole frequency $f_p$ is set to 40 times the corner frequency. I.e.: 
$$f_p = 40 \cdot f_0$$

In fact a pole frequency close to the switching frequency has to be avoided in order to prevent interferences when filtering. Therefore a random value much higher than $f_s$ has to be chosen.

Concerning the value of the crossing frequency, the theoretical value is $\frac{f_s}{2}$. In reality this doesn't work so a commonly adopted value is the one chosen.

The Bode diagram of the low pass filter used is illustrated in figure 5.2. That implies the following Bode diagram for the controller used:

![Bode diagram of the controller](image)

A slope of $-20$dB/decade is created by a transfer function of the form $H(s) = \frac{1}{s}$. As shown in figure 10.2, the slope is required to change to $+20$dB/decade at $f_0$. That means two zeros of the form $(s + \omega z_1)$ and $(s + \omega z_2)$ are needed at that frequency. The first will modify the slope of the controller diagram to 0dB/decade and the second to $+20$dB/decade. Finally a zero slope at a fixed frequency $f_z$ is desired, which implies a pole of the form $\frac{1}{s + \omega p}$. Combining those elements will lead to the general form of the controller transfer function:

13
\[ H(s) = \frac{(s + \omega_{z_1})(s + \omega_{z_2})}{s(s + \omega_p)} \quad (10.1) \]

The expressions of \( \omega_{z_1}, \omega_{z_2} \) and \( \omega_p \) according to the frequencies used are:

\[
\begin{align*}
\omega_{z_1} &= 2\pi \cdot f_0 \\
\omega_{z_2} &= 2\pi \cdot f_0 \\
\omega_p &= 2\pi \cdot f_p
\end{align*} \quad (10.2)

Furthermore, the value of the voltage transducer gain is set to \( T \).

In order to determine the gain of the voltage compensator, the expressions of the magnitudes of the filter, the transducer, the controller and the compensator are needed:

\[
\begin{align*}
G_{db}[G(s)] &= 20\log |G(s)| \\
G_{db}[H(s)] &= 20\log |H(s)| \\
G_{db}[T] &= 20\log |T| \\
G_{db}[K_C] &= 20\log |K_C|
\end{align*} \quad (10.3)

*Figure 10.1* shows that the magnitude of the whole setting will be zero for \( f = f_c \). That means:

\[ G_{db}[G(s)] + G_{db}[H(s)] + G_{db}[T] + G_{db}[K_C] = 0 \quad (10.4) \]

Thus the value of the compensator gain:

\[ K_c = 10^{\frac{-(G_{db}[G(s)] + G_{db}[H(s)] + G_{db}[T])}{20}} \quad (10.5) \]

From here on the overall compensator transfer function \( C(s) \) will be used:

\[ C(s) = K_c \cdot H(s) \quad (10.6) \]

Knowing the OLTF one can easily determine the CLTF by using the equation:

\[ \text{CLTF}(s) = \frac{\text{OLTF}(s)}{1 + \text{OLTF}(s)} \quad (10.7) \]

\[ \text{OLTF}(s) = G(s) \cdot H(s) \cdot K_c \cdot T \quad (10.8) \]

When using the closed loop transfer function (CLTF), there will be a restriction in order to maintain the stability of the system:

The restriction will be that the denominator of the CLTF cannot equal zero, i.e.:

\[ 1 + G(s) \cdot H(s) \cdot K_c \cdot T \neq 0 \quad (10.9) \]
That implies that neither $|G(s) \cdot H(s) \cdot K_c \cdot T| = 1$ (modulus of the OLT) nor $\text{angle}(G(s) \cdot H(s) \cdot K_c \cdot T) = 180^\circ$ (phase of the OLT).

11. Design of the voltage compensator

Knowing this restriction and the value of $K_c$, one can now proceed to the design of the compensator. A compensator design that is frequently used in power electronics (fig. 11.1) will be adopted and the values of its components will be calculated using the results obtained in chapter 10.

![Fig. 11.1: Adopted voltage compensator design](image)

In order to determine the values of the resistances and the capacitors, one has to calculate the transfer function of the operational amplifier. We suppose:

$$\begin{align*}
Z_{eq1} &= R_0 + \frac{R_1}{1 + j \omega R_1 C_1} \\
Z_{eq2} &= R_2 + \frac{1}{j \omega C_2} \quad (11.1)
\end{align*}$$

Applying the Millman theorem in A (see fig. 11.1) and supposing that the operational amplifier is perfect (i.e., $v^+ = v^-$), leads to the following transfer function:

$$TF_{\text{comp}}(s) = -\frac{R_2}{R_0} \cdot \frac{s + \frac{1}{R_2 C_2}}{s + \frac{1}{R_1 C_1}} \cdot \frac{s + \frac{R_1 + R_0}{R_0 R_1 C_1}}{s + \frac{R_1 + R_0}{R_0 R_1 C_1}} \quad (11.2)$$

By comparison, using the overall compensator transfer function calculated before (equation (10.6)), the values of $R_0, R_2, C_1, C_2$ can be determined. $R_1$ was set to a certain value.
\[
\begin{align*}
C_e &= \frac{1}{\omega_C \cdot R_1} \\
R_0 &= \frac{R_1}{\omega_P \cdot R_1 \cdot C_1 - 1} \\
R_2 &= R_0 \cdot K_c \\
C_2 &= \frac{1}{\omega_C \cdot R_2}
\end{align*}
\] (11.3)

Once the theoretical values found, a simulation of the voltage compensator using Mathcad 2001 Professional was conducted. This simulation is added in appendix D.

12. Further restriction for the filter design

When using the plant in a closed loop a third restriction appears. In fact as the output signal will be compared to the carrier signal, it is important that the slope of the output voltage ripple is not higher than the carrier signal slope, in order to prevent multiple crossings of the two signals. That would imply an increase of the switching frequency in an uncontrolled manner and could destroy or at least harm the inverter. Therefore the following condition appears:

\[
S_R \cdot T_v \cdot |C(f_x)| \leq S_T
\] (12.1)

where: \( S_R = \frac{\Delta T \cdot \pi}{8 \cdot C_{\text{min}}^3} \) is the slope of the output voltage ripple, \( T_v \) the voltage transducer gain, \( S_T = \frac{4V_T}{T_s} \) the slope of the triangular carrier signal and \( C(f_c) \) the controller transfer function for a fixed frequency (\( f_x = f_s \) for 2-level modulation and \( f_x = 2f_s \) for 3-level modulation).

In order to find the minimum capacitor that has to be used, one first has to re-write \( K_c \) as a function of an unknown capacitor \( C_{\text{min}}^3 \), using the same conditions as in chapter 10, i.e. \( f = f_c \). Once this is done, \( C(s) \) [(10.6)] has to be calculated as a function of \( C_{\text{min}}^3 \) using the output ripple frequency, which is twice the switching frequency. Finally the new expression of \( C(s) \) can be replaced in [(12.1)]. The calculations were done using Mathcad 2001 Professional and its results are added in appendix D.

13. Simulation results

After having theoretically designed the filter and the voltage compensator, the values of its components were calculated with Mathcad 2001 Professional. Those values were used for a simulation of the plant using Orcad Capture CIS 9.2. The following waveforms show the results of this simulation. Appendix B shows the overall plant that was used for the simulation.

The main interest was to check the behavior of the plant design, especially the obtained output signal that was desired to be sinusoidal. Figure 13.1 shows the filter input voltage (fig. 13.1 a) and the filter output voltage (fig. 13.1 b), which is the voltage of the load, for the closed loop circuit.
The obtained output voltage is sinusoidal, which proves that the Mathcad calculations were correct. A zoom of figure 13.1 allows comparing the filter output voltage and the desired perfectly sinusoidal waveform (fig. 13.2). The figure shows that the real output voltage ripple is smaller than the imposed theoretic value of $IV$.

Another interesting comparison can be done between the triangular carrier voltage $V_T$ and the controller output voltage $V_c$. A very common problem in inverter design is to keep the
slope of $V_c$ lower than the slope of $V_T$. Figure 13.3 shows that this requirement has be respected for the plant. The zoom was done at $\frac{\pi}{2}$, where the slope of the ripple is highest.

![Comparison of the carrier voltage with the controller output voltage](image)

Fig. 13.3: Comparison of the carrier voltage with the controller output voltage

Finally a simulation of a changing load was done. Figure 13.4 shows the voltage transients of the change from half load to full load and figure 13.5 the change from full load to half load. The transient over voltage has to be limited because it can heavily damage the load. Another important factor when changing the load is the speed of the return to the steady-state.

![Voltage transient, full load to half load](image)

Fig. 13.4: Voltage transient, full load to half load

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Figures 13.6-13.10 show the waveforms of the voltages and currents of the DC source, one switch, the capacitor and the inductor.

Fig. 13.5: Voltage transient, half load to full load

Fig. 13.6: Current of the DC source
In figure 13.8 it is easy to verify that the calculated maximum current ripple of the inductor current is smaller than the value calculated with Mathcad 2001 Professional (appendix B). The Mathcad value is 10.4 Amperes.
**Fig. 13.9**: Switch voltage (13.9 a)  
Switch current (13.9 a)

**Fig. 13.10**: Switch voltage (13.10 a)  
Switch current (13.10 a)
14. Conclusion

The first problem encountered in this part of the study was to define the filter input voltage $V_{in}$ depending on the inverter input voltage $E$. That was possible using the so-called modulation function.

Once the value of the filter output voltage depending on $E$ was obtained, a controller that permitted us to obtain the desired transfer function and the Bode diagram wanted could be defined. In fact the controller transfer function had to possess two zeros and one pole in order to fulfill requirements. Defining the corner frequencies didn’t pose a problem as certain restrictions had to be respected, implying these frequencies.

When having calculated the different transfer functions, magnitudes and gains, a voltage compensator model was chosen that is very frequently used in industrial applications. Knowing all the different restrictions of the theoretical controller transfer function, the specific values could be determined. This was done by identifying the unknown values of the components used in the industrial application using the theoretical values.

Finally a third restriction on the filter capacitor that appears when working with a closed loop had to be studied. It appears that this is not a real restriction as the study showed that any kind of capacitor responding to the first two restrictions could be used.

PART 3

15. Introduction

In the first part of the study the inverter design was carried out for linear loads. This type of load is very rare in reality and most of the devices using converters are nonlinear loads. The next step of the inverter design will therefore be the study of the behavior of the designed full-bridge inverter, filter and voltage compensator when a nonlinear load replaces the linear one.

First of all, a very general explication of nonlinear loads is given. This revision allows to understand the problems created by this type of load. Then, a load that is mostly used in all kinds of devices is connected to the inverter-filter-compensator system instead of the resistance that was used so far. The study of the new plant will show the problems that arise with nonlinear loads.

Once the simulation was carried out, a new filter and a new voltage compensator have to be designed. The new components and the behavior of the system will be simulated with Orcad Capture CIS 9.2.

16. Theoretical study of nonlinear loads

This project will be limited to the study of the load represented in figure 16.1. It represents the by far most common type of nonlinear load. This load will also be employed in the inverter design of this project.

There are the following three states of the load during a semi-period (figures 16.1, 16.2).
1. $\theta_1 \leq \theta < \frac{\pi}{2}$: diodes $D_2$ and $D_3$ are conducting and $i_t = i_c + i_R$ (16.1) (see fig. 16.1 a)

2. $\frac{\pi}{2} \leq \theta < \theta_2$: diodes $D_2$ and $D_3$ are conducting and $i_R = i_c + i_t$ (16.2) (see fig. 16.1 b)

3. $\theta_2 \leq \theta < \theta_3$: diodes $D_2$ and $D_3$ are blocking and $i_t = 0$ (16.3) (see fig. 16.1 c)

Fig. 16.1 a: State 1

Fig. 16.1 b: State 2

Fig. 16.1 c: State 3

Fig. 16.2: Load input current $i_t$, load input voltage $V_L$ and load capacitor voltage $V_C$
During this time diodes $D_1$ and $D_4$ are constantly blocking.

During state 1 the capacitor voltage $V_c$ is the same as the sinusoidal input voltage $V_{il}$. When $\theta$ reaches $\frac{\pi}{2}$ the capacitor current starts to change direction and the capacitor discharges itself. As soon as $V_c \geq V_{il}$, the diodes will block.

Be $V_c = V_{peak} \cdot \sin(\theta)$ \hspace{1cm} (16.4)

During $\theta \in \left[\theta_2; \theta_3\right]$ the capacitor current is: $i_c = C \frac{dV_c}{dt} = C \omega \frac{dV_c}{\omega \cdot dt}$ \hspace{1cm} (16.5)

Using (16.4) in (16.5) leads to: $i_c = C \omega V_c \cos(\theta)$ \hspace{1cm} (16.6)

One can choose the parameters in a way that the capacitor voltage ripple is very small. Doing this permits to assume that the resistance current is constant. Its expression therefore is:

\[ i_R = \frac{V_{peak}}{R} \hspace{1cm} (16.7) \]

Replacing $i_R$ and $i_c$ in (16.1) using expressions (16.6) and (16.7) leads to:

\[ i_i = \frac{V_{peak}}{R} + C \omega V_c \cos(\theta) \hspace{1cm} (16.8) \]

Knowing that $i_i = 0$ for $\theta \in \left[\theta_2; \theta_3\right]$, one obtains:

\[ 0 = \frac{V_{peak}}{R} + C \omega V_c \cos(\theta) \hspace{1cm} (16.9) \]

That leads to:

\[ \cos(\theta_3) = -\frac{1}{RC\omega} \hspace{1cm} (16.10) \]

Be $t_{charge}$ the time corresponding to $\theta_1 \leq \theta < \frac{\pi}{2}$. The minimum value of the capacitor voltage $V_{c_{min}}$ can thus be written:

\[ V_{c_{min}} = V_{peak} \sin(2\pi f t_{charge}) \hspace{1cm} (16.11) \]

Resolving this equation leads to:

\[ t_{charge} = \frac{\arccos \left( \frac{V_{c_{min}}}{V_{peak}} \right)}{2\pi f} \hspace{1cm} (16.12) \]

Using the basic equation $\Delta q = i_c \cdot t_{c_{peak}} = CAV$ (16.13), one can show that the peak value of the capacitor current $I_{c_{peak}}$ is written:
\[ I_{\text{peak}} = \frac{C(V_{\text{peak}} - V_{\text{cmn}})}{t_c} \]  \hspace{1cm} (16.14)

Furthermore, one can express the energy of the plant as:

\[ W_m = \frac{P_{\text{in}}}{f} = C\left(V_{\text{peak}}^2 - V_{\text{cmn}}^2\right) \]  \hspace{1cm} (16.15)

Thus, the capacitance needed to fulfill the desired ripple specifications can be calculated:

\[ C = \frac{P_{\text{in}}}{f\left(V_{\text{peak}}^2 - V_{\text{cmn}}^2\right)} \]  \hspace{1cm} (16.16)

One obtains the same results for the second semi-period.

17. Specification of the nonlinear load employed

The actual nonlinear load employed in this project is more or less the same as described in chapter 16. The only difference is the inductor added between the power source and the load. The inductor at the load input allows to set the crest factor of the load to a desired value. It also prevents the load input current from being too high, which could damage the circuit. The load inrush current can be limited by using the device displayed in figure 17.1 between the filter and the load. The semiconductor \( S \) can be set to close at an appropriate time.

![Fig. 17.1: Device to lessen the inrush current](image)

Furthermore using a load input inductor permits to limit the voltage drop in the filter inductor. The maximum admissible voltage drop is given by the difference between the inverter input voltage and the filter output voltage:

\[ v_{\text{drop}} = E - V_{\text{ef}} \]  \hspace{1cm} (17.1)

The aim of the project is to work with an average power of 3kVA. Using this value in an Orcad Capture simulation leads to an active power of \( P=1950W \). So the power factor equals \( \cos(\phi) \approx \frac{2}{3} \).
Using the active power value, the values of the capacitance and the resistance of the nonlinear load could be calculated (appendix D).

Knowing the values of the capacitance and the resistance, it is possible to determine the inductance needed in order to obtain a crest factor $CF=3$. It is interesting to fix the crest factor to a low value, because a high crest factor means a low filter inductor. That would imply a higher filter current ripple, which is not desirable as it causes an increase of the losses of the inverter.

The expression of the crest factor is:

$$CF = \frac{I_{\mu, \text{rms}}}{I_{\mu, \text{peak}}}.\quad (17.2)$$

Once the simulation has been carried out with a random inductance, the software permits to determine easily the peak value and the efficient value of $I$. Using equation (17.2) one can calculate the crest factor. There is a mathematical approach to determine directly the inductance knowing the crest value, but it is very complex and takes a lot of time. For that reason the experimental method was chosen in order to obtain the desired $CF$.

The inductance that was found in order to obtain $CF=3$ is $160 \mu H$. The waveforms of $I_\mu$ and $I_{\mu, \text{rms}}$ are displayed in figure 17.2.

![Fig. 17.2: RMS and real load input current](image)

The results of the Mathcad 2001 Professional calculations (appendix D) and the experimental determination of the load input inductance allowed to carry out the simulation of the nonlinear load. The results are displayed in figure 17.3.
18. Simulation of the whole plant

After the theoretical approach in chapter 16 and the simulation of the nonlinear load on its own in chapter 17, the linear load of the plant was replaced by the nonlinear one. The characteristics of the filter and the voltage compensator were maintained (appendix C).

When using a nonlinear load, a feedback control is very important. In fact, the open loop plant is not steady and high voltage distortion can be observed even with good parameters (figure 18.1). Operating the system with a feedback control does not necessarily prevent distortion. It is very important to set a convenient modulation factor and an appropriate filter inductor in order to obtain a minimum distortion.

This imposes a further restriction when choosing the filter inductor. Its value influences the voltage drop that can be observed at the filter output. As the load imposes a maximum admissible voltage drop, the filter inductance must not be higher than a certain maximum value.
The detailed calculations with a randomly chosen value of the admissible voltage drop (70V) are added in appendix D.

In the case of this project, the parameters chosen for the linear system satisfied the requirements of the new load as well. The obtained filter output voltage met the requirements (low distortion) and no modification of the plant had to be carried out. The results of the simulation are shown in figure 18.2.

![Fig. 18.2: Load input voltage \( V_{\text{IL}} \), load output voltage \( V_{\text{d}} \) and load input current \( I_{\text{IL}} \)](image)

Usually an inverter has to be redesigned several times before finding the optimal parameters to be chosen. It is very rare to find satisfying results with the first design. That's why it has been decided to artificially disturb the system, in order to show the distortions that can occur.

The parameters causing those unwanted effects are the value of the modulation factor

\[
m = \frac{V_{\text{output}}}{E} \quad (m \in [0:1]) \quad \text{(18.1)}
\]

and the value of the filter inductor \( L_{\text{F}} \). When \( m \) approaches 1, i.e. when the input voltage is nearly the same as the output voltage, the filter output waveform is as shown on figure 18.3. The exact value used is: \( m=0.9978 \).

![Fig. 18.3: Distorted load input voltage \( V_{\text{IL}} \), load output voltage \( V_{\text{d}} \) and load input current \( I_{\text{IL}} \)](image)
Increasing the inductance of the filter inductor to 1300μH leads to the waveforms displayed in figure 18.4.

![Waveform Diagram](image)

*Fig. 18.4: Distorted load input voltage $V_{dl}$, load output voltage $V_{dl}$, and load input current $I_{dl}$*

When using the maximum admissible filter inductance calculated (appendix D), the instability of the filter output voltage, which is the load input voltage, appears. This distortion is however small enough to be neglected.

*Figure 18.5* finally shows the filter output waveform using an increased filter inductance of 600μH as well a modulation factor $m=0.9978$. When observing the filter input voltage, one can clearly see the problems a maladapted nonlinear load can cause. In fact, during the voltage distortion of the filter output voltage (i.e., the load input voltage), the switches are not commutating any more.

![Waveform Diagram](image)

*Fig. 18.5: Distorted load input voltage $V_{dl}$, load output voltage $V_{dl}$, filter input voltage $V_{df}$ and load input current $I_{dl}$*

Should a distortion of the filter output voltage be discovered when changing the nature of the load (linear to nonlinear), one has to change the parameters mentioned above. There is no mathematical solution to resolve the problems encountered and all improvement of the output waveform has to be obtained by an experimental approach.
19. Conclusion

After having designed the nonlinear load to obtain a crest factor of 3, this nonlinear load was integrated into the closed loop circuit replacing the linear load used in the precedent parts of the project. This was necessary, because linear loads do basically not exist in reality. Therefore designing an inverter for linear loads only doesn’t make sense. The model of the most common nonlinear load that can be found in devices was employed, in order to guarantee a maximum compatibility.

The problems (especially voltage distortion) arising when using a nonlinear load in a circuit designed for linear loads did not appear for the current project. The parameters calculated for the linear load in part 2 perfectly worked for the nonlinear one as well. This is rather rare and usually voltage distortion will occur. Therefore it was considered to be useful to maintain the found parameters for the final inverter, but nevertheless to simulate possible distortion problems by modifying the values of the modulation factor \( m \) and of the filter inductor \( L_f \).

Conclusion

The theoretical design of a voltage inverter demands great precision when calculating the different parameters and restrictions that will have to be applied when conceiving the model. The first step of such an undertaking was to define the requirements that have to be met for the desired converter. One of the main objectives was to achieve a quasi-perfect sinusoidal waveform of the output voltage as well as reducing the costs, the size and the weight of the device. The chosen 3-level modulation permitted to obtain a very satisfying compromise of those goals.

Once this had been done, it was possible to proceed to the filter design and the voltage compensator design employing linear loads. Performing closed loop simulations and replacing the linear load by a nonlinear load imposed additional restrictions for the filter design. Using a nonlinear load showed how important it is to work with feedback control and to choose the right parameters, in order to avoid voltage distortion that can heavily harm the device connected to the voltage inverter.

There are various tools available for calculating the parameters and restrictions, but for this project the program Mathcad 2001 Professional had been chosen. It is a very simple to use yet powerful computer application. One can change single parameters and the software will automatically calculate all values and graphics depending on the modified parameters. That made it very easy to adjust the design, when problems with the actual setting had been encountered.

Those calculation results just represent the basics of the design work. Once they have been determined, it is important to use different computer programs in order to check the functioning and behavior of the plant under certain conditions. For the current project mainly Orcad Capture CIS Version 9.2 (PSpice) has been used. Some checks have been carried out with Psim, which has been especially programmed for power electronics. This part of the theoretical conception is very important to avoid superfluous costs when assembling the prototype.
Nomenclature

E: Continuous voltage source
V_if: Filter input voltage
V_of: Filter output voltage
V_oc: Controller output voltage
V_p: Peak voltage of the carrier signal
V_ref: Reference voltage
V_ii: Load input voltage
V_ol: Load output voltage
v_drop: Voltage drop
I_in: Load input current
I_peak: Peak value of the load input current
I_RMS: Root Means Square (RMS) value of the load input current
L_f: Value of filter inductor
C_f: Value of filter capacitor
R_L: Value of linear resistive load
\omega_0: corner pulsation
f_0: corner frequency \( f_0 = \frac{\omega_0}{2\pi} \)
f_c: Crossing frequency
f_p: Pole frequency
f_s: Switching frequency
T_s: Switching period \( T_s = \frac{1}{f_s} \)

OLTIF: Open Loop transfer Function
CLTF: Closed Loop Transfer Function
F(s): Standardized low pass filter transfer function
G(s): Final filter transfer function
H(s): Controller transfer function (without gain)
K_c: Controller gain
C(s): Controller transfer function (with gain)
TF(s): Operational amplifier transfer function
T: Transducer gain
Q: Quality factor
s: Laplace variable
D: Duty cycle
d(t): modulation function
m: Modulation factor
CF: Crest factor
\(\cos(\phi)\): Power factor
\(P_o\): Output power
\(P_{in}\): Load input power
\(W_{in}\): Load input energy
\(t_{\text{charge}}\): Capacitor charging time
t: Time
q: Charge
i: Current
References


Appendix A

Sinusoidal 2 level modulation with resistive load

Sinusoidal 3 level modulation with resistive load

3-level modulation curves
Appendix D

Filter Design for a 3-level Modulation Single Phase Full-bridge Inverter Compensator Design  Non-Linear Load

**Specifications**

\[
\begin{align*}
\text{P}_0 &:= 3000 \quad \text{V} \cdot \text{A} \\
\text{P} &:= 1950 \quad \text{W} \\
\cos(\Phi) &:= \frac{\text{P}}{\text{P}_0} \quad \cos(\Phi) = 0.65 \\
V_i &:= 250 \quad \text{V} \\
f_s &:= 20 \cdot 10^3 \quad \text{Hz} \\
T_s &:= \frac{1}{f_s} \quad \text{s} \\
f_r &:= 2 \cdot f_s \quad \text{Hz} \\
V_p &:= 5 \quad \text{V} \\
\text{teta} &:= 0,0.01..2\pi \\
V_{\text{of}} &:= 179.61 \quad \text{V} \\
V_0 &:= 127 \quad \text{V} \\
f &:= 60 \quad \text{Hz} \\
M &:= \frac{V_{\text{of}}}{V_i} \quad M = 0.718 \\
didt &:= 54.894 \cdot 10^3 \quad \text{A} \cdot \text{s}^{-1}
\end{align*}
\]

**Non-Linear Load**

Load resistance \( R_0 := \frac{V_{\text{of}}^2}{\text{P}} \quad R_0 = 16.543 \quad \Omega \)

Design of the Load capacitor

\[
V_{\text{cmin}} := 160 \quad \text{V} \quad \text{Minimal Capacitor Voltage allowed}
\]

\[
C := \frac{\text{P}}{f \cdot (V_{\text{of}}^2 - V_{\text{cmin}}^2)} \quad C = 4.88 \times 10^{-3} \quad \text{F}
\]
Appendix D

Filter Inductance

Maximum inductance current allowed

\[ \Delta I_{\text{max}} := 11 \text{ A} \]

Maximal inductance current

\[ L_{f_{\text{min}}} = \frac{\Delta I}{2 \cdot \Delta I_{\text{max}}} \left( V_i - V_{o_f} \cdot \sin \left( \frac{\pi}{4} \right) \right) \left( V_{o_f} \cdot \sin \left( \frac{\pi}{4} \right) \right) \]

Minimal Inductance

\[ L_{f_{\text{min}}} = 1.42 \times 10^{-4} \text{ H} \]

Another restriction for the filter Inductance : Voltage drop

The voltage drop in the filter inductance is fixed to \( \Delta V_{\text{drop}} := V_i - V_{o_f} \)

\[ L_{f_{\text{max}}} = \frac{\Delta V_{\text{drop}}}{\frac{d}{dt}} \]

\[ L_{f_{\text{max}}} = 1.282 \times 10^{-3} \text{ H} \]

\[ L_f := 150 \times 10^{-6} \text{ H} \]

Chosen Inductance

Maximum current ripple

\[ \Delta I(\text{teta}) := \begin{cases} \frac{T_s}{(2 \cdot L_f)} \left( V_i - V_{o_f} \cdot \sin(\text{teta}) \right) \left( V_{o_f} \cdot \sin(\text{teta}) \right) & \text{if } \text{teta} \leq \pi \\ \frac{T_s}{(2 \cdot L_f)} \left( -V_i - V_{o_f} \cdot \sin(\text{teta}) \right) \left( V_{o_f} \cdot \sin(\text{teta}) \right) & \text{if } \text{teta} > \pi \end{cases} \]

\[ \Delta I \left( \frac{\pi}{4} \right) = 10.414 \text{ A} \]
Appendix D

Filter Capacitor

First restriction: voltage ripple

We fixed the maximum current ripple to $\Delta V_{\text{Ripple}} := 1 \text{ V}$

$$C_{\text{min1}} := \frac{\Delta I \left( \frac{\pi}{4} \right)}{8} \frac{T_s}{2\Delta V_{\text{Ripple}}}$$

$C_{\text{min1}} = 3.254 \times 10^{-5} \text{ F}$ Minimal capacitance depending on voltage ripple

Second restriction: Filter corner frequency

The corner frequency must be 10 times smaller than the ripple frequency.

$$C_{\text{min2}} := \frac{100}{\left(2 \pi f_f\right)^2 L_f}$$

$C_{\text{min2}} = 1.055 \times 10^{-5} \text{ F}$

$C_f := 3.3 \times 10^{-5} \text{ F}$

$$\Delta V(\text{teta}) := \Delta I(\text{teta}) \cdot \frac{T_s}{2C_f}$$

$$\Delta V \left( \frac{\pi}{4} \right) = 0.986 \text{ V}$$

![Graph showing the voltage ripple over theta](image)

Corner Frequency

$$f_0 := \frac{1}{2\pi \sqrt{L_f C_f}}$$

$f_0 = 2.262 \times 10^3 \text{ Hz}$
Compensator Design

\[ f_c := \frac{f_s}{4} \]

\[ f_c = 5 \times 10^3 \text{ Hz} \]

\[ j := \sqrt{-1} \]

\[ f := 10, 10.1 \ldots 10^4 \]

The transfer function of the plant is:

\[ G(f) := \frac{V_i}{V_p} \frac{1}{1 + L_f C_f (2\pi f \cdot f)^2} \]

\[ G_{\text{mod}}(f) := 20 \cdot \log(|G(f)|) \]

\[ G_{\text{phase}}(f) := \arg(G(f)) \]

\[ f_0 = 2.262 \times 10^3 \text{ Hz} \]  

Corner frequency of the plant
Appendix D

The transfer function of the controller is
\[ H(f) := \frac{(j \cdot 2\pi \cdot f + 2\pi \cdot f_{c_1})}{j \cdot 2\pi f} \cdot \frac{(j \cdot 2\pi \cdot f + 2\pi \cdot f_{c_2})}{(j \cdot 2\pi \cdot f + 2\pi \cdot f_p)} \]

The zeros frequencies are equal to the filter corner frequency

\[ f_{c_1} := f_0 \quad \text{thus} \quad f_{c_1} = 2.262 \times 10^3 \quad \text{Hz} \]

\[ f_{c_2} := f_0 \quad \text{thus} \quad f_{c_2} = 2.262 \times 10^3 \quad \text{Hz} \]

The second pole frequency must be 40 times the filter corner frequency

\[ f_{cp} := 40 \cdot f_0 \quad \text{thus} \quad f_{cp} = 9.049 \times 10^4 \quad \text{Hz} \]

\[ H_c(f) := \frac{(j \cdot 2\pi \cdot f + 2\pi \cdot f_{c_1})}{j \cdot 2\pi f} \cdot \frac{(j \cdot 2\pi \cdot f + 2\pi \cdot f_{c_2})}{(j \cdot 2\pi \cdot f + 2\pi \cdot f_{cp})} \]

\[ H_{cm}(f) := 20 \log \left| H_c(f) \right| \]

\[ H_{cp}(f) := \arg(H_c(f)) \]
Appendix D

The magnitude of the plant for the crossing frequency is:

\[ G_{fc} := G_{\text{mod}}(f_c) \quad G_{fc} = 22.191 \text{ dB} \]

The magnitude of \( H_c \) for the crossing frequency is:

\[ H_{cfc} := H_{\text{cmod}}(f_c) \quad H_{cfc} = -23.548 \text{ dB} \]

The magnitude of the transducer is:

\[ T_{v} := 0.025 \]
\[ T_{vdB} := 20 \cdot \text{log}(T_{v}) \quad T_{vdB} = -32.041 \text{ dB} \]

The total magnitude of the system must be zero dB at the crossing frequency. Thus we obtain the compensator gain \( K_c \).

\[ K_{cdB} := -(G_{fc} + H_{cfc} + T_{vdB}) \]
\[ K_{cdB} = 33.399 \text{ dB} \]

Then the absolute value of the compensator \( K_c \)

\[ K_{C} := 10^{\frac{K_{cdB}}{20}} \quad K_C = 46.766 \]

\[ 20 \cdot \text{log} \left( |K_C \cdot H_c(f)| \right) \]
Appendix D

**Open-Loop Transfer Function**

\[
\text{OLTF}(f) := K_c \cdot H_c(f) \cdot T_c \cdot G(f)
\]

\[
\text{OLTF}_{\text{dB}}(f) := 20 \cdot \log\left(\left|\text{OLTF}(f)\right|\right)
\]

\[
\text{OLTF}_{\text{phase}}(f) := \arg(\text{OLTF}(f))
\]

\[
\text{OLTF}_{\text{dB}}(f_c) = -4.822 \times 10^{-15}
\]

**Phase margin**

\[
\phi := \pi + \text{OLTF}_{\text{phase}}(f_c)
\]

\[
\phi = 0.666 \quad \text{radian} \quad \text{or} \quad \phi_{\text{deg}} := \frac{\phi \cdot 180}{\pi} \quad \phi_{\text{deg}} = 38.151 \quad \text{degrees}
\]
Compensator Parameters

Fixing $R_1$,

\[
C_1 := \frac{1}{2\pi \cdot f_{czl} \cdot R_1}
\]

\[
R_0 := \frac{R_1}{R_1 \cdot C_1 \cdot 2\pi \cdot f_{cp} - 1}
\]

\[
R_2 := K_e \cdot R_0
\]

\[
C_2 := \frac{1}{2\pi \cdot f_{czl} \cdot R_2}
\]

\[
\text{TF}_{\text{opamp}}(f) := \frac{R_2}{R_0} \cdot \frac{j \cdot 2 \cdot \pi \cdot f + \frac{1}{R_1 \cdot C_1}}{j \cdot 2 \cdot \pi \cdot f}
\]

\[
\text{TF}_{\text{dB}}(f) := 20 \cdot \log\left(\left|\text{TF}_{\text{opamp}}(f)\right|\right)
\]

\[
\frac{\text{TF}_{\text{dB}}(f)}{20 \log\left|K_e \cdot H_e(f)\right|}
\]

\[
R_1 := 10^4 \ \Omega
\]

\[
C_1 = 7.036 \times 10^{-9} \ \text{F}
\]

\[
R_0 = 256.41 \ \Omega
\]

\[
R_2 = 1.199 \times 10^4 \ \Omega
\]

\[
C_2 = 5.867 \times 10^{-9} \ \text{F}
\]